**Verification of PI3LVD512 IBIS model**

1. **Introduction:**

To verify the correlation between the ibis model and hspice model, we need to do some simulations:

1. Add **50Ω** pull-down resistor to the INPUT:

PI3LVD512

**OUTP**

**SCL\_C**

**SDA\_C**

**OUTN**

**SCL\_C**

**SDA\_C**

200Ω

**SCL\_C**

**SDA\_C**

200Ω

**SCL\_C**

**SDA\_C**

50Ω

**SCL\_C**

**SDA\_C**

A0

**SCL\_C**

**SDA\_C**

C

**SCL\_C**

**SDA\_C**

C

**SCL\_C**

**SDA\_C**

**Differential Signals**

**SCL\_C**

**SDA\_C**

50Ω

**SCL\_C**

**SDA\_C**

A1

**SCL\_C**

**SDA\_C**

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0B1

**SCL\_C**

**SDA\_C**

1B1

**SCL\_C**

**SDA\_C**

**INP**

**SCL\_C**

**SDA\_C**

**INN**

**SCL\_C**

**SDA\_C**

200Ω

**SCL\_C**

**SDA\_C**

200Ω

**SCL\_C**

**SDA\_C**

**6.0V**

**SCL\_C**

**SDA\_C**

**6.0V**

**SCL\_C**

**SDA\_C**

1. The frequency of signal is **50MHz**:

vin1 inp 0 pulse ( 3 0 0 .2n .2n 9.8n 20n)

vin2 inn 0 pulse ( 0 3 0 .2n .2n 9.8n 20n)

1. Add **10pF** pull-down capacitance to the output;
2. Add **50pF** pull-down capacitance to the output;
3. The frequency of signal is **250MHz**:

vin1 inp 0 pulse ( 3 0 0 0.1n 0.1n 1.9n 4n)

vin2 inp 0 pulse ( 0 3 0 0.1n 0.1n 1.9n 4n)

1. Add **10pF** pull-down capacitance to the output;
2. Add **50pF** pull-down capacitance to the output;
3. Add **50Ω** resistor between the INPUT and IC’s PIN:

PI3LVD512

**OUTP**

**SCL\_C**

**SDA\_C**

**OUTN**

**SCL\_C**

**SDA\_C**

200Ω

**SCL\_C**

**SDA\_C**

200Ω

**SCL\_C**

**SDA\_C**

50Ω

**SCL\_C**

**SDA\_C**

A0

**SCL\_C**

**SDA\_C**

C

**SCL\_C**

**SDA\_C**

C

**SCL\_C**

**SDA\_C**

**Differential Signals**

**SCL\_C**

**SDA\_C**

50Ω

**SCL\_C**

**SDA\_C**

A1

**SCL\_C**

**SDA\_C**

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0B1

**SCL\_C**

**SDA\_C**

1B1

**SCL\_C**

**SDA\_C**

**INP**

**SCL\_C**

**SDA\_C**

**INN**

**SCL\_C**

**SDA\_C**

200Ω

**SCL\_C**

**SDA\_C**

200Ω

**SCL\_C**

**SDA\_C**

**6.0V**

**SCL\_C**

**SDA\_C**

**6.0V**

**SCL\_C**

**SDA\_C**

1. The frequency of signal is **50MHz**:

vin1 inp 0 pulse ( 3 0 0 .2n .2n 9.8n 20n)

vin2 inn 0 pulse ( 0 3 0 .2n .2n 9.8n 20n)

1. Add **10pF** pull-down capacitance to the output;
2. Add **50pF** pull-down capacitance to the output;
3. The frequency of signal is **250MHz**:

vin1 inp 0 pulse ( 3 0 0 0.1n 0.1n 1.9n 4n)

vin2 inp 0 pulse ( 0 3 0 0.1n 0.1n 1.9n 4n)

1. **Without** pull-down capacitance to the output;
2. Add **10pF** pull-down capacitance to the output;
3. **Conclusion:**
4. For SWITCH1, the simulation results of IBIS model can match very well with the HSPICE model at different simulating conditions.

1. **Simulation Result:**
2. Add **50Ω** pull-down resistor to the INPUT:

PI3LVD512

**OUTP**

**SCL\_C**

**SDA\_C**

**OUTN**

**SCL\_C**

**SDA\_C**

200Ω

**SCL\_C**

**SDA\_C**

200Ω

**SCL\_C**

**SDA\_C**

50Ω

**SCL\_C**

**SDA\_C**

A0

**SCL\_C**

**SDA\_C**

C

**SCL\_C**

**SDA\_C**

C

**SCL\_C**

**SDA\_C**

**Differential Signals**

**SCL\_C**

**SDA\_C**

50Ω

**SCL\_C**

**SDA\_C**

A1

**SCL\_C**

**SDA\_C**

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0B1

**SCL\_C**

**SDA\_C**

1B1

**SCL\_C**

**SDA\_C**

**INP**

**SCL\_C**

**SDA\_C**

**INN**

**SCL\_C**

**SDA\_C**

200Ω

**SCL\_C**

**SDA\_C**

200Ω

**SCL\_C**

**SDA\_C**

**6.0V**

**SCL\_C**

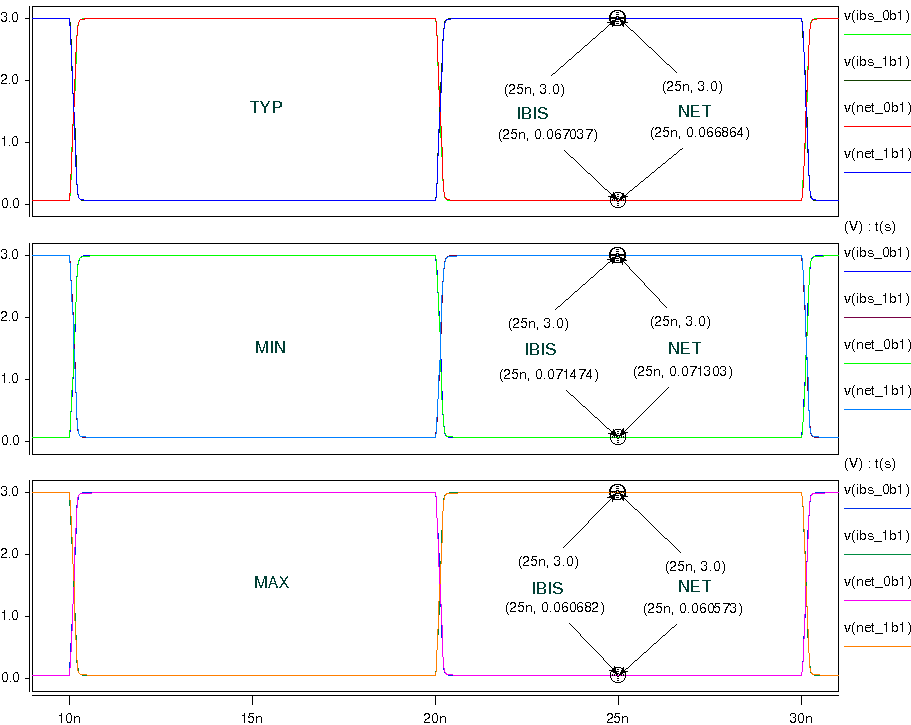
**SDA\_C**

**6.0V**

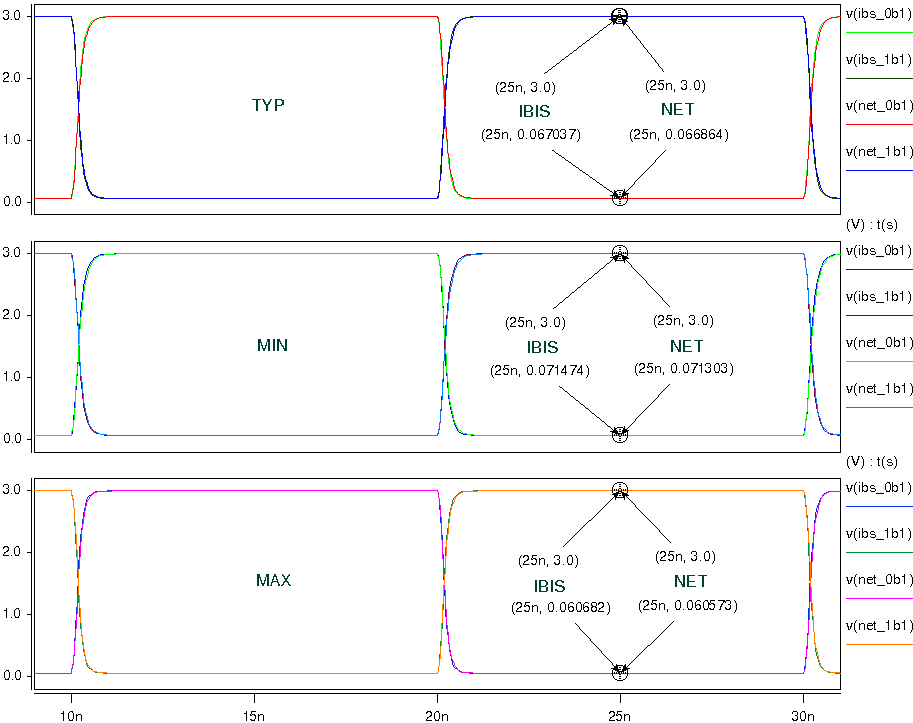
**SCL\_C**

**SDA\_C**

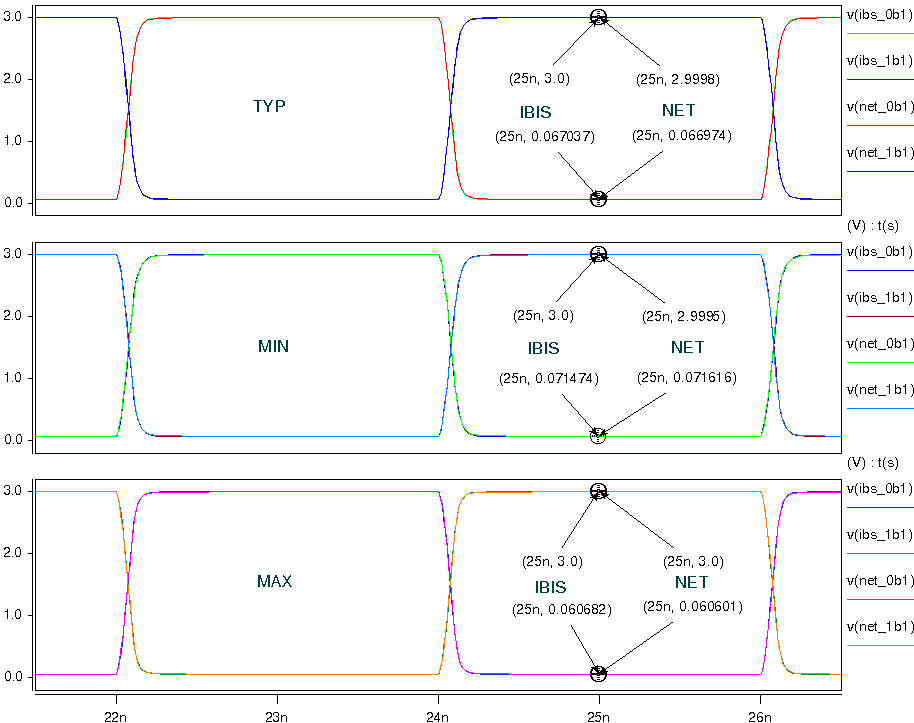
1. The frequency of signal is **50MHz**:
2. Add **10pF** pull-down capacitance to the output;



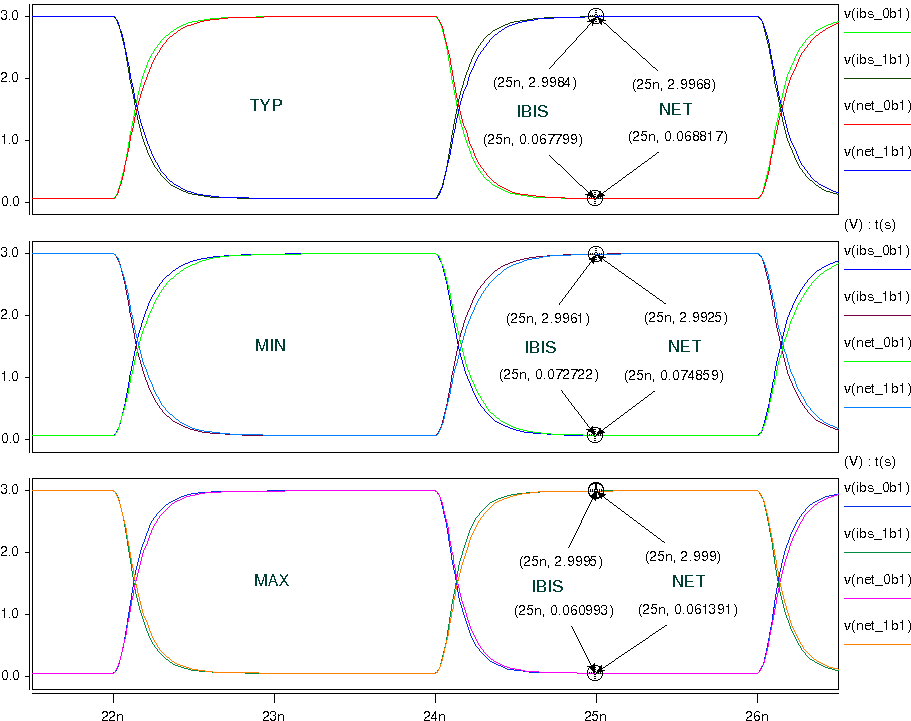
1. Add **50pF** pull-down capacitance to the output;



1. The frequency of signal is **250MHz**:
2. Add **10pF** pull-down capacitance to the output;



1. Add **50pF** pull-down capacitance to the output;



1. Add **50Ω** resistor between the INPUT and IC’s PIN:

PI3LVD512

**OUTP**

**SCL\_C**

**SDA\_C**

**OUTN**

**SCL\_C**

**SDA\_C**

200Ω

**SCL\_C**

**SDA\_C**

200Ω

**SCL\_C**

**SDA\_C**

50Ω

**SCL\_C**

**SDA\_C**

A0

**SCL\_C**

**SDA\_C**

C

**SCL\_C**

**SDA\_C**

C

**SCL\_C**

**SDA\_C**

**Differential Signals**

**SCL\_C**

**SDA\_C**

50Ω

**SCL\_C**

**SDA\_C**

A1

**SCL\_C**

**SDA\_C**

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0B1

**SCL\_C**

**SDA\_C**

1B1

**SCL\_C**

**SDA\_C**

**INP**

**SCL\_C**

**SDA\_C**

**INN**

**SCL\_C**

**SDA\_C**

200Ω

**SCL\_C**

**SDA\_C**

200Ω

**SCL\_C**

**SDA\_C**

**6.0V**

**SCL\_C**

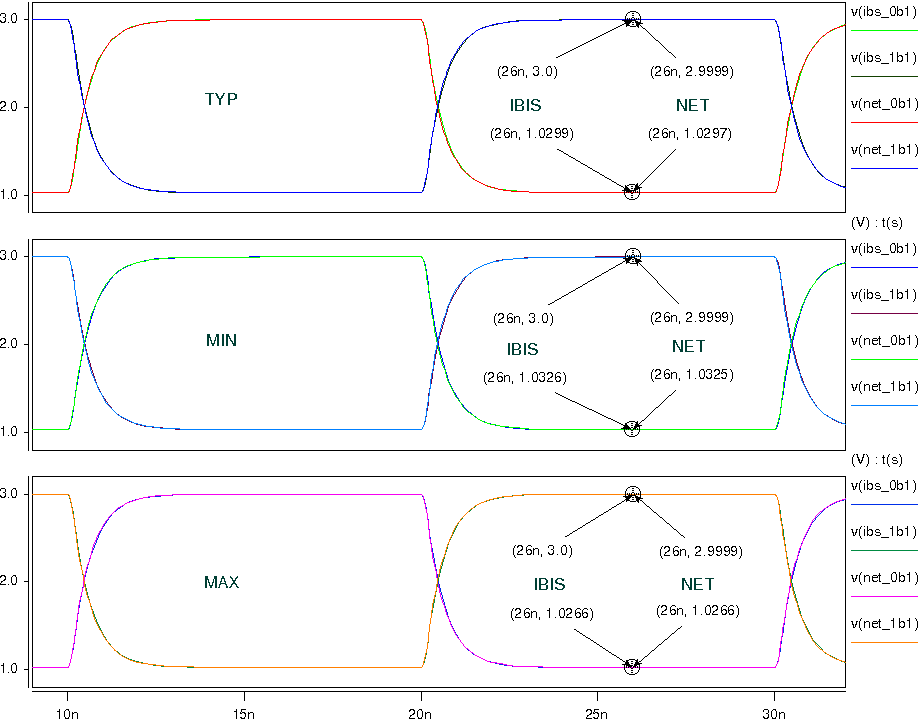
**SDA\_C**

**6.0V**

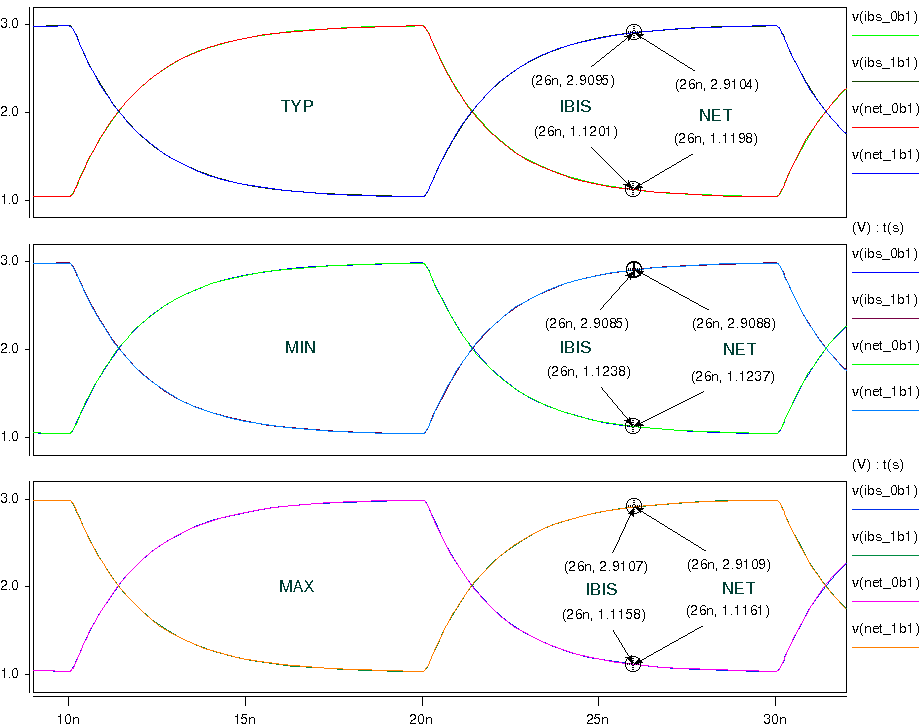
**SCL\_C**

**SDA\_C**

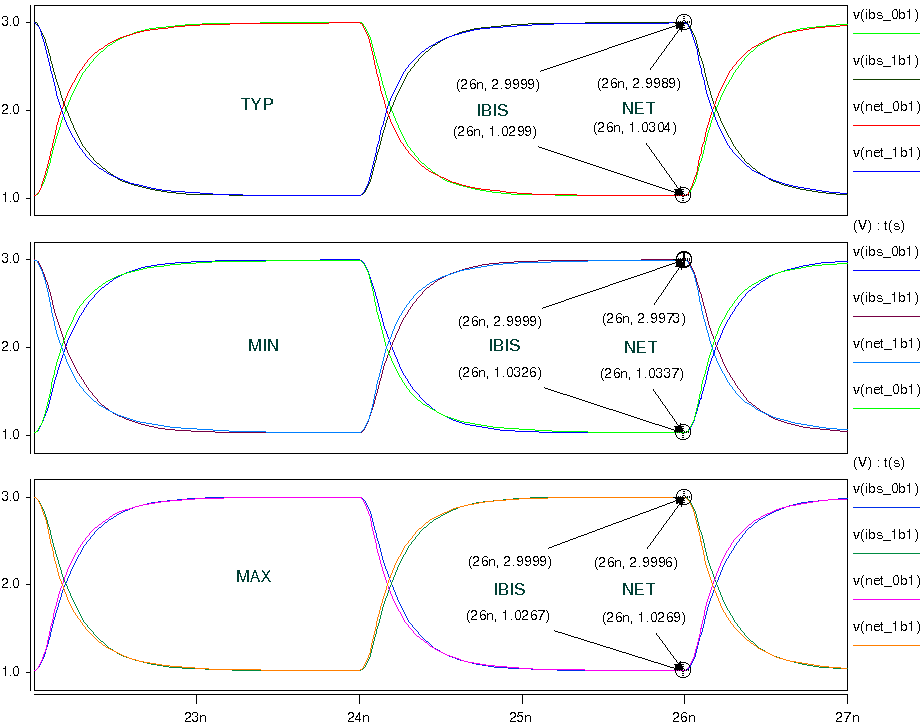
1. The frequency of signal is **50MHz**:
2. Add **10pF** pull-down capacitance to the output;



1. Add **50pF** pull-down capacitance to the output;



1. The frequency of signal is **250MHz**:
2. **Without** pull-down capacitance to the output;



1. Add **10pF** pull-down capacitance to the output;

