**Verification of PI3L500-A IBIS model**

1. **Introduction:**

To verify the correlation between the ibis model and hspice model, we need to do some simulations with following conditions:

PI3L500-A

**OUT0**

**SCL\_C**

**SDA\_C**

**OUT1**

**SCL\_C**

**SDA\_C**

R

**SCL\_C**

**SDA\_C**

R

**SCL\_C**

**SDA\_C**

A0

**SCL\_C**

**SDA\_C**

C

**SCL\_C**

**SDA\_C**

C

**SCL\_C**

**SDA\_C**

**Differential Signals**

**SCL\_C**

**SDA\_C**

**Output**

**SCL\_C**

**SDA\_C**

A1

**SCL\_C**

**SDA\_C**

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0B1

**SCL\_C**

**SDA\_C**

1B1

**SCL\_C**

**SDA\_C**

**IINN**

**SCL\_C**

**SDA\_C**

**INP**

**SCL\_C**

**SDA\_C**

R=50Ω

**SCL\_C**

**SDA\_C**

R=50Ω

**SCL\_C**

**SDA\_C**

1. The frequency of signal is **50MHz (100Mbps)**.

vinn a0 0 pulse ( 3 0 0 .1n .1n 9.9n 20n)

vinp a1 0 pulse ( 0 3 0 .1n .1n 9.9n 20n)

Adding **50Ω** resistor between the signal and INPUT, with **10pF** pull-down capacitance and **500Ω** pull-down resistor to the OUTPUT:

1. without package
2. with package
3. The frequency of signal is **250MHz (500Mbps)**.

vinn a0 0 pulse ( 3 0 0 .1n .1n 1.9n 4n)

vinp a1 0 pulse ( 0 3 0 .1n .1n 1.9n 4n)

Adding **50Ω** resistor between the signal and INPUT, with **2pF** pull-down capacitance and **50Ω** pull-down resistor to the OUTPUT:

1. without package
2. with package
3. **Conclusion:**
4. For SWITCH1, the simulation results of IBIS model can match quite well with the HSPICE model at different load conditions.

1. **Simulation Result:**
2. The frequency of signal is **50MHz (100Mbps)**.

With **10pF** pull-down capacitance and **500Ω** pull-down resistor to the OUTPUT:

1. without package



1. with package



1. The frequency of signal is **250MHz (500Mbps)**.

With **2pF** pull-down capacitance and **50Ω** pull-down resistor to the OUTPUT:

1. without package



1. with package

