KEYSIGHT TECHNOLOGIES

HDMI Test Report

Overall Result: PASS

Test Configuration Details	
Device Description	
Device ID	Transmitter
Fixture Type	Other
Probe Connection	4 Probes
Probe Head Type	N5444A
Lane Connection	1 Data Lane
HDMI Specification	2.0
HDMI Test Type	TMDS Physical Layer Tests
Test Session Details	
Infiniium SW Version	05.60.00603
Infiniium Model Number	DSOX92504A
Infiniium Serial Number	MY54410104
Application SW Version	2.11
Debug Mode Used	No
Probe (Channel 1)	Model: N2801A Serial: US54094067 Head: N5444A Atten: Calibrated (9 AUG 2016 14:10:30), Using Cal Atten (5.6226E+000) Skew: Calibrated (9 AUG 2016 14:11:12), Using Cal Skew
Probe (Channel 2)	Model: N2801A Serial: US54094054 Head: N5444A Atten: Calibrated (9 AUG 2016 14:15:19), Using Cal Atten (5.4285E+000) Skew: Calibrated (9 AUG 2016 14:16:00), Using Cal Skew
Probe (Channel 3)	Model: N2801A Serial: US54094059 Head: N5444A Atten: Calibrated (9 AUG 2016 14:19:22), Using Cal Atten (5.6325E+000) Skew: Calibrated (9 AUG 2016 14:20:11), Using Cal Skew
Probe (Channel 4)	Model: N2801A Serial: US54094057 Head: N5444A Atten: Calibrated (9 AUG 2016 15:17:37), Using Cal Atten (5.5290E+000) Skew: Calibrated (9 AUG 2016 15:18:23), Using Cal Skew
Last Test Date	2016-08-26 11:39:50 UTC +08:00

Summary of Results

Test Statistics	
Failed	0
Passed	19
Total	19

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	7-9: Clock Jitter	119 mTbit	52.4 %	VALUE <= 250 mTbit
✓	0	1	7-4: Clock Rise Time	122.677 ps	63.6 %	VALUE >= 75.000 ps
✓	0	1	7-4: Clock Fall Time	126.466 ps	68.6 %	VALUE >= 75.000 ps
✓	0	1	7-8: Clock Duty Cycle(Minimum)	50.080	25.2 %	>=40%
✓	0	1	7-8: Clock Duty Cycle(Maximum)	50.740	15.4 %	<=60%
✓	0	1	7-10: D0 Mask Test	0.000	50.0 %	No Mask Failures
✓	0	1	7-10: D0 Data Jitter	150 m	50.0 %	<=0.3Tbit
✓	0	1	7-4: D0 Rise Time	117.192 ps	56.3 %	VALUE >= 75.000 ps
✓	0	1	7-4: D0 Fall Time	115.835 ps	54.4 %	VALUE >= 75.000 ps
✓	0	1	7-2: VL Clock +	2.739 V	46.3 %	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	7-2: VL Clock -	2.728 V	42.7 %	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	7-7: Intra-Pair Skew - Clock	23 mTbit	42.3 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	1	7-2: VL D0+	2.763 V	45.7 %	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	7-2: VL D0-	2.751 V	49.7 %	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	7-7: Intra-Pair Skew - Data Lane 0	29 mTbit	40.3 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	1	7-3: Voff Clock +	-4 mV	30.0 %	-10 mV <= VALUE <= 10 mV
✓	0	1	7-3: Voff Clock -	-5 mV	25.0 %	-10 mV <= VALUE <= 10 mV
✓	0	1	7-3: Voff D0+	-5 mV	25.0 %	-10 mV <= VALUE <= 10 mV
✓	0	1	7-3: Voff D0-	-5 mV	25.0 %	-10 mV <= VALUE <= 10 mV

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✓ 7-9: Clock Jitter

Reference: Test ID 7-9

Test Summary: Pass Test Description: 2 Channels Connection Model: TMDS differential clock jitter must not exceed 0.25*Tbit, relative to the ideal Recovery Clock. For compliance, the DUT should output 27MHz(or 25MHz), 74.25MHz, 148.5MHz, and 222.75MHz for testing.

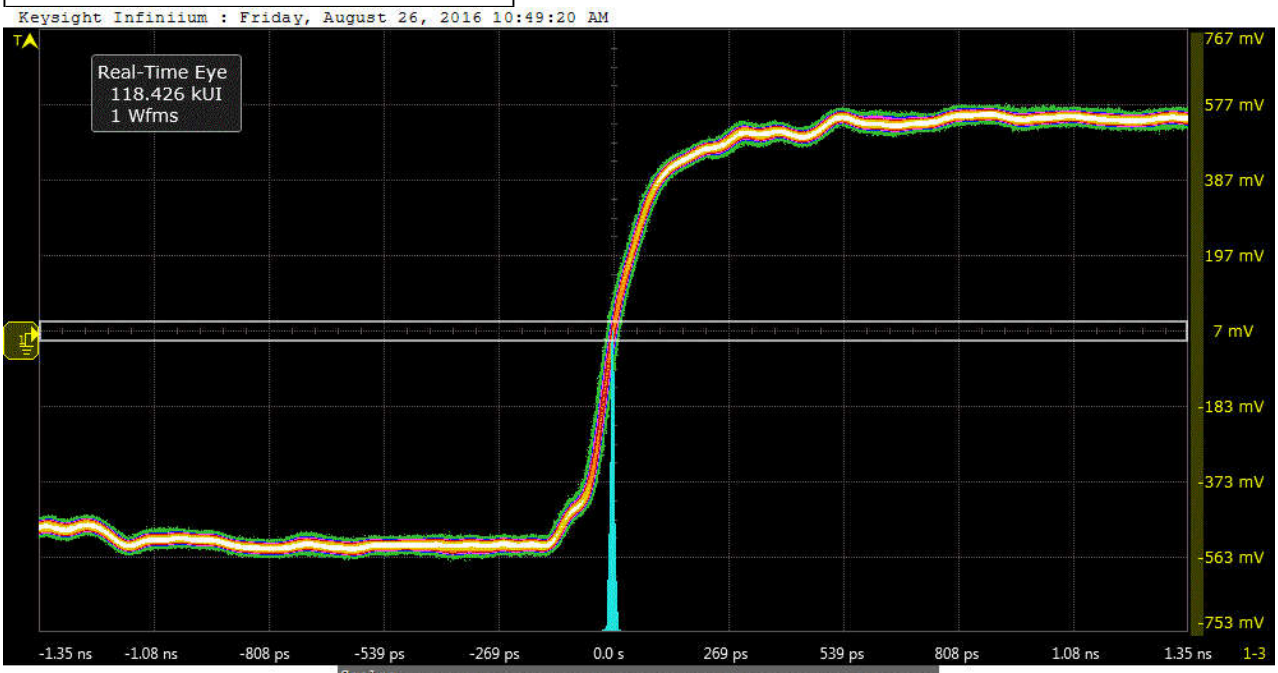
Pass Limits: <= 250 mTbit **Clock Jitter** 119 mTbit

Result Details

HDMIAutomationConfig	Timing 100	**Test Frequency(MHz)**	297.129	**Tbit(ps)**	336.555	**Clock Jitter(ps)**	39.980
# Samples	16.000000000 M	**# Edges**	118.426000 k	**Acquisition Bandwidth (GHz)**	13.000		

Trial 1

Trial 1: Clock Jitter



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7-4: Clock Rise Time

Reference: Test ID 7-4

Test Summary: Pass Test Description: 2 Channels Connection Model: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

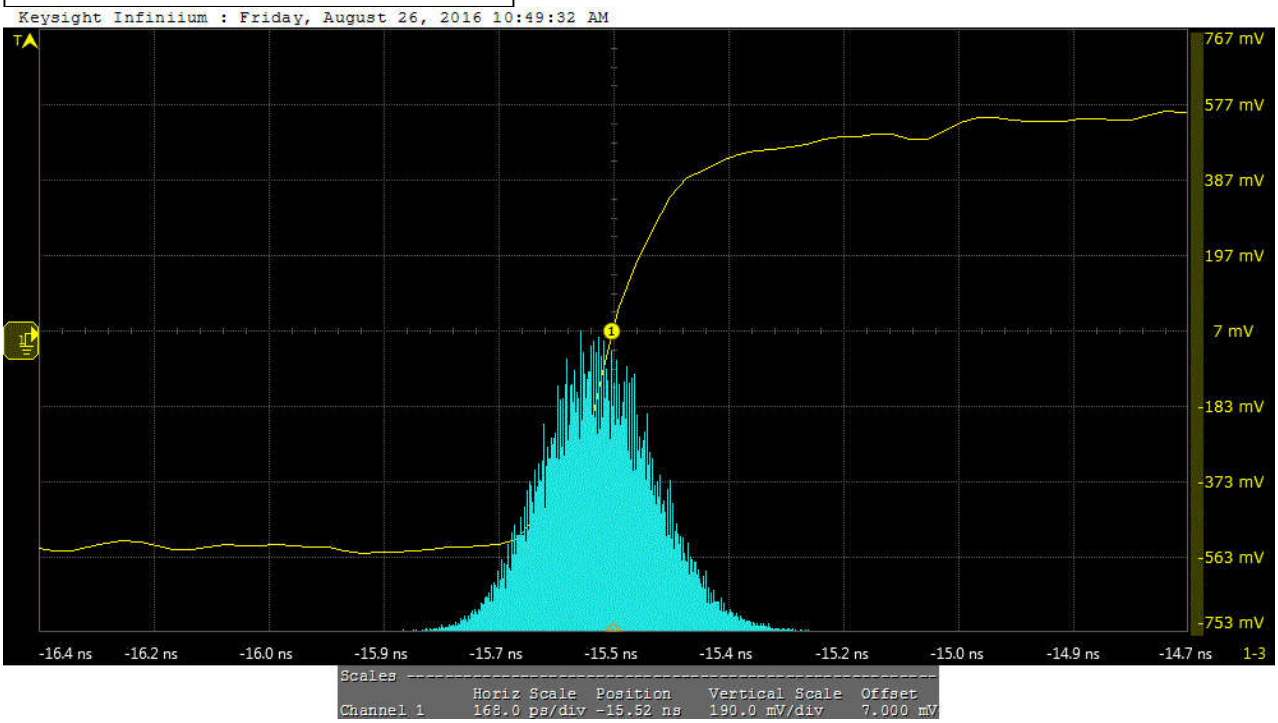
Pass Limits:	>= 75.000 ps	Raw Clock Transition Time	122.677 ps

Result Details

HDMIAutomationConfig	Timing 100	Test Frequency(MHz)	297.129	Upper Threshold(%)	80.000
Lower Threshold(%)	20.000	# Edges	118.798000 k	Acquisition Bandwidth (GHz)	13.000

Trial 1

Trial 1: Raw Clock Transition Time



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✓7-4: Clock Fall Time

Reference: Test ID 7-4

Test Summary: Pass Test Description: 2 Channels Connection Model: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

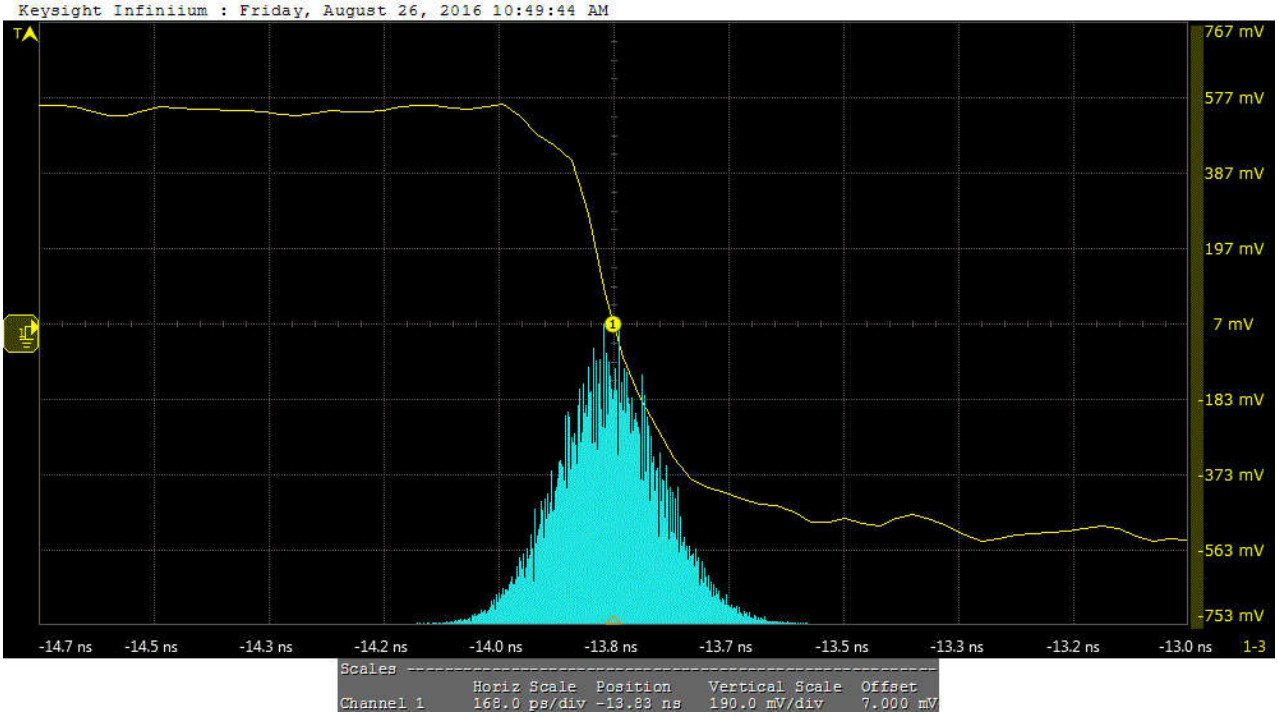
Pass Limits:	>= 75.000 ps	Raw Clock Transition Time	126.466 ps

Result Details

HDMIAutomationConfig	Timing 100	Test Frequency(MHz)	297.129	Upper Threshold(%)	80.000
Lower Threshold(%)	20.000	# Edges	118.799000 k	Acquisition Bandwidth (GHz)	13.000

Trial 1

Trial 1: Raw Clock Transition Time



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✓7-8: Clock Duty Cycle(Minimum)

Reference: Test ID 7-8

Test Summary: Pass Test Description: 2 Channels Connection Model: Clock duty cycle must be at least 40% and not more than 60%.The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

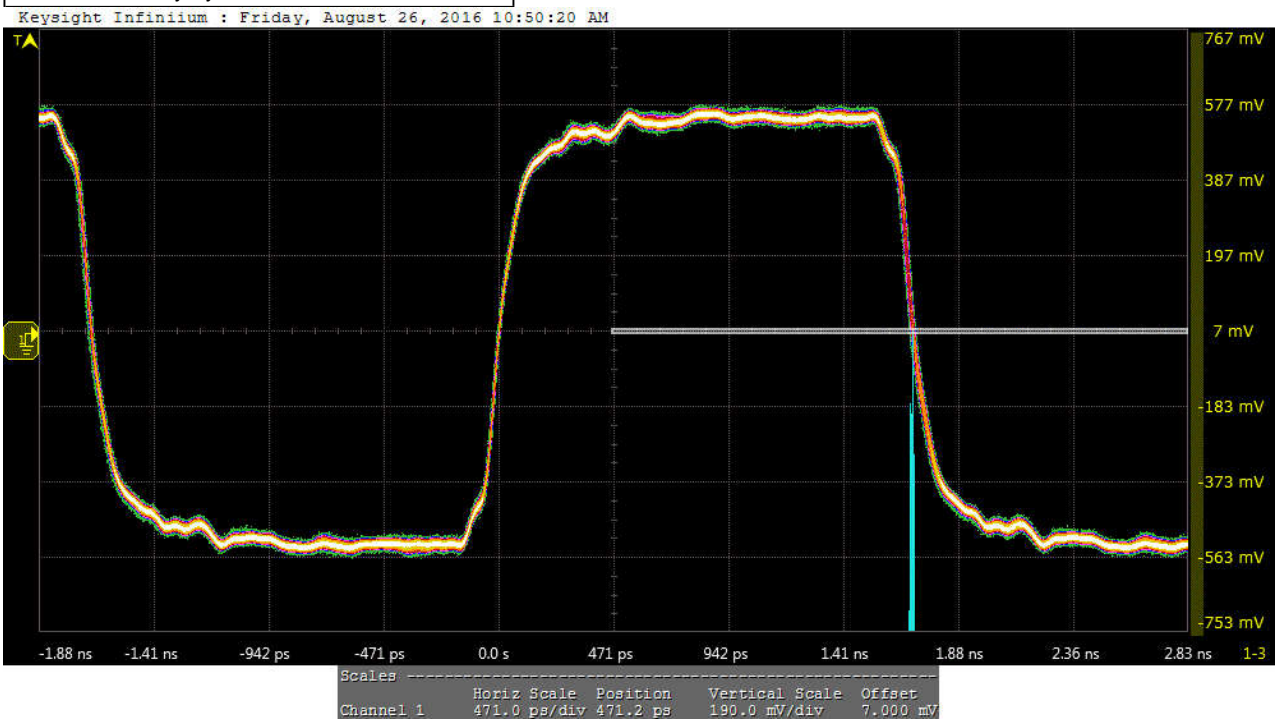
Pass Limits:	>=40%	Clock Duty Cycle Minimum	50.080

Result Details

HDMIAutomationConfig	Timing 100	Test Frequency(MHz)	297.129	# Edges	118.426000 k	TdutyMIN(ns)	1.685

Trial 1

Trial 1: Clock Duty Cycle Minimum



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7-8: Clock Duty Cycle(Maximum)

Reference: Test ID 7-8

Test Summary: Pass Test Description: 2 Channels Connection Model: Clock duty cycle must be at least 40% and not more than 60%.The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

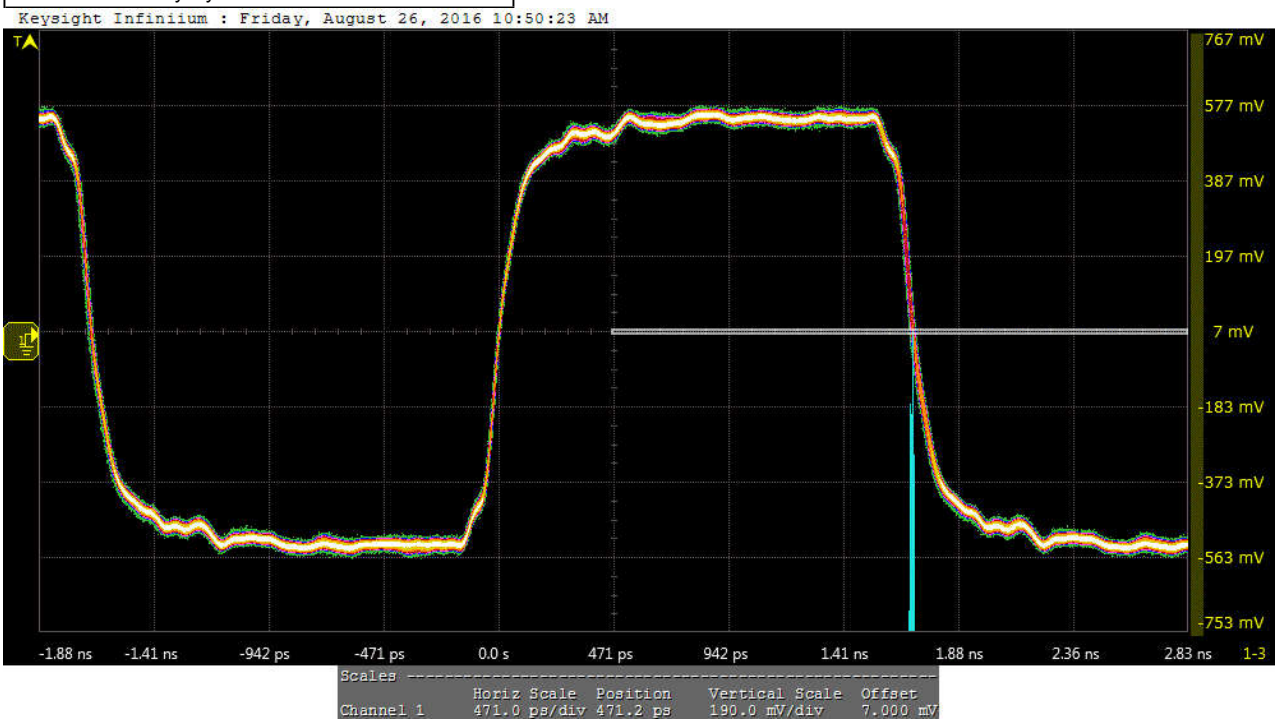
Pass Limits:	<=60%	Clock Duty Cycle Maximum	50.740

Result Details

HDMIAutomationConfig	Timing 100	Test Frequency(MHz)	297.129	# Edges	10.000000 k	TdutyMAX(ns)	1.708

Trial 1

Trial 1: Clock Duty Cycle Maximum



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7-10: D0 Mask Test

Reference: Test ID 7-10

Test Summary: Pass Test Description: For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.

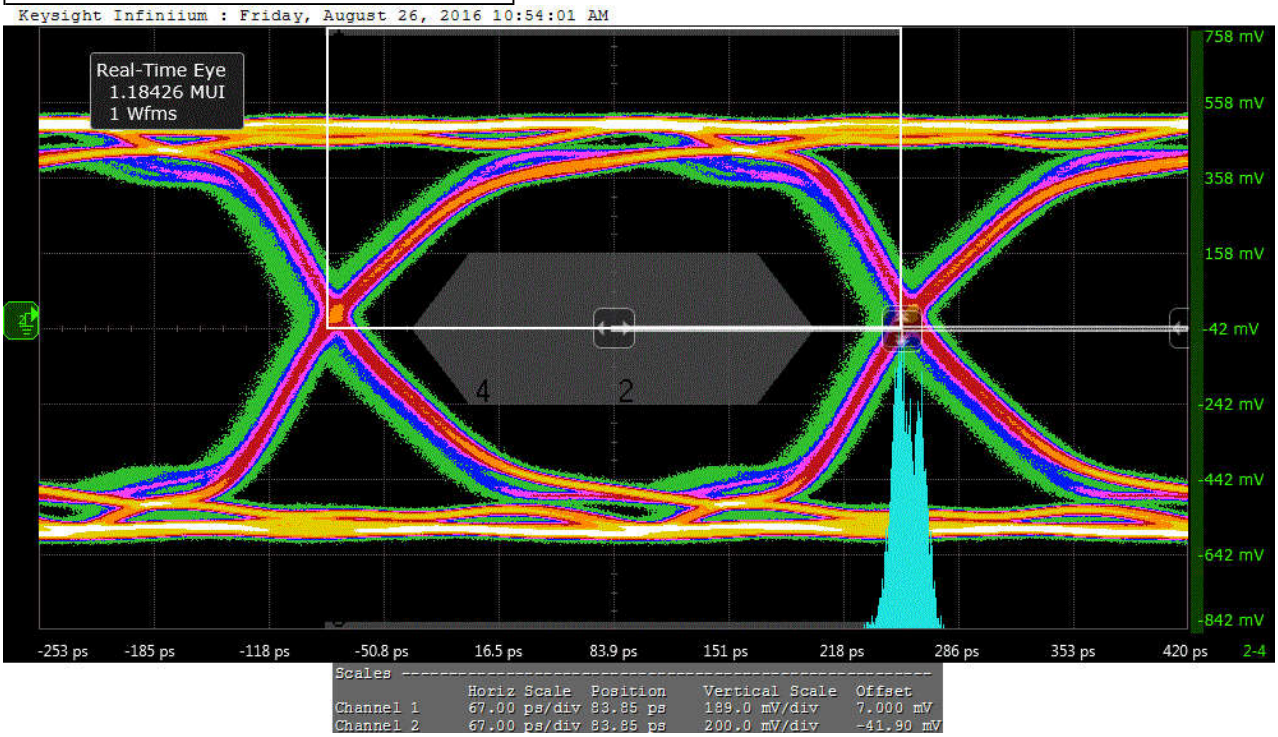
Pass Limits: No Mask Failures | **Total # failures** 0.000

Result Details

HDMIAutomationConfig	Timing 100	**Eye Width(ps)**	286.590	**Eye Height(mV)**	809.000	**Data Lane A**	D0
Test Frequency(MHz)	297.129	**Mask Moved(ps)**	0.000	**# Acquisitions Point**	16.000000000 M	**Tbit(ps)**	336.702
RightJitterData(Tbit)	150 m	**LeftJitterData(Tbit)**	148 m	**RightJitterData(ps)**	50.480	**LeftJitterData(ps)**	49.960
Maximum Margin	NA	**Maximum Margin (Vertical)**	NA	**Differential Swing Voltage, VH(V)**	499 m		
Differential Swing Voltage,VL (V)	-575 m	**Differential Swing Voltage(V)**	1.074				
Acquisition Bandwidth (GHz)	13.000						

Trial 1

Trial 1: Total # failures



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7-10: D0 Data Jitter

Reference: Test ID 7-10

Test Summary: Pass Test Description: For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.

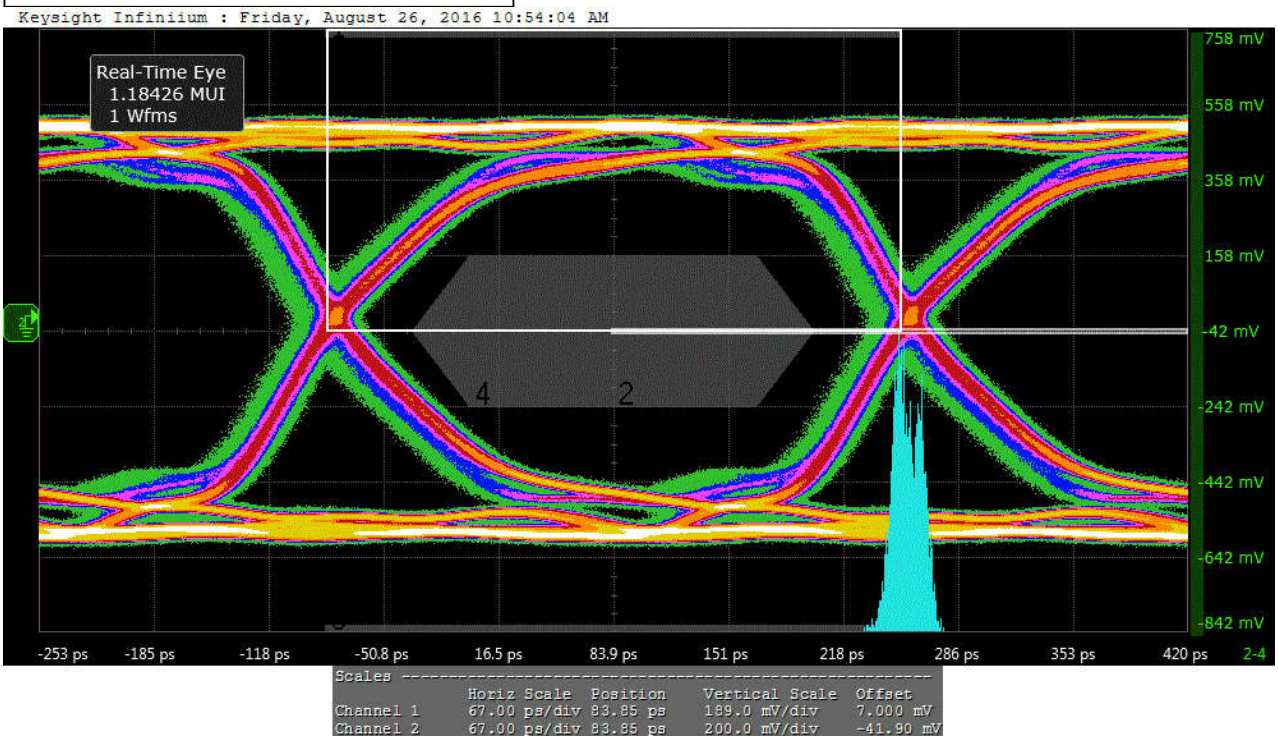
Pass Limits: <=0.3Tbit | **TbitCheck** 150 m

Result Details

HDMIAutomationConfig	Timing 100

Trial 1

Trial 1: TbitCheck



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7-4: D0 Rise Time

Reference: Test ID 7-4

Test Summary: Pass Test Description: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

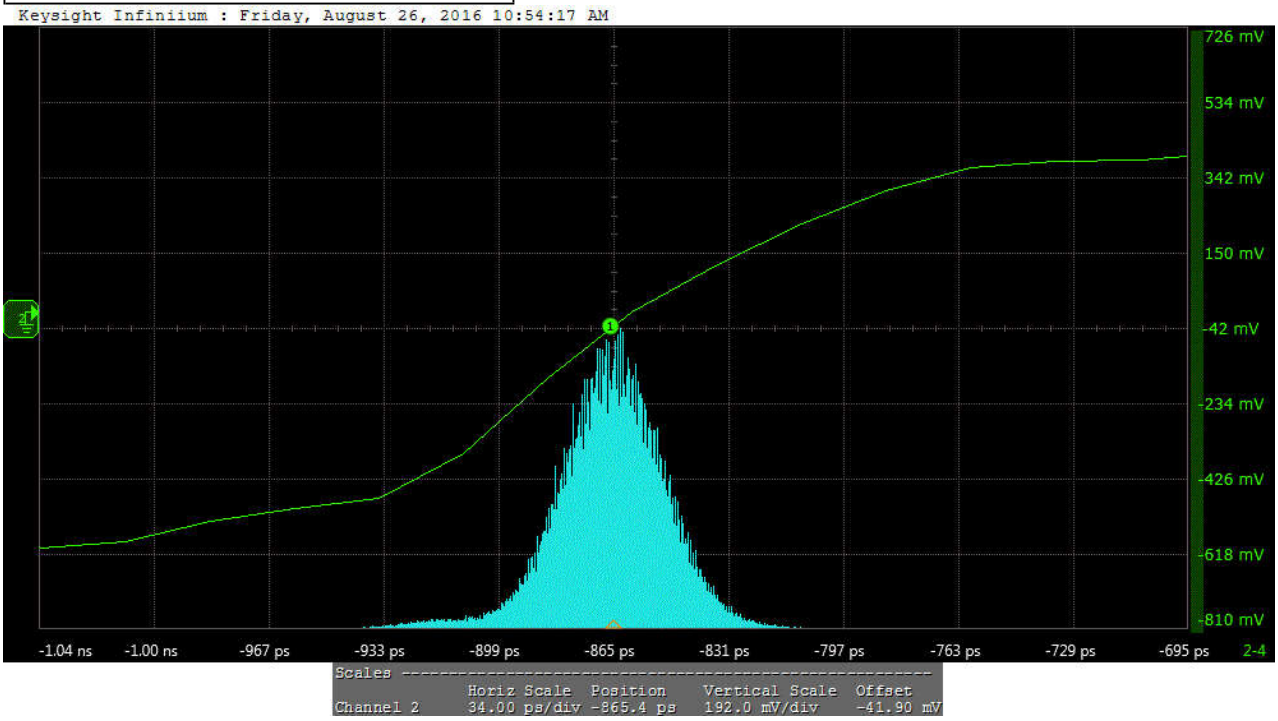
Pass Limits: >= 75.000 ps **Transition Time** 117.192 ps

Result Details

HDMIAutomationConfig	Timing 100	**Test Frequency(MHz)**	297.129	**Data Lane A**	D0	**Upper Threshold(%)**	80.000
Lower Threshold(%)	20.000	**#Edge**	142.600000 k	**Acquisition Bandwidth (GHz)**	13.000		

Trial 1

Trial 1: Transition Time



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7-4: D0 Fall Time

Reference: Test ID 7-4

Test Summary: Pass Test Description: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

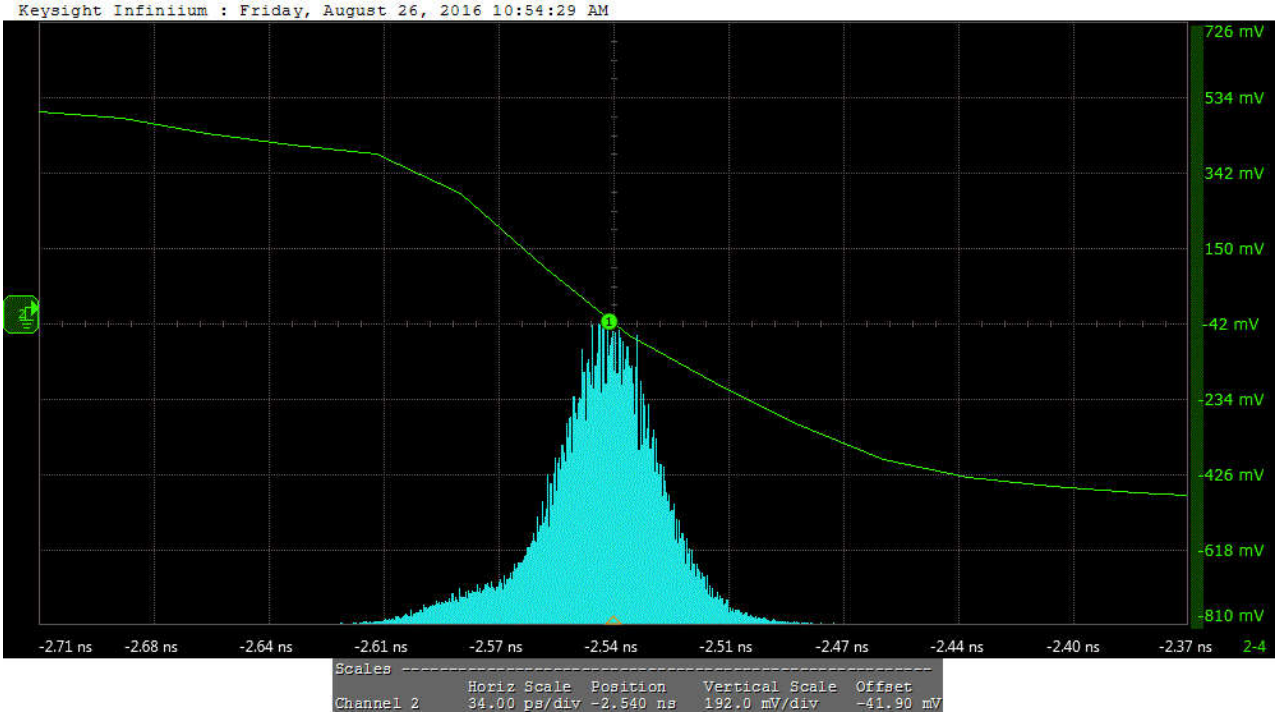
Pass Limits: >= 75.000 ps | **Transition Time** 115.835 ps

Result Details

HDMIAutomationConfig	Timing 100	**Test Frequency(MHz)**	297.129	**Data Lane A**	D0	**Upper Threshold(%)**	80.000
Lower Threshold(%)	20.000	**#Edge**	142.600000 k	**Acquisition Bandwidth (GHz)**	13.000		

Trial 1

Trial 1: Transition Time



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7-2: VL Clock +

Reference: Test ID 7-2

Test Summary: Pass Test Description: The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.

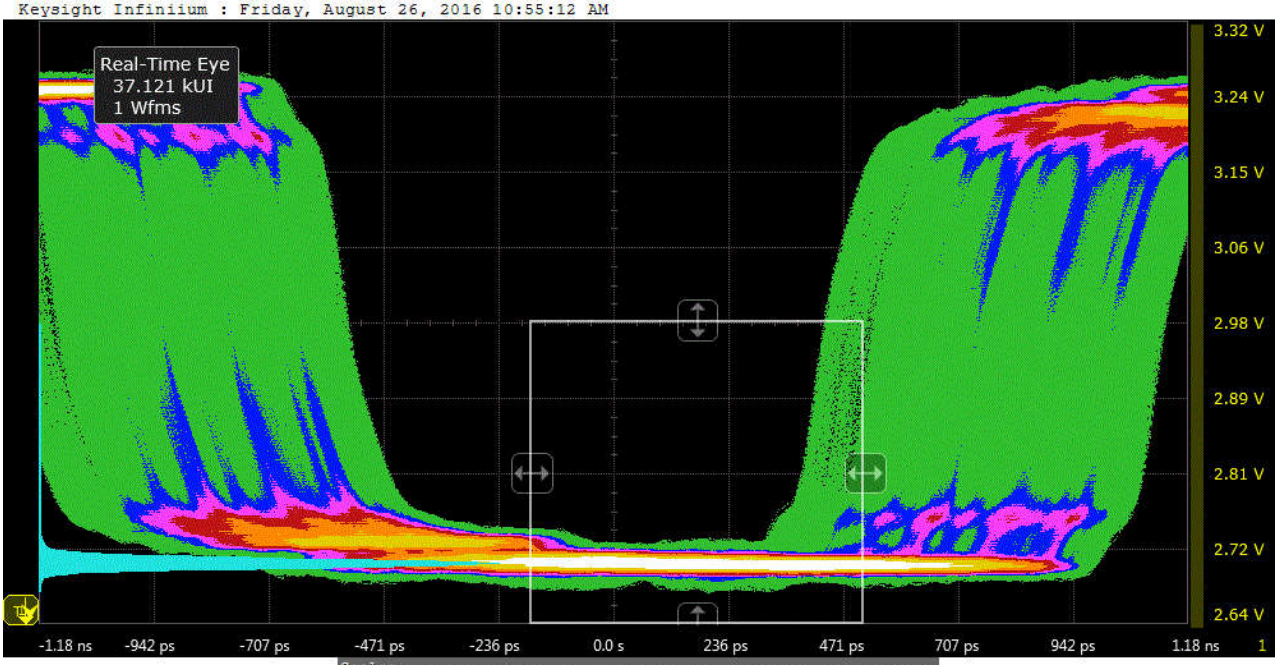
Pass Limits: [LowerLimit V to 2.900 V] | **VL** 2.739 V

Result Details

HDMIAutomationConfig	Timing 100	**Test Frequency**	297.129 MHz	**# Edges**	37.121000 k	**VH**	3.274 V
VL	(See image)	**DUT supports clock rates > 165MHz**	true	**PassLimit Min (LowerLimit)**	2.600 V		

Trial 1

Trial 1: VL



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✓7-2: VL Clock

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Reference: Test ID 7-2

Test Summary: Pass Test Description: The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.

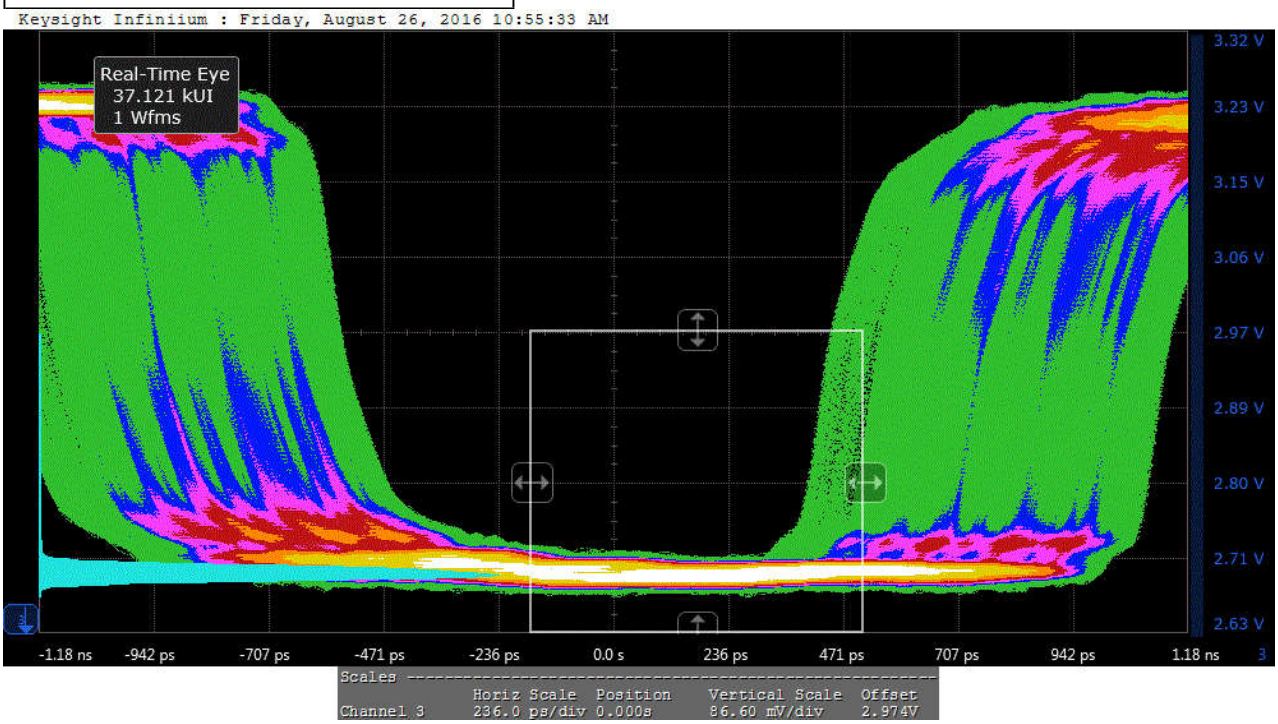
Pass Limits: [LowerLimit V to 2.900 V] **VL** 2.728 V

Result Details

HDMIAutomationConfig	Timing 100	**Test Frequency**	297.129 MHz	**# Edges**	37.121000 k	**VH**	3.270 V
VL	(See image)	**DUT supports clock rates > 165MHz**	true	**PassLimit Min (LowerLimit)**	2.600 V		

Trial 1

Trial 1: VL



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7-7: Intra-Pair Skew - Clock

Reference: Test ID 7-7

Test Summary: Pass Test Description: Frequency > 165 MHz: Intra-Pair Skew must not exceed 0.15*Tbit. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

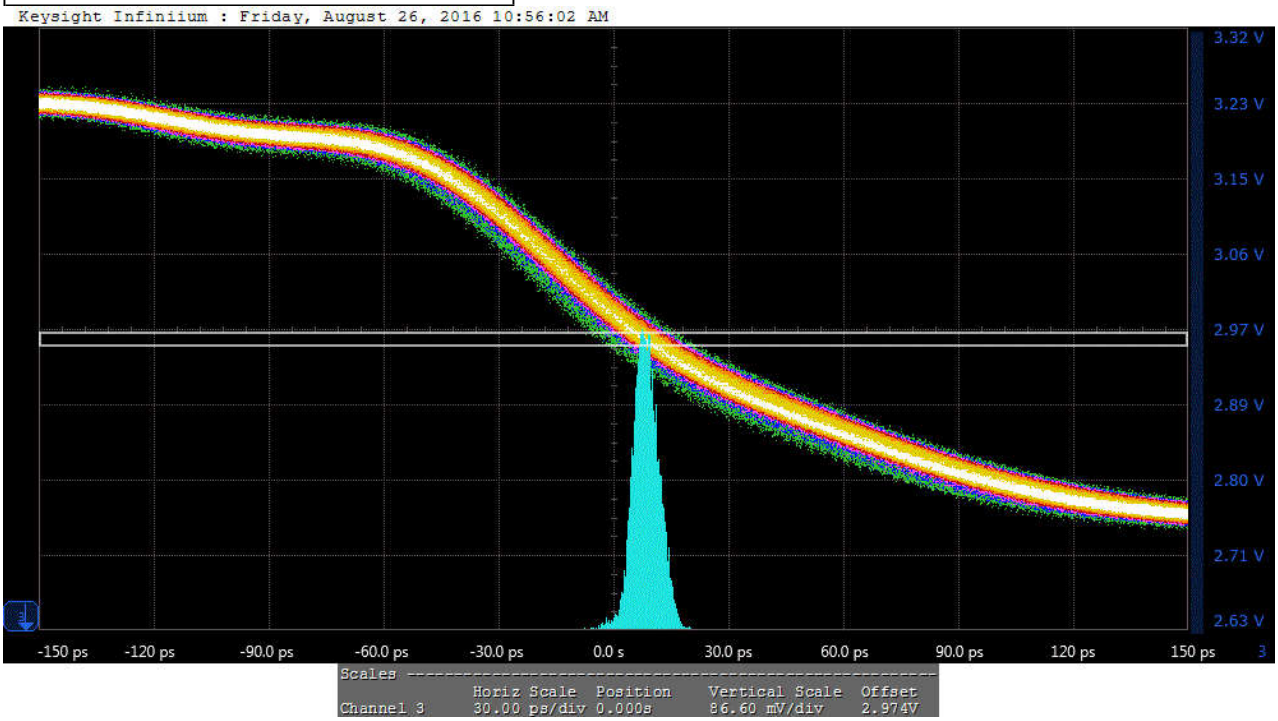
Pass Limits:	[-150 mTbit to 150 mTbit]	Clock Intra-Pair Skew	23 mTbit

Result Details

HDMIAutomationConfig	Timing 100	Max skew (ps)	20.390	Min skew (ps)	-7.270	Clk+ threshold (V)	2.976
Clk- threshold (V)	2.963	Acquisition Bandwidth (GHz)	13.000	Test Frequency(MHz)	297.129		
Clock Intra-Pair Skew(ps)	7.730						

Trial 1

Trial 1: Clock Intra-Pair Skew



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7-2: VL D0+

Reference: Test ID 7-2

Test Summary: Pass Test Description: The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.

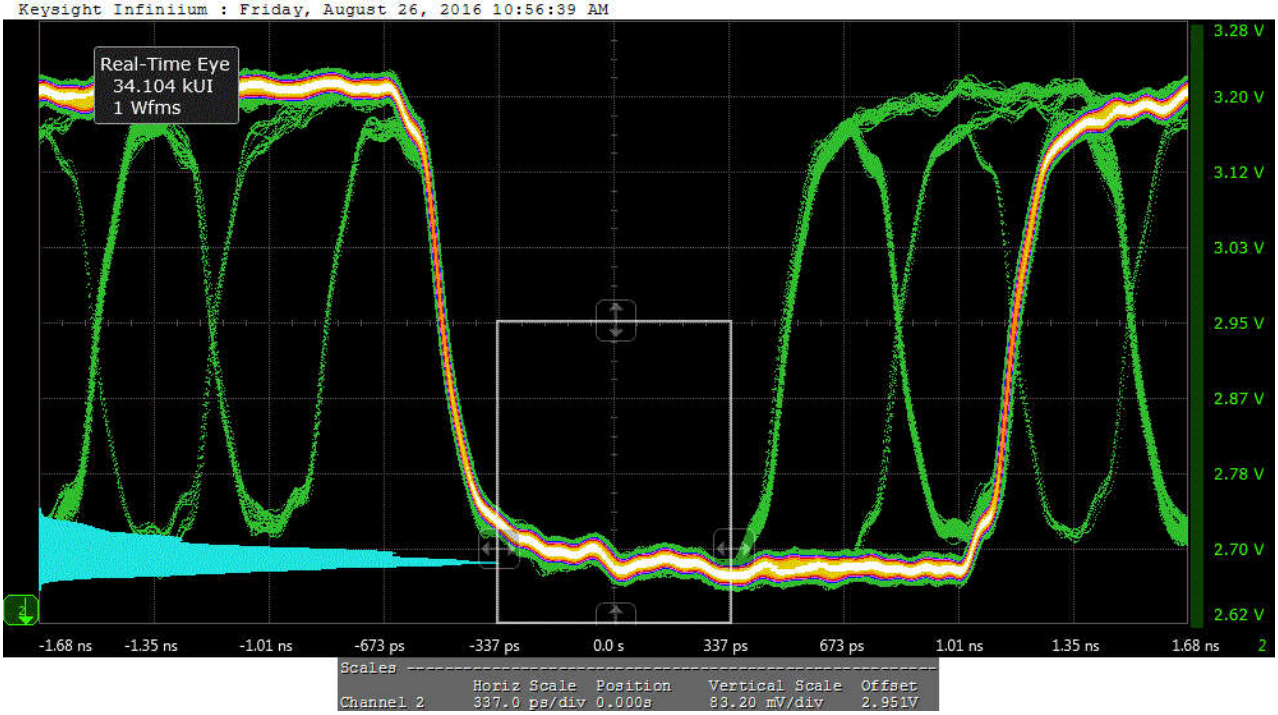
Pass Limits:	[LowerLimit V to 2.900 V]	VL	2.763 V

Result Details

HDMIAutomationConfig	Timing 100	Test Frequency	297.129 MHz	# Edges,VL	34.104000 k		
# Edges,VH	34.109000 k	VH	3.283 V	VL	(See image)	DUT supports clock rates > 165MHz	true
PassLimit Min (LowerLimit)	2.600 V						

Trial 1

Trial 1: VL



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7-2: VL
D0-

Reference: Test ID

Test Summary: Pass Test Description: The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.

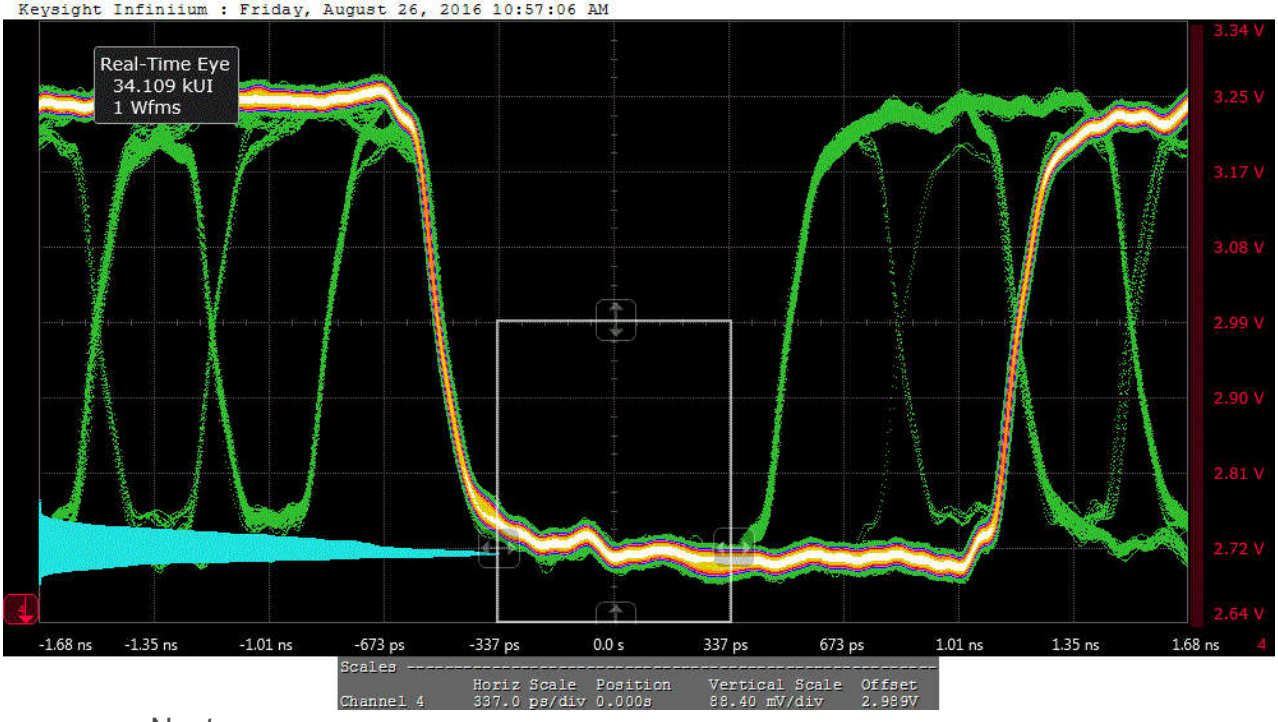
Pass Limits: [LowerLimit V to 2.900 V] **VL** 2.751 V

Result Details

HDMIAutomationConfig	Timing 100	**Test Frequency**	297.129 MHz	**# Edges,VL**	34.109000 k
# Edges,VH	34.104000 k	**VH**	3.278 V	**VL**	(See image)
DUT supports clock rates > 165MHz	true				
PassLimit Min (LowerLimit)	2.600 V				

Trial 1

Trial 1: VL



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7-7: Intra-Pair Skew - Data Lane 0

Reference: Test ID 7-7

Test Summary: Pass Test Description: Frequency > 165 MHz: Intra-Pair Skew must not exceed 0.15*Tbit. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

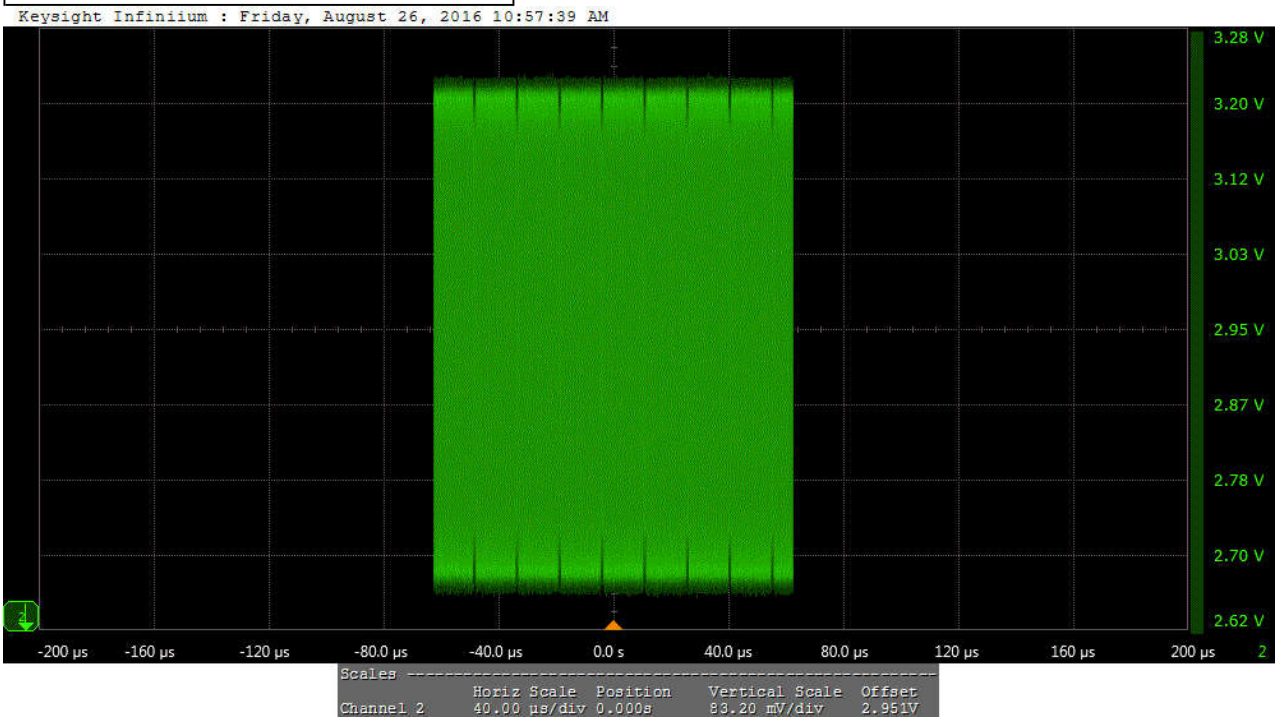
Pass Limits:	[-150 mTbit to 150 mTbit]	Data Intra-Pair Skew	29 mTbit

Result Details

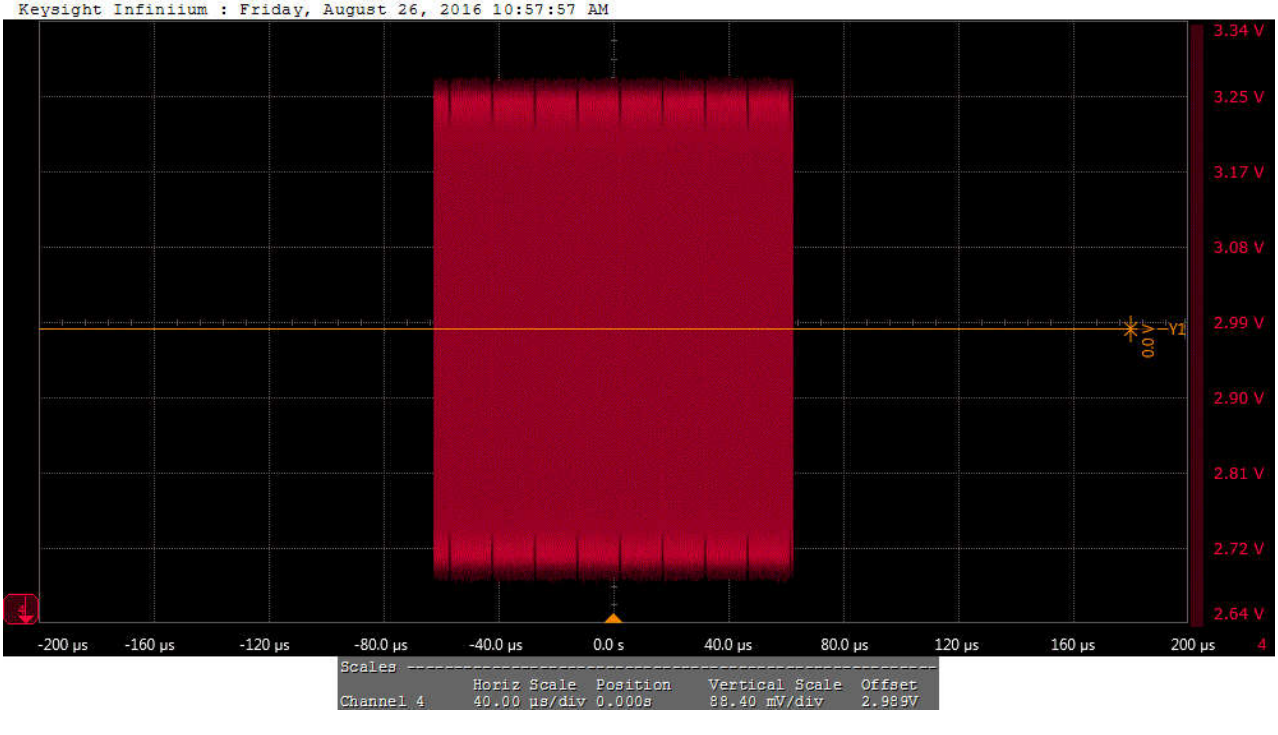
HDMIAutomationConfig	Timing 100	D+ Average Measurement Screenshot	(See image)
D- Average Measurement Screenshot	(See image)	Max skew (ps)	20.860
Min skew (ps)	4.450		
D+ threshold (V)	2.947	D- threshold (V)	2.981
Acquisition Bandwidth (GHz)	13.000		
Test Frequency(MHz)	297.129	Data Intra-Pair Skew(ps)	9.840

Trial 1

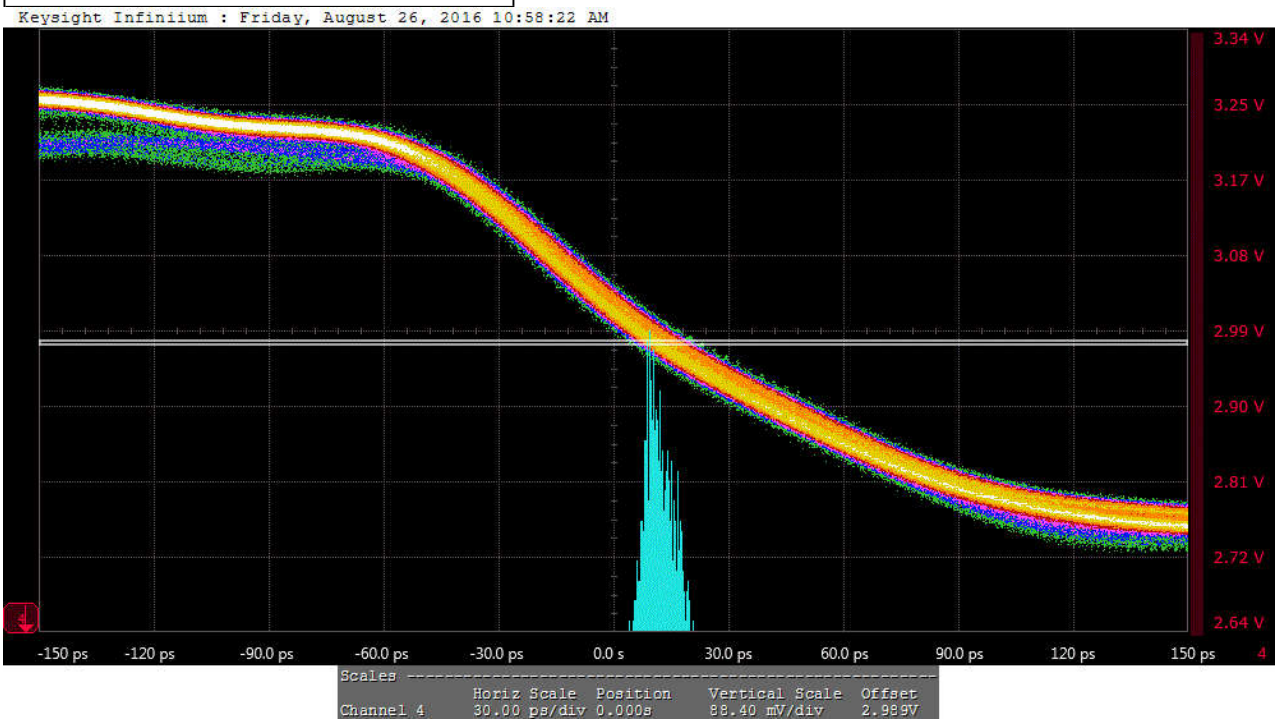
Trial 1: D+ Average Measurement Screenshot



Trial 1: D- Average Measurement Screenshot



Trial 1: Data Intra-Pair Skew



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✓7-3: Voff Clock +

Reference: Test ID 7-3

Test Summary: Pass Test Description: Confirm that a disabled TMDS link only allows leakage currents within specified limits.

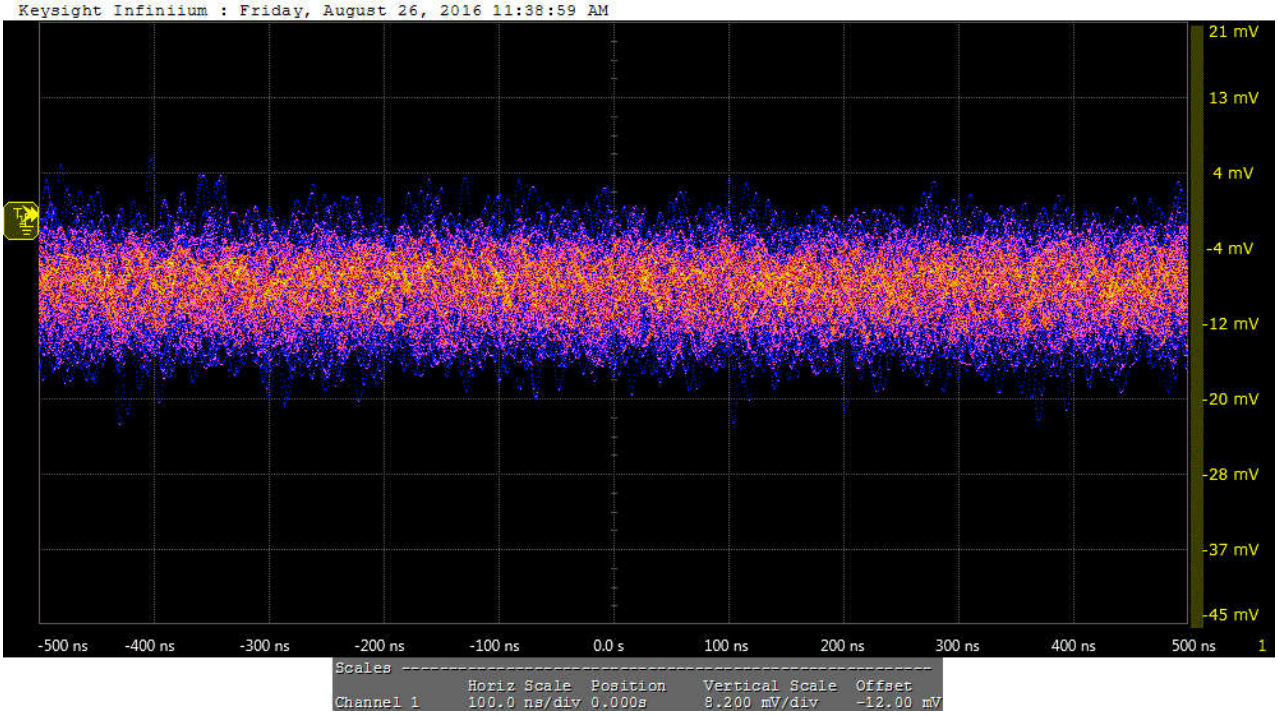
Pass Limits: [-10 mV to 10 mV] **Voff** -4 mV

Result Details

HDMIAutomationConfig Timing 100

Trial 1

Trial 1: Voff



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✓7-3: Voff Clock -

Reference: Test ID 7-3

Test Summary: Pass | Test Description: Confirm that a disabled TMDS link only allows leakage currents within specified limits.

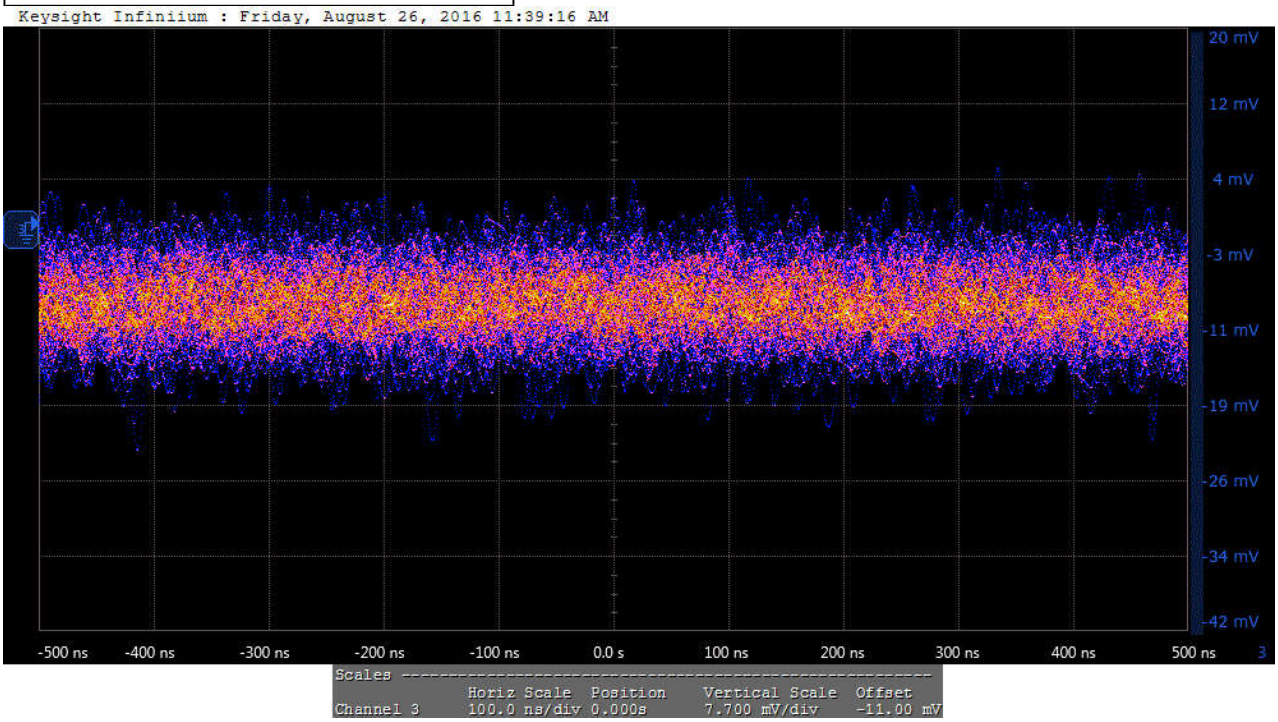
Pass Limits: [-10 mV to 10 mV] **Voff** -5 mV

Result Details

HDMIAutomationConfig Timing 100

Trial 1

Trial 1: Voff



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✓7-3: Voff D0+

Reference: Test ID 7-3

Test Summary: Pass | Test Description: Confirm that a disabled TMDS link only allows leakage currents within specified limits.

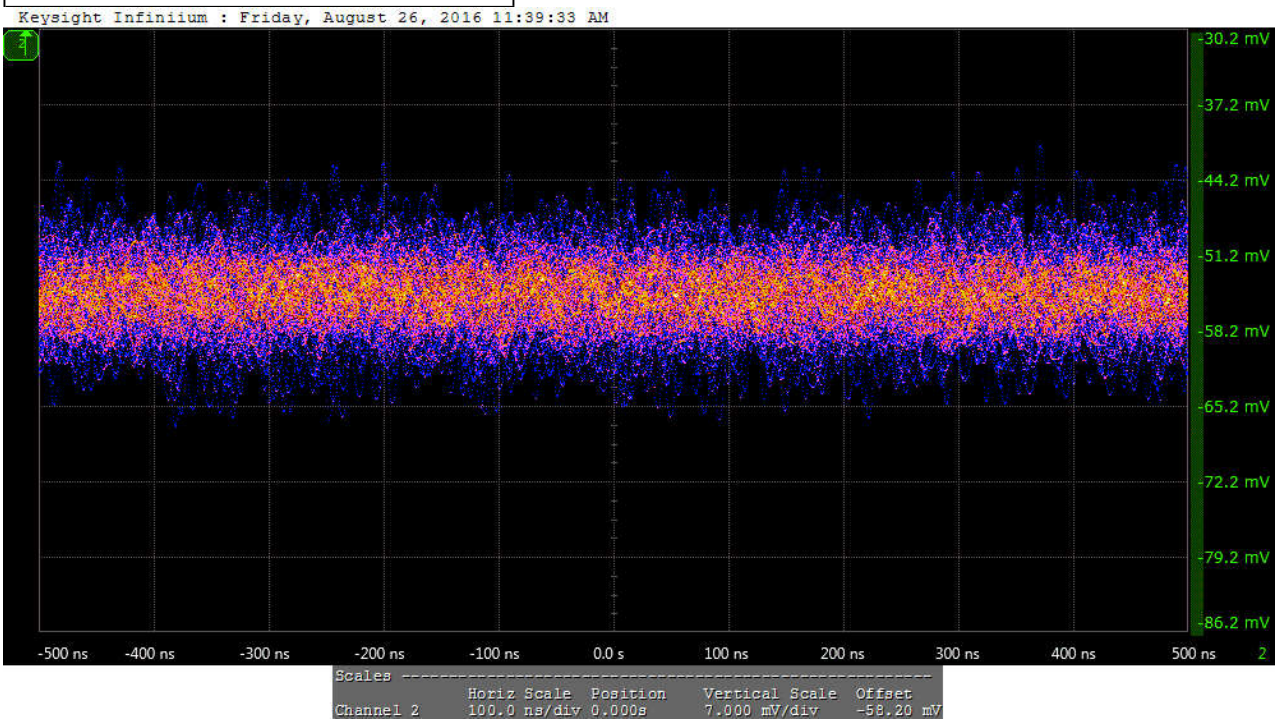
Pass Limits: [-10 mV to 10 mV] **Voff** -5 mV

Result Details

HDMIAutomationConfig Timing 100

Trial 1

Trial 1: Voff



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7-3: Voff

D0-

Reference: Test ID

Test Summary: Pass | Test Description: Confirm that a disabled TMDS link only allows leakage currents within specified limits.

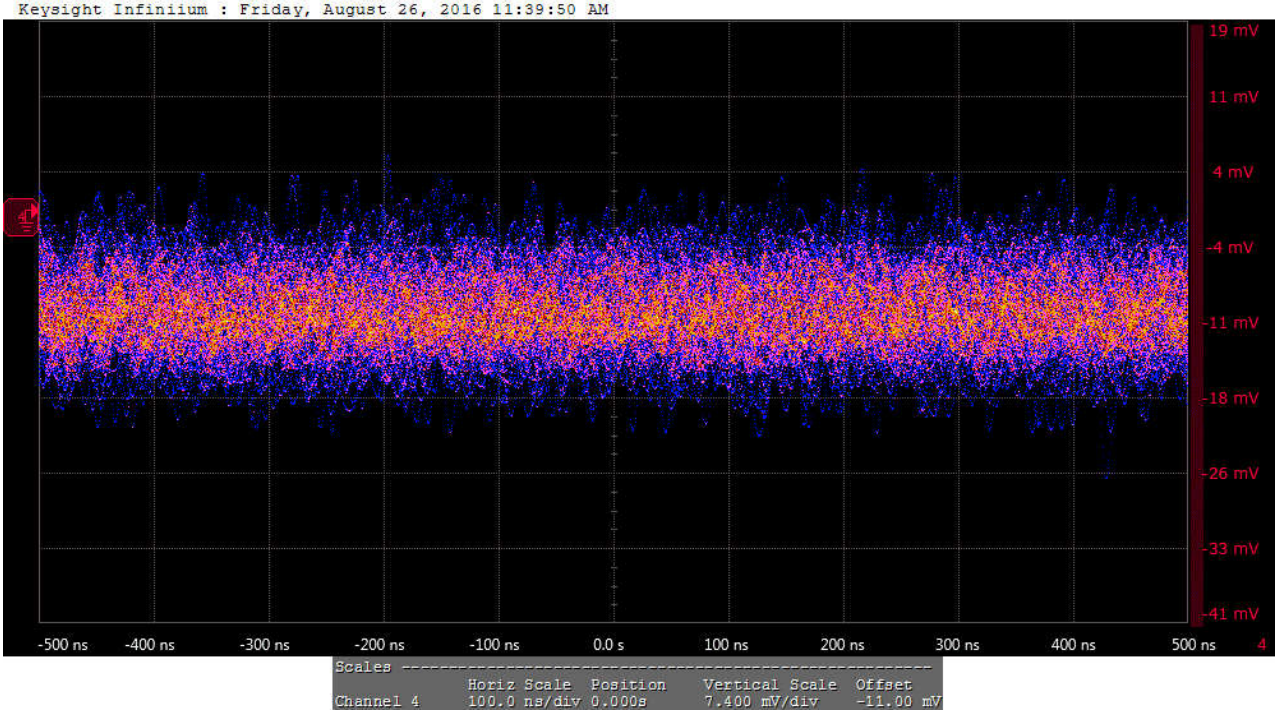
Pass Limits: [-10 mV to 10 mV] **Voff** -5 mV

Result Details

HDMIAutomationConfig Timing 100

Trial 1

Trial 1: Voff



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