PI3HDX1204B1
PI3HDX1204B1 HDMI Application Information

Table of Contents

1 Introduction 2
2 EVB Schematic 2
2.1 Source Application 2
2.1.1 ESD Protectors on Output TMDS 2
2.1.2 Extra Component for Rise/fall Time Control 3
2.1.3 Leakage Blockage for VOFF Test 3
2.2 Sink Application 4
2.2.1 ESD Protectors on Input TMDS 5
3 Layout Design Guideline 5
3.1 AC Coupling Capacitor 5
3.2 Output Trace Length 5
3.3 Differential Impedance (TDR) 6
3.4 Ground Via on Thermal Pad 7
4 Test Result 7
4.1 HDMI2.0 Test Setup 7
4.2 HDMI2.0 Trace Loss 7
4.3 HDMI2.0 Compliance Test Result of PI3HDX1204B1 EVB 8
4.4 HDMI1.4 Compliance Test Result of PI3HDX1204B1 EVB 10
5 References 12

1 Introduction

PI3HDX1204B1 is a dual-mode DP level shifter and HDMI 2.0 re-driver. As HDMI data rate can be as fast as 6Gbps, signal integrity is critical. Typical application circuit, layout guideline and test setup are described in this application information.

2 EVB Schematic

2.1 Source Application

PI3HDX1204B1 is designed to accept AC-coupled as well as DC-coupled main link signals. When a dual-mode DP source is connected to the input of PI3HDX1204B1 in a source application, AC coupling capacitors must be placed at the input side.

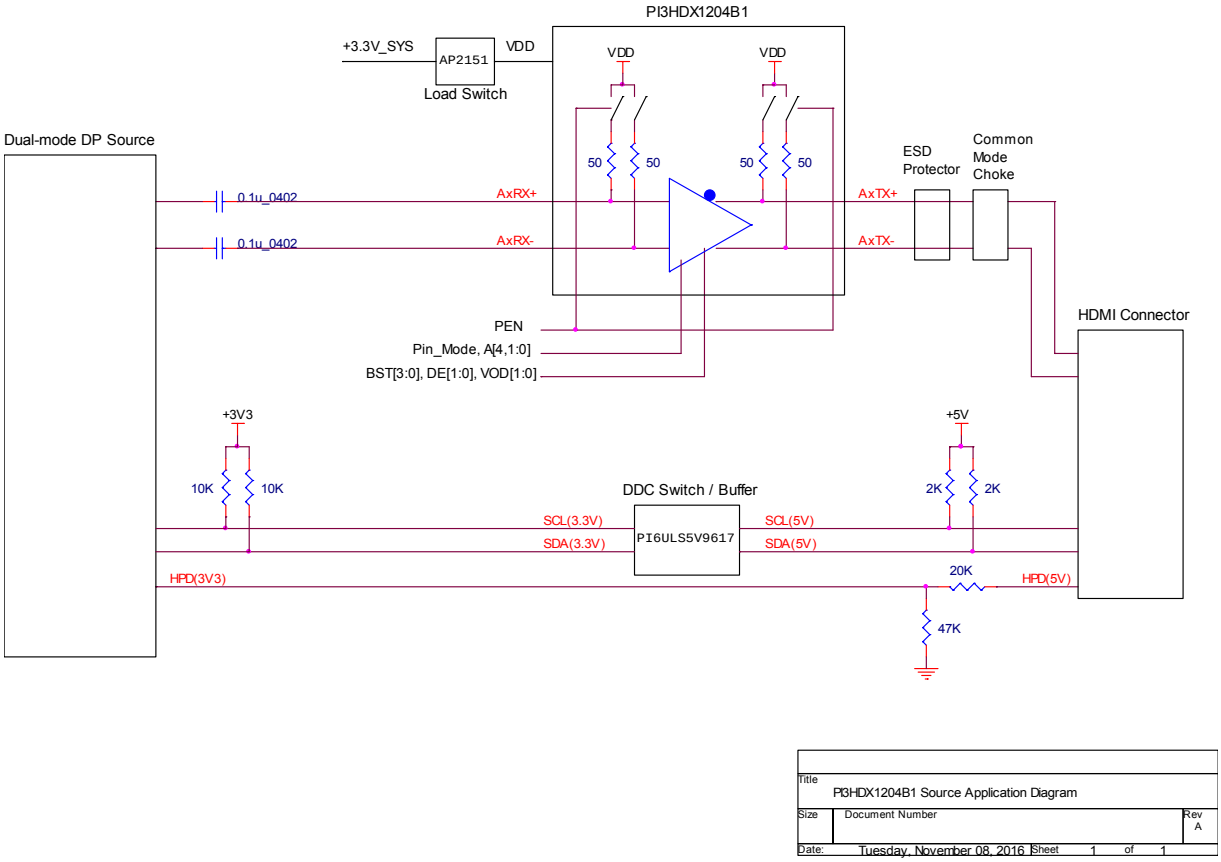

Figure 1: PI3HDX1204B1 Source Application Circuit

2.1.1 ESD Protectors on Output TMDS

As 8kV contact ESD is commonly required, ESD protectors are implemented at the output TMDS pins of PI3HDX1204B1 for source application. ESD8104 HDMI2.0 ESD protector can be considered to protect the 3.3V TMDS paths as its reverse working voltage is 3.3V.
http://www.onsemi.com/pub_link/Collateral/ESD8104-D.PDF

2.1.2 Extra Component for Rise/fall Time Control

Per HDMI2.0 specification, rise/fall time of TMDS clock is kept at minimal 75ps while that of TMDS data is decreased to minimal 42.5ps if data rate is between 3.4Gbps and 6Gbps.

Table 7-3 Source TMDS Electrical - 6G – T_{RISE}, T_{FALL} Requirements

Reference	Requirement
[HDMI 2.0: Table 6-2] AC Characteristics for 3.4 Gbps < R_{bit} ≤ 6.0 Gbps at TP1	Rise/Fall time: Data (20% to 80%): ≥42.5 ps Rise/Fall time: Clock (20% to 80%): ≥75 ps

Table 1: HDMI2.0 Trise/fall Requirement

PI3HDX1204B1 is designed to meet the rise/fall time of TMDS data. If output trace length is short, maybe 1” only, common-mode choke or external inductor can be considered for slowing down the rise/fall time for TMDS clock of PI3HDX1204B1.

2.1.3 Leakage Blockage for VOFF Test

When performing VOFF test specified in HDMI1.4a Compliance Test Specification, each output TMDS of PI3HDX1204B1 will be pulled to 3.3V via an external 50kΩ resistor. In this case, current will pass through an internal ESD protector at the output TMDS pin of PI3HDX1204B1 and leakage will be found at VCC pin of PI3HDX1204B1.

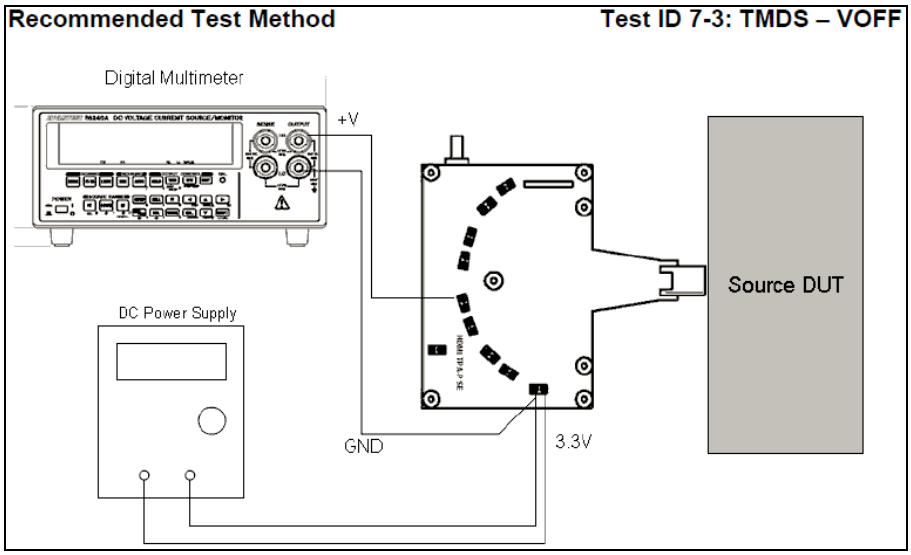

Figure 2: HDMI1.4 VOFF Test Setup

Test ID 7-3: TMDS – V_{OFF}	
Reference	**Requirement**
[HDMI: Table 4-23] Source DC Characteristics at TP1	TMDS single-ended standby (off) output voltage, V_{OFF} must be within AVcc ±10mVolts.

Table 2: HDMI1.4 VOFF Requirement

To avoid this leakage, AP2151A power switch can be employed between the main 3.3V supply on a system and the VCC power plane of PI3HDX1204B1. Below is an example borrowed from an evaluation board schematic.

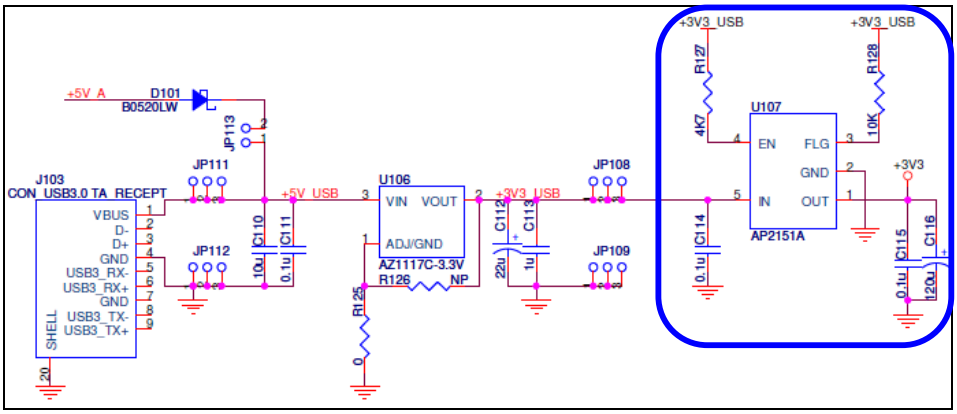

Figure 3: Power Distribution Switch Example

2.2 Sink Application

PI3HDX1204B1 can also be employed in a sink application as it offers a range of equalization setting.

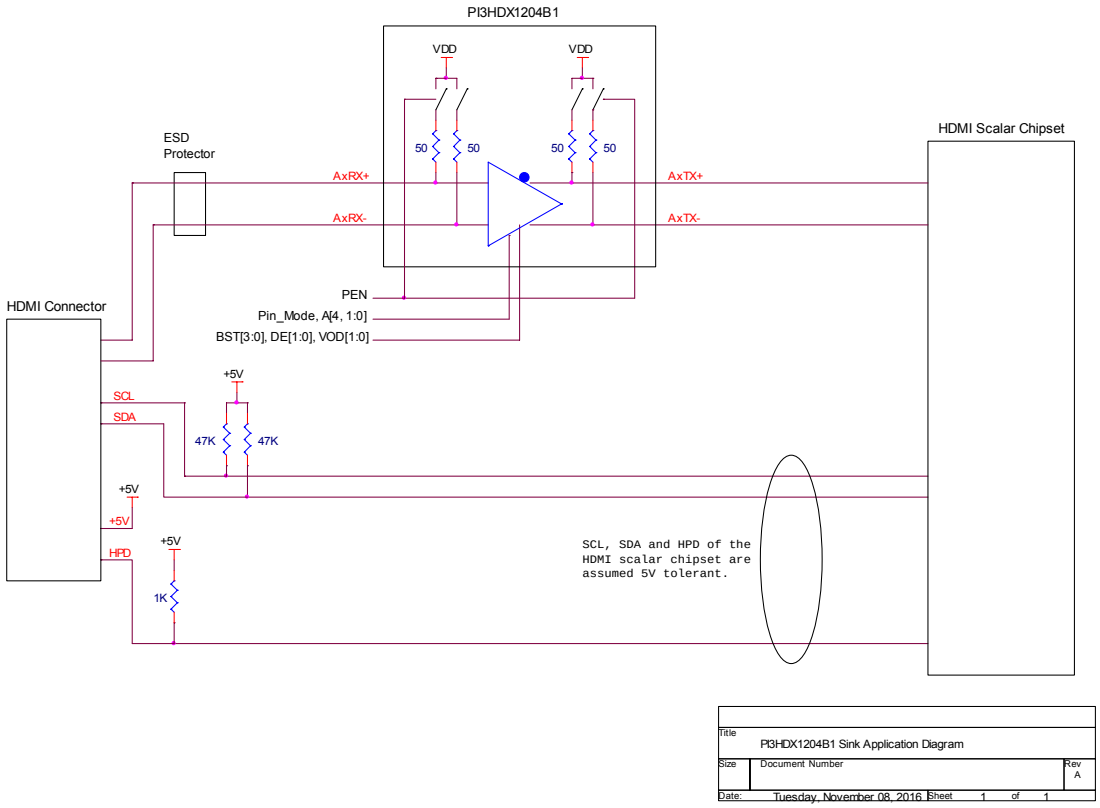

Figure 4: PI3HDX1204B1 Sink Application Circuit

2.2.1 ESD Protectors on Input TMDS

ESD protector selection guidance for source and sink applications is the same. Please refer to Section 2.1.1 for details.

3 Layout Design Guideline

3.1 AC Coupling Capacitor

Below is an example of placing AC coupling capacitors on high-speed channels.

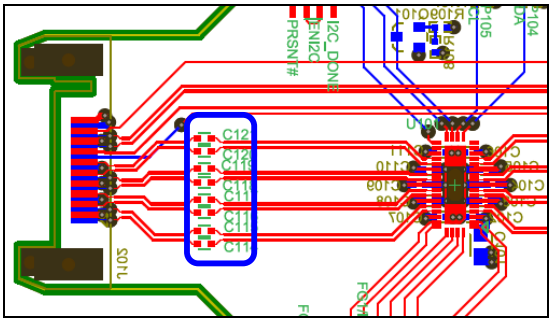

Figure 5: AC Coupling Capacitor Placement

3.2 Output Trace Length

To fulfill minimal 75ps rise/fall time requirement of TMDS clock, 1.5 – 4.5” TMDS trace length between PI3HDX1204B1 and HDMI connector for source application is recommended. This trace length varies with PCB trace width, characteristics of common-mode choke/ESD protector and connector quality. If trace width is 5 mil, 2.7 – 3.3” is recommended. Furthermore, isolation space should be larger than 5 mil to minimize the crosstalk so thus jitter. Below is the PI3HDX1204B1 placement on its evaluation board.

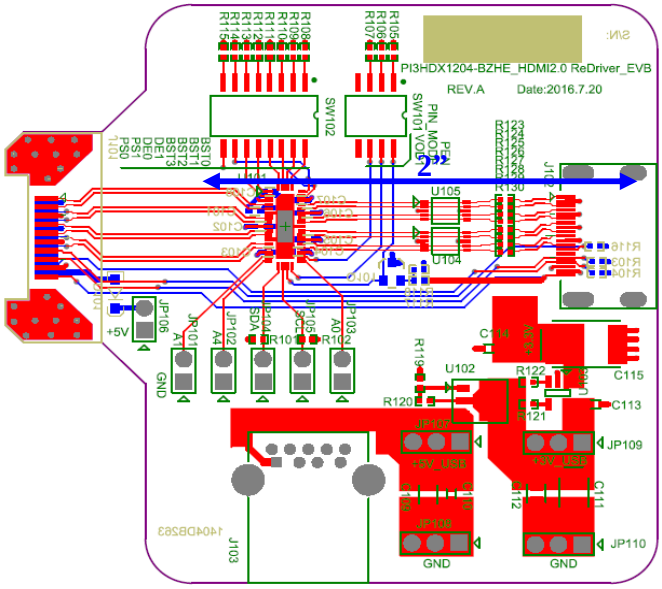

Figure 6: PI3HDX1204B1 Source EVB PCB

3.3 Differential Impedance (TDR)

Layout guideline especially for high-speed transmission is critical. Please refer to PI3DPxxx_PI3HDxxx_Layout Guideline for detailed recommendations. Differential impedance test is required for both source and sink applications per HDMI2.0 specification.

Table 7-17 Source TMDS Electrical - 6G – Differential Impedance Requirements

Reference	Requirement
[HDMI 2.0: Table 6-3] Source Impedance Characteristics for (3.4 Gbps < R_{bit} ≤ 6.0 Gbps) at TP1	Through Connection ImpedanceΔ: 100 Ω +/- 15%◊ ◊ single excursion is permitted out to a max/min of 100 Ω +/- 25% and of a duration less than 250 ps. Δ Impedance from TP1 to Source Termination Source Termination Impedance: 75 to 150 Ω

Table 3: HDMI2.0 Differential Impedance Requirement for Source Application

Table 8-7 Sink TMDS Electrical - 6G – Differential Impedance Requirements

Reference	Requirement
[HDMI 2.0: Table 6-8] Sink Impedance Characteristics for (3.4 Gbps < R_{bit} ≤ 6.0 Gbps) at TP2	Through Connection ImpedanceΔ: 100 Ω +/- 15%◊ ◊ A single excursion is permitted out to a max/min of 100 Ω ±25% and of duration less than 250 ps. Δ Impedance from TP2 to Sink Termination Sink Termination Impedance: 90 Ω to 110 Ω

Table 4: HDMI2.0 Differential Impedance Requirement for Sink Application

The PCB impedance immediately before and after an ESD protector must be adjusted to compensate the capacitance loading of the ESD protector. Below is an example designing RClampe0544M in PI3HDX1204B1 evaluation board. Trace impedances before and after the ESD protector are tuned to compensate the capacitance of RClamp0544M. Semtech's layout guideline is followed.
https://www.semtech.com/images/promo/Layout_Guidelines_for_adding_ESD_Protection_in_HDMI.pdf

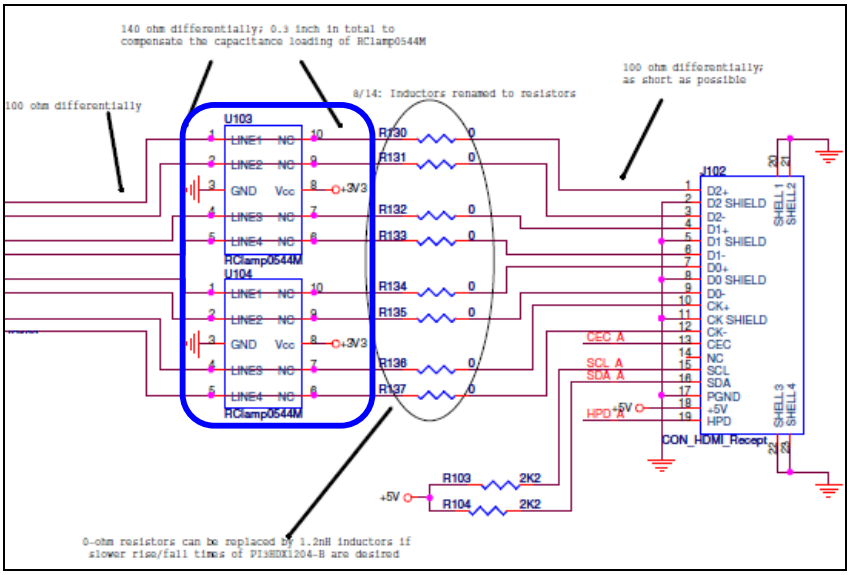

Figure 7: ESD Protector on PI3HDX1204D(-B) Source EVB

3.4 Ground Via on Thermal Pad

At least eight ground vias are required on thermal pad of PI3HDX1204B1. The recommended via size is 12/24 mil. Below is a reference for PI3HDX1204B1 ground pad.

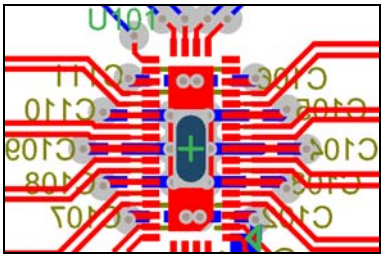

Figure 8: Thermal Pad Design Example

4 Test Result

4.1 HDMI2.0 Test Setup

HDMI2.0 source test setup is available for evaluation and pre-test. Below is the internal HDMI2.0 test setup.

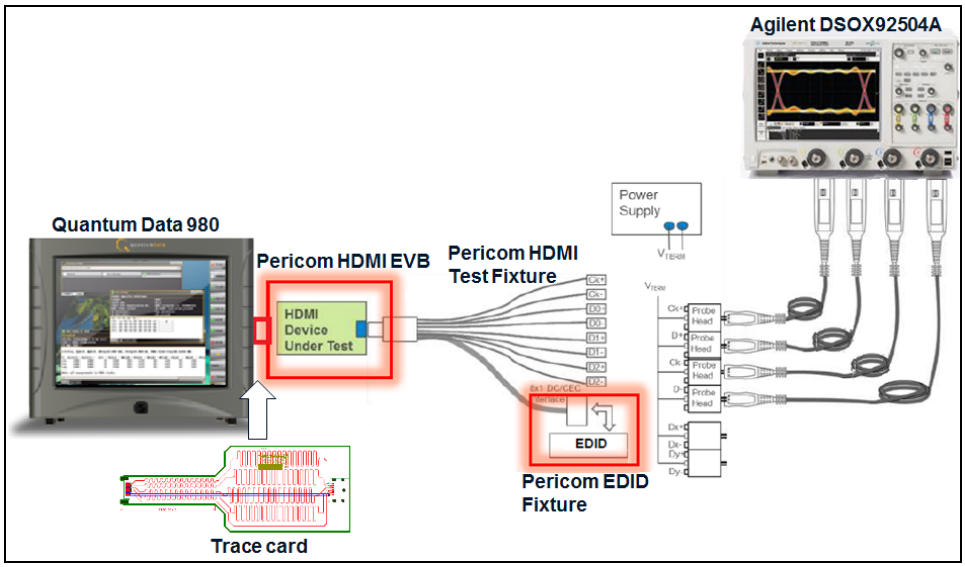

Figure 9: HDMI2.0 Test Setup

4.2 HDMI2.0 Trace Loss

PI3HDX1204B1 is evaluated with the use of tailor-made FR4 trace cards as input traces plugged to the EVB.

HDMI FR4 trace	0 in	6 in	12 in	18 in	24 in	30 in	36 in
Insertion loss @ 6Gbps	-5.91 dB	-9.75 dB	-10.47 dB	-13.05 dB	-15.87 dB	-16.97 dB	-21.20 dB

Table 5: HDMI2.0 FR4 Trace Loss

4.3 HDMI2.0 Compliance Test Result of PI3HDX1204B1 EVB

KEYSIGHT TECHNOLOGIES

HDMI Test Report

Overall Result: PASS

Test Configuration Details	
Device Description	
Device ID	Transmitter
Fixture Type	Other
Probe Connection	4 Probes
Probe Head Type	N5444A
Lane Connection	1 Data Lane
HDMI Specification	2.0
HDMI Test Type	TMDS Physical Layer Tests
Test Session Details	
Infiniium SW Version	05.60.00603
Infiniium Model Number	DSOX92504A
Infiniium Serial Number	MY54410104
Application SW Version	2.11
Debug Mode Used	No
Probe (Channel 1)	Model: N2801A Serial: US54094067 Head: N5444A Atten: Calibrated (9 AUG 2016 14:10:30), Using Cal Atten (5.6226E+000) Skew: Calibrated (9 AUG 2016 14:11:12), Using Cal Skew
Probe (Channel 2)	Model: N2801A Serial: US54094054 Head: N5444A Atten: Calibrated (9 AUG 2016 14:15:19), Using Cal Atten (5.4285E+000) Skew: Calibrated (9 AUG 2016 14:16:00), Using Cal Skew
Probe (Channel 3)	Model: N2801A Serial: US54094059 Head: N5444A Atten: Calibrated (9 AUG 2016 14:19:22), Using Cal Atten (5.6325E+000) Skew: Calibrated (9 AUG 2016 14:20:11), Using Cal Skew
Probe (Channel 4)	Model: N2801A Serial: US54094057 Head: N5444A Atten: Calibrated (9 AUG 2016 15:17:37), Using Cal Atten (5.5290E+000) Skew: Calibrated (9 AUG 2016 15:18:23), Using Cal Skew
Last Test Date	2016-08-26 12:54:52 UTC +08:00

Summary of Results

Test Statistics	
Failed	0
Passed	46
Total	46

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	HF1-2: Clock Rise Time	127.210 ps	69.6 %	VALUE >= 75.000 ps
✓	0	1	HF1-2: Clock Fall Time	127.596 ps	70.1 %	VALUE >= 75.000 ps
✓	0	1	HF1-6: Clock Duty Cycle(Minimum)	49.760	24.4 %	>=40%
✓	0	1	HF1-6: Clock Duty Cycle(Maximum)	50.310	16.2 %	<=60%
✓	0	1	HF1-6: Clock Rate	148.456300000 MHz	2.4 %	85.000000000 MHz <= VALUE <= 150.000000000 MHz
✓	0	1	HF1-7: Differential Clock Voltage Swing, Vs (TP1)	1.097 V	12.9 %	400 mV < VALUE < 1.200 V
✓	0	1	HF1-7: Clock Jitter (TP2_EQ with Worst Case Positive Skew)	175 mTbit	41.7 %	VALUE <= 300 mTbit
✓	0	1	HF1-7: Clock Jitter (TP2_EQ with Worst Case Negative Skew)	225 mTbit	25.0 %	VALUE <= 300 mTbit
✓	0	1	HF1-5: D0 Maximum Differential Voltage	605 m	22.4 %	VALUE <= 780 m
✓	0	1	HF1-5: D0 Minimum Differential Voltage	-598 m	23.3 %	VALUE >= -780 m
✓	0	1	HF1-2: D0 Rise Time	107.100 ps	152.0 %	VALUE >= 42.500 ps
✓	0	1	HF1-2: D0 Fall Time	107.220 ps	152.3 %	VALUE >= 42.500 ps
✓	0	1	HF1-8: D0 Mask Test (TP2_EQ with Worst Case Positive Skew)	0.000	50.0 %	No Mask Failures
✓	0	1	HF1-8: D0 Mask Test (TP2_EQ with Worst Case Negative Skew)	0.000	50.0 %	No Mask Failures
✓	0	1	HF1-1: VL Clock +	2.731 V	46.1 %	2.300 V <= VALUE <= 3.100 V
✓	0	1	HF1-1:Clock + VSwing	552 mV	12.0 %	200 mV <= VALUE <= 600 mV
✓	0	1	HF1-1: VL Clock -	2.723 V	47.1 %	2.300 V <= VALUE <= 3.100 V
✓	0	1	HF1-1:Clock - VSwing	552 mV	12.0 %	200 mV <= VALUE <= 600 mV
✓	0	1	HF1-4: Intra-Pair Skew - Clock	28 mTbit	40.7 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	1	HF1-1: VL D0+	2.777 V	20.5 %	2.300 V <= VALUE <= 2.900 V
✓	0	1	HF1-1: D0+ VSwing	488 mV	44.0 %	400 mV <= VALUE <= 600 mV
✓	0	1	HF1-1: VL D0-	2.764 V	22.7 %	2.300 V <= VALUE <= 2.900 V
✓	0	1	HF1-1: D0- VSwing	501 mV	50.0 %	400 mV <= VALUE <= 600 mV
✓	0	1	HF1-4: Intra-Pair Skew - Data Lane 0	50 mTbit	33.3 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	1	HF1-5: D1 Maximum Differential Voltage	610 m	21.8 %	VALUE <= 780 m
✓	0	1	HF1-5: D1 Minimum Differential Voltage	-601 m	22.9 %	VALUE >= -780 m
✓	0	1	HF1-2: D1 Rise Time	109.200 ps	156.9 %	VALUE >= 42.500 ps
✓	0	1	HF1-2: D1 Fall Time	106.130 ps	149.7 %	VALUE >= 42.500 ps
✓	0	1	HF1-8: D1 Mask Test (TP2_EQ with Worst Case Positive Skew)	0.000	50.0 %	No Mask Failures
✓	0	1	HF1-8: D1 Mask Test (TP2_EQ with Worst Case Negative Skew)	0.000	50.0 %	No Mask Failures
✓	0	1	HF1-4: Intra-Pair Skew - Data Lane 1	-26 mTbit	41.3 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	1	HF1-1: VL D1+	2.759 V	23.5 %	2.300 V <= VALUE <= 2.900 V
✓	0	1	HF1-1: D1+ VSwing	492 mV	46.0 %	400 mV <= VALUE <= 600 mV
✓	0	1	HF1-1: VL D1-	2.756 V	24.0 %	2.300 V <= VALUE <= 2.900 V
✓	0	1	HF1-1: D1- VSwing	492 mV	46.0 %	400 mV <= VALUE <= 600 mV
✓	0	1	HF1-5: D2 Maximum Differential Voltage	603 m	22.7 %	VALUE <= 780 m
✓	0	1	HF1-5: D2 Minimum Differential Voltage	-593 m	24.0 %	VALUE >= -780 m
✓	0	1	HF1-2: D2 Rise Time	103.460 ps	143.4 %	VALUE >= 42.500 ps
✓	0	1	HF1-2: D2 Fall Time	103.160 ps	142.7 %	VALUE >= 42.500 ps
✓	0	1	HF1-8: D2 Mask Test (TP2_EQ with Worst Case Postive Skew)	0.000	50.0 %	No Mask Failures
✓	0	1	HF1-8: D2 Mask Test (TP2_EQ with Worst Case Negative Skew)	0.000	50.0 %	No Mask Failures
✓	0	1	HF1-1: VL D2+	2.775 V	20.8 %	2.300 V <= VALUE <= 2.900 V
✓	0	1	HF1-1: D2+ VSwing	487 mV	43.5 %	400 mV <= VALUE <= 600 mV
✓	0	1	HF1-1: VL D2-	2.775 V	20.8 %	2.300 V <= VALUE <= 2.900 V
✓	0	1	HF1-1: D2- VSwing	479 mV	39.5 %	400 mV <= VALUE <= 600 mV
✓	0	1	HF1-4: Intra-Pair Skew - Data Lane 2	21 mTbit	43.0 %	-150 mTbit <= VALUE <= 150 mTbit

4.4 HDMI1.4 Compliance Test Result of PI3HDX1204B1 EVB

KEYSIGHT TECHNOLOGIES

HDMI Test Report

Overall Result: PASS

Test Configuration Details	
Device Description	
Device ID	Transmitter
Fixture Type	Other
Probe Connection	4 Probes
Probe Head Type	N5444A
Lane Connection	1 Data Lane
HDMI Specification	2.0
HDMI Test Type	TMDS Physical Layer Tests
Test Session Details	
Infiniium SW Version	05.60.00603
Infiniium Model Number	DSOX92504A
Infiniium Serial Number	MY54410104
Application SW Version	2.11
Debug Mode Used	No
Probe (Channel 1)	Model: N2801A Serial: US54094067 Head: N5444A Atten: Calibrated (9 AUG 2016 14:10:30), Using Cal Atten (5.6226E+000) Skew: Calibrated (9 AUG 2016 14:11:12), Using Cal Skew
Probe (Channel 2)	Model: N2801A Serial: US54094054 Head: N5444A Atten: Calibrated (9 AUG 2016 14:15:19), Using Cal Atten (5.4285E+000) Skew: Calibrated (9 AUG 2016 14:16:00), Using Cal Skew
Probe (Channel 3)	Model: N2801A Serial: US54094059 Head: N5444A Atten: Calibrated (9 AUG 2016 14:19:22), Using Cal Atten (5.6325E+000) Skew: Calibrated (9 AUG 2016 14:20:11), Using Cal Skew
Probe (Channel 4)	Model: N2801A Serial: US54094057 Head: N5444A Atten: Calibrated (9 AUG 2016 15:17:37), Using Cal Atten (5.5290E+000) Skew: Calibrated (9 AUG 2016 15:18:23), Using Cal Skew
Last Test Date	2016-08-26 11:39:50 UTC +08:00

Summary of Results

Test Statistics	
Failed	0
Passed	19
Total	19

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	7-9: Clock Jitter	119 mTbit	52.4 %	VALUE <= 250 mTbit
✓	0	1	7-4: Clock Rise Time	122.677 ps	63.6 %	VALUE >= 75.000 ps
✓	0	1	7-4: Clock Fall Time	126.466 ps	68.6 %	VALUE >= 75.000 ps
✓	0	1	7-8: Clock Duty Cycle(Minimum)	50.080	25.2 %	>=40%
✓	0	1	7-8: Clock Duty Cycle(Maximum)	50.740	15.4 %	<=60%
✓	0	1	7-10: D0 Mask Test	0.000	50.0 %	No Mask Failures
✓	0	1	7-10: D0 Data Jitter	150 m	50.0 %	<=0.3Tbit
✓	0	1	7-4: D0 Rise Time	117.192 ps	56.3 %	VALUE >= 75.000 ps
✓	0	1	7-4: D0 Fall Time	115.835 ps	54.4 %	VALUE >= 75.000 ps
✓	0	1	7-2: VL Clock +	2.739 V	46.3 %	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	7-2: VL Clock -	2.728 V	42.7 %	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	7-7: Intra-Pair Skew - Clock	23 mTbit	42.3 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	1	7-2: VL D0+	2.763 V	45.7 %	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	7-2: VL D0-	2.751 V	49.7 %	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	7-7: Intra-Pair Skew - Data Lane 0	29 mTbit	40.3 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	1	7-3: Voff Clock +	-4 mV	30.0 %	-10 mV <= VALUE <= 10 mV
✓	0	1	7-3: Voff Clock -	-5 mV	25.0 %	-10 mV <= VALUE <= 10 mV
✓	0	1	7-3: Voff D0+	-5 mV	25.0 %	-10 mV <= VALUE <= 10 mV
✓	0	1	7-3: Voff D0-	-5 mV	25.0 %	-10 mV <= VALUE <= 10 mV

5 References

(1) High-Definition Multimedia Interface Specification Version 2.0a, HDMI Forum, March 19, 2015
(2) High-Definition Multimedia Interface Specification Version 2.0h Compliance Test Specification, HDMI Forum, April 3, 2015
(3) High-Definition Multimedia Interface Specification Version 1.4b, HDMI Licensing, LLC, October 11, 2011
(4) High-Definition Multimedia Interface Compliance Test Specification Version 1.4a, HDMI Licensing, LLC, March 4, 2010
(5) SI05-03 Surging Ideas TVS Diode Application Note, Semtech, April 21, 2005