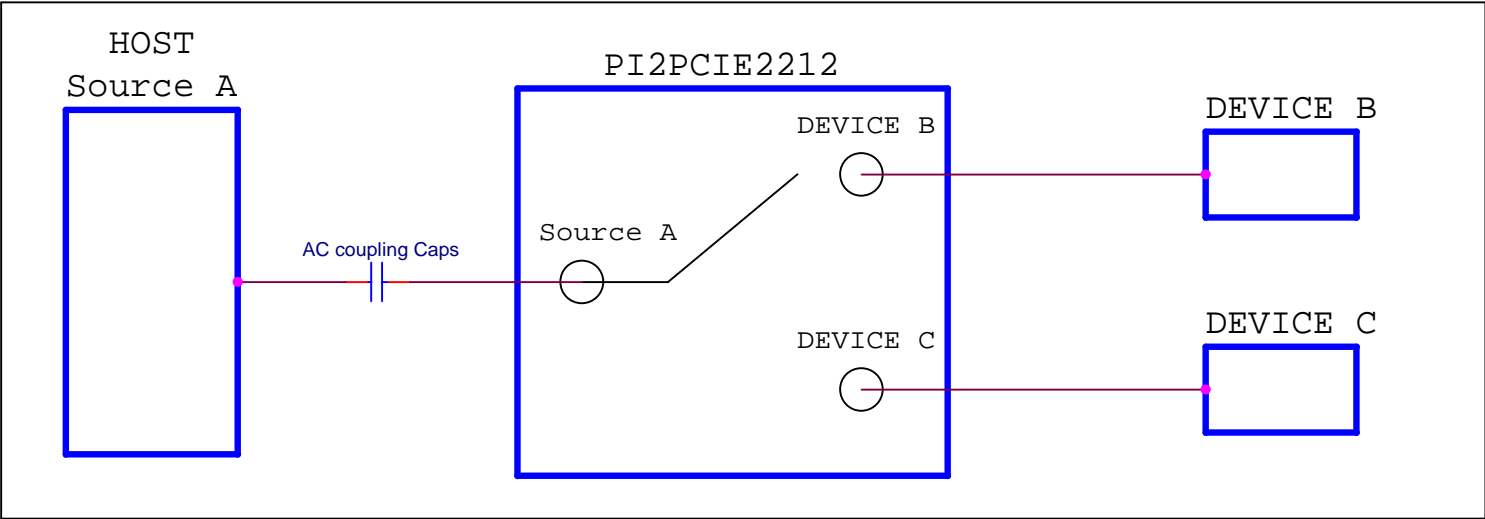
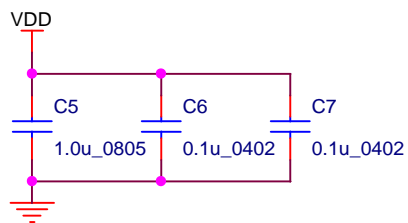


Revision History

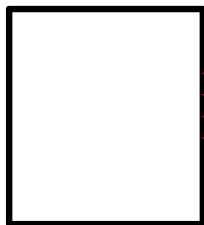
Date	History
2/26/2014	First Released

Block Diagram





Source A



A0_P
A0_N
A1_P
A1_N

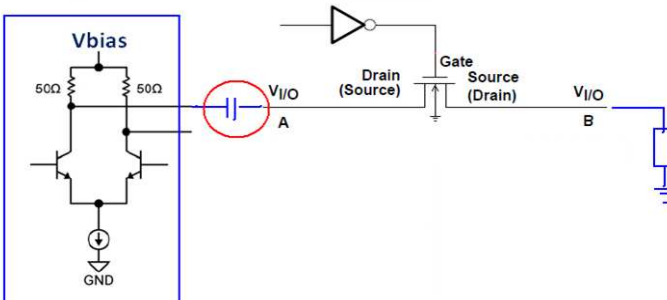
C1
C2
C3
C4

0.1uF_0402
0.1uF_0402
0.1uF_0402
0.1uF_0402

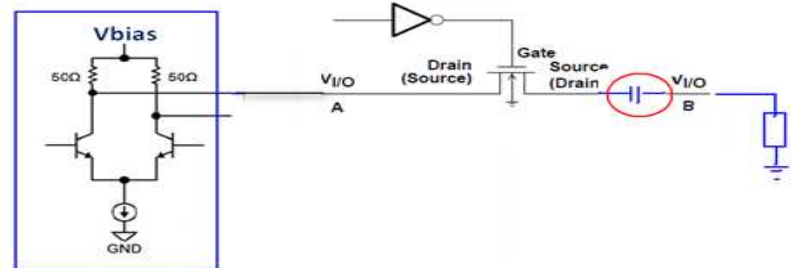


Use AC coupling cap to block DC bias.

If source side signal input Vbias Voltage higher than device Vbias Voltage , need to add the AC coupling capacitor at switch signal input.



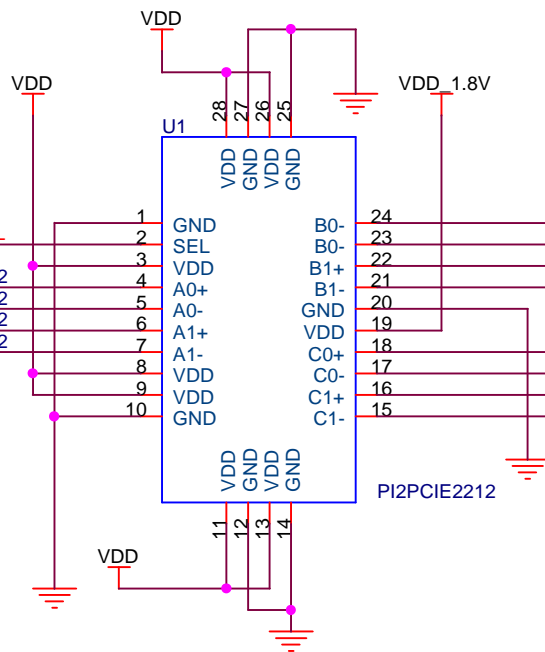
OR



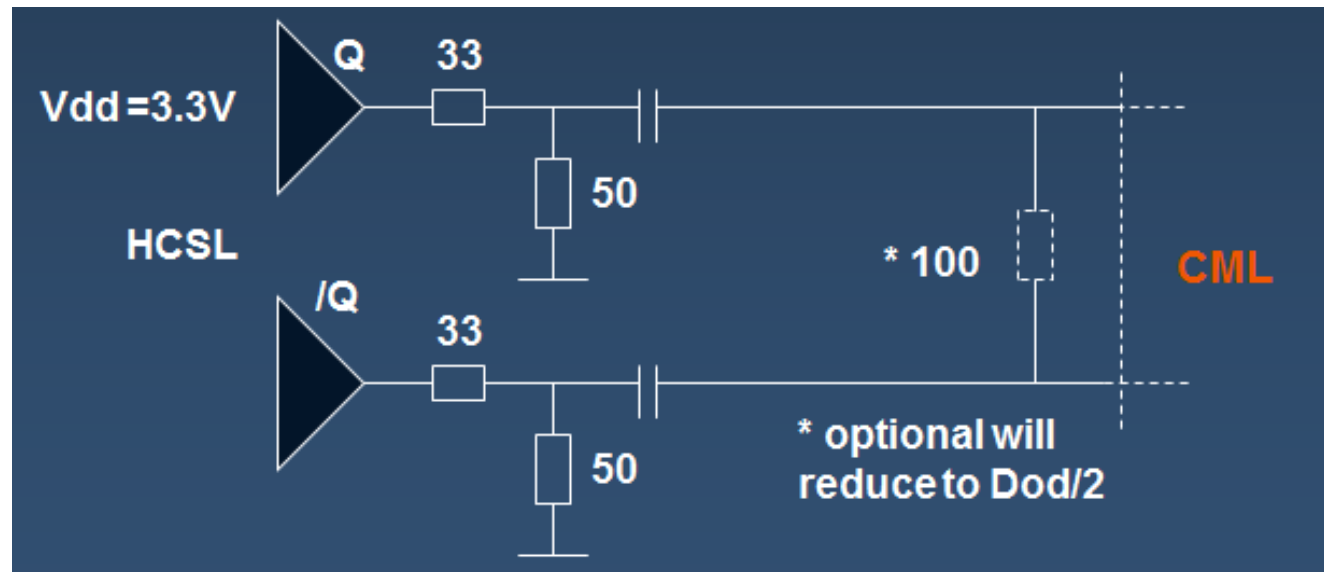
If Device side signal Vbias voltage more than source IC, need to add the AC coupling at Switch signal output.

SELECTION TRUTH TABLE

SEL	FUNCTION
0	A to B
1	A to C



HCSL to CML Clock Model



The Termination key is simple (least component count) and efficient (keep the signal quality, least loss and reflection)

DC coupling can keep DC level while transmit AC signal, but use AC coupling is much easier for cross transformation and less reliability.