For the customer use only

PI2EQX5964ZFE EvalBoard Rev.A User Guide

Introduction

Pericom Semiconductor's PI2EQX5964ZFE is a low power, PCIE compliant signal redriver. The device provides programmable equalization, amplification, and de-emphasis by using 8 elect bits, to optimize performance over a variety of physical mediums by reducing Inter-Symbol Interference.

PI2EQX5964ZFE supports eight 100-Ohm Differential CML data I/O's between the Protocol ASIC to a switch fabric, across a backplane, or to extend the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides fl edibility with signal integrity of the signal before the re-driver, whereas the integrated emphasis circuitry provides flexibility with signal integrity of the signal after the reDriver.

In addition to providing signal re-conditioning, Pericom's PI2EQX5964ZFE also provides power management Stand-by mode operated by a Power Down pin.

This user guide describes how to use PI2EQX5964ZFE ReDriver in the evaluation board. Figure1 shows top view and bottom view of PI2EQX5964ZFE EVB.

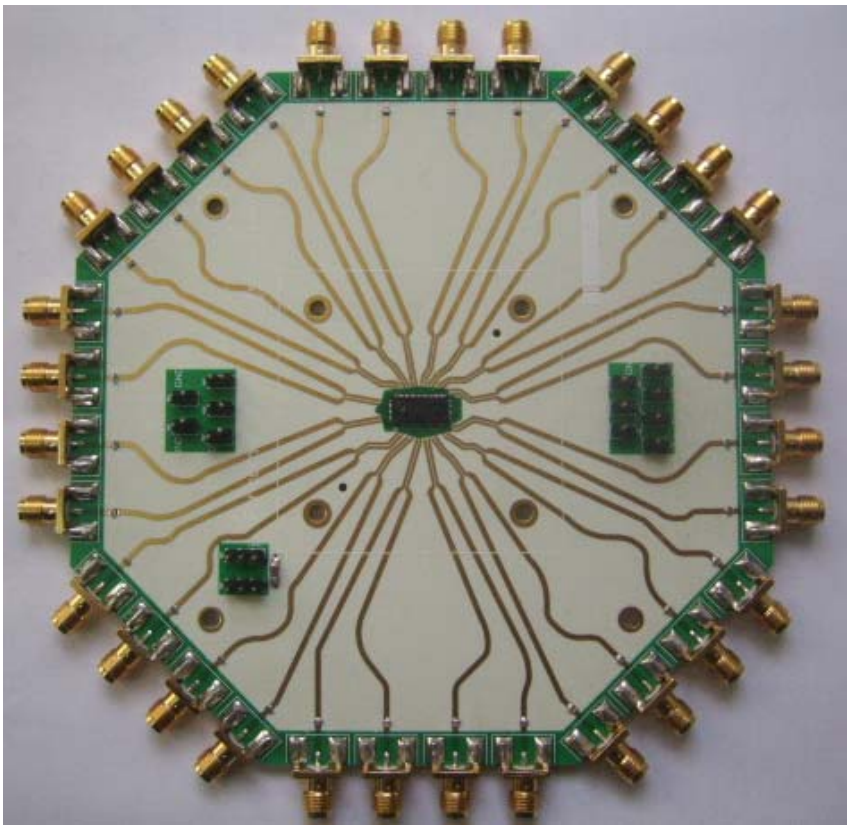


Figure1a Top View of PI2EQX5964ZFE EVB

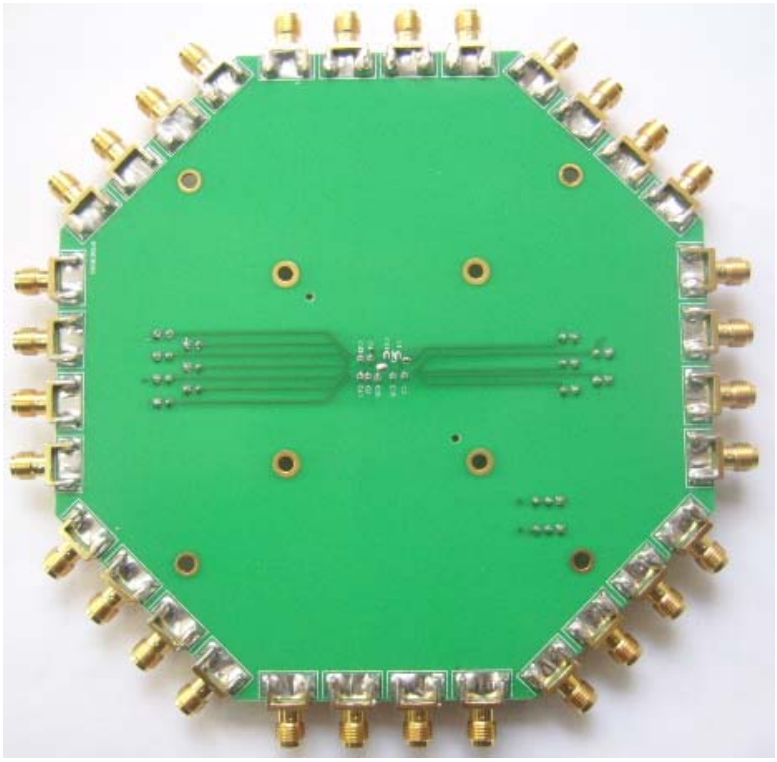


Figure1b Bottom View of PI2EQX5964ZFE EVB

Board Operation

- **Logical Block Diagram**

Figure2 shows the logical block diagram of PI2EQX5964ZFE.

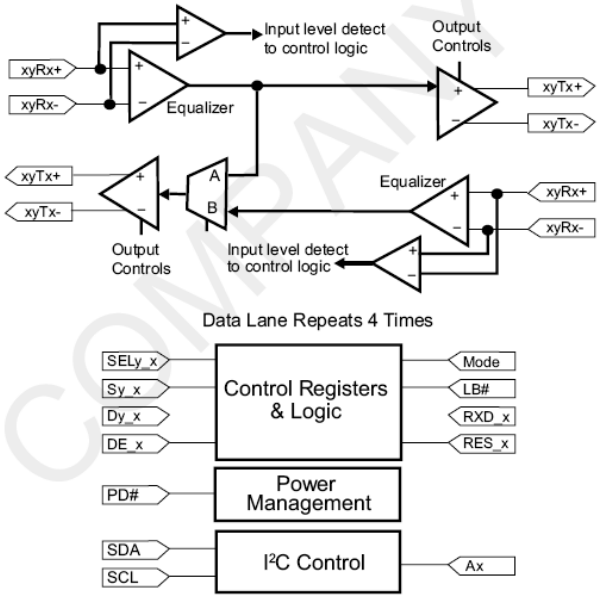


Figure2. Logical Block Diagram of PI2EQX5964ZFE

- **Board Circuit**

1) Power Supply

On the EVB, the power supply is from 3-Pin header-VDD and GND mark as below.

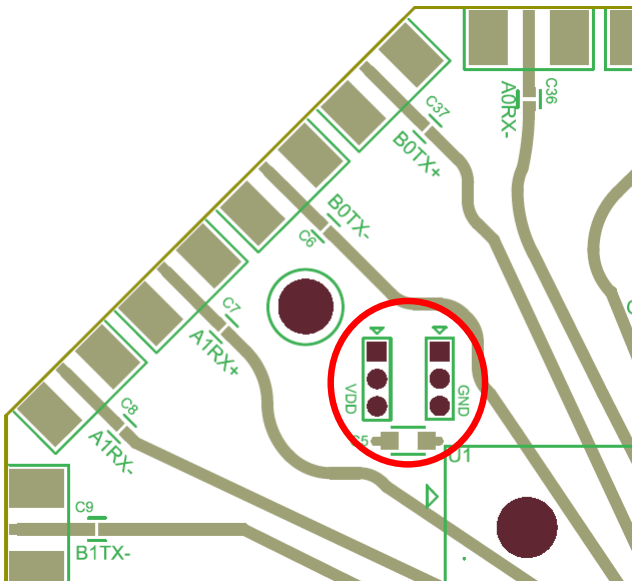


Figure3. VDD and GND pin Header Location

2) Configuration Control

PI2EQX5964ZFE provides I2C configuration control depending on the state of the MODE pin input (red circle in Figure4).

When MODE is set **LOW**, reprogramming of the control registers via I2C is allowed. MODE pin has internal 100K pull-up resistor. So it should be pull down by Jumper MODE pin externally.
Figure4 shows the Mode pin location on EVB.

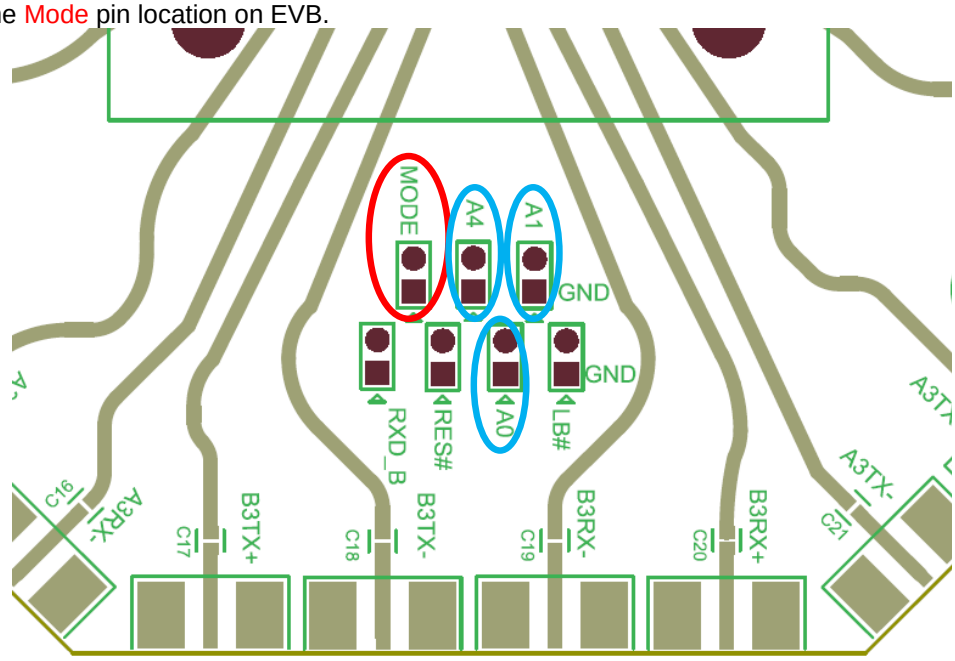


Figure4. MODE pin Header Location

- The integrated I2C interfaces operate as a slave device, supporting standard rate operation of 100Kbps, with 7-bit addressing mode and LSB indication either a read or write operation as shown below. The address for a specific device is determined by **A0, A1 and A4** pins with internal **PULL-UP** resistors. So up to eight PI2EQX5964 devices can be connected to a single I2C bus. Figure4 shows A4, A1 and A0 pin header location in **Blue** circle.

Address Assignment							
A6	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**R/W**
1	1	Program	0	0	Programmable		1=R, 0=W

- Data bytes must be 8-bits long and transferred with MSB first. Please see I2C data transfer diagram in Page16 of datasheet. For data byte definition as below, please see Page8 -11 of datasheet in detail.

Configuration Register Summary

Byte	Mnemonic	Function
0	SIG	Signal Detect, indicates valid input signal level
1	RX50	Receiver Detect Output, indicates whether a receiver load was detected
2	LBEC	Loopback and Emphasis Control, provides for control of the loopback function and emphasis mode (pre-emphasis or de-emphasis)
3	INDIS	Channel Input Disable, controls whether a channels input buffer is enabled or disabled
4	OUTDIS	Channel Output Disable: Controls whether a channels output buffer is enabled or disabled
5	RESET	Channel Reset
6	PWR	Power Down Control, enables power down for each channel individually
7	RXDE	Receiver Detect Enable, controls the receiver detect operation
8	AEOC	A-Channels Equalizer and Output Control
9	BEOC	B-Channels Equalizer and Output Control
10	RSVD	Reserved
11	VTH	Idle detect threshold control

- For I2C inputs, SCL and SDA pin are tolerant with **+3.3V power.** Figure5 is SCL and SDA pins location on EVB.

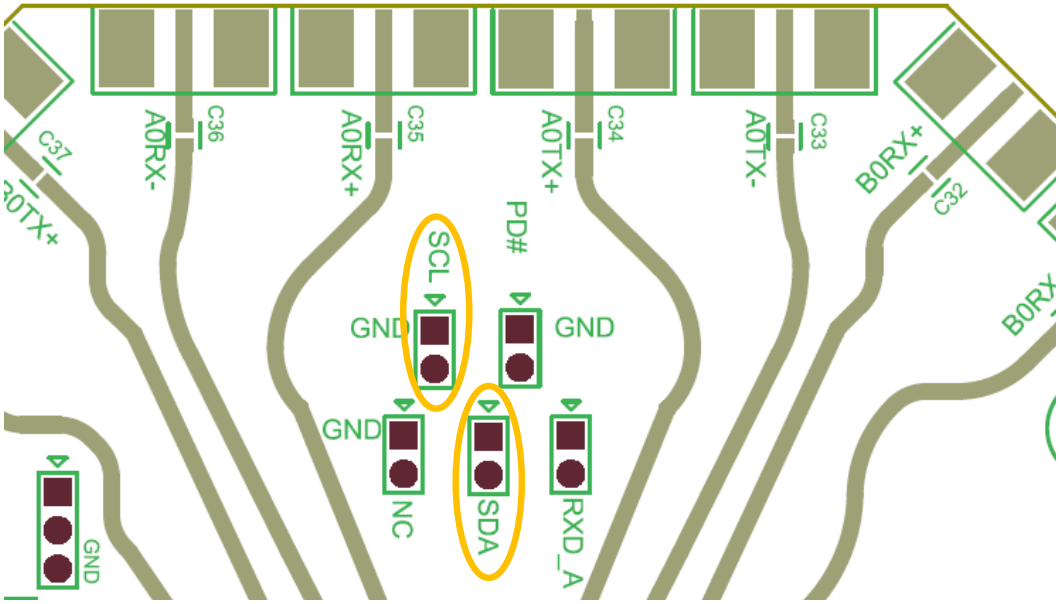


Figure5. SCL and SDA pin Header Location

NOTE: Other pins, PD#, RXD_A, RXD_B, LB# and RES# should be NC if I2C mode is selected.

- I2C Configuration Sequence

Figure6 is WRITE sequence.

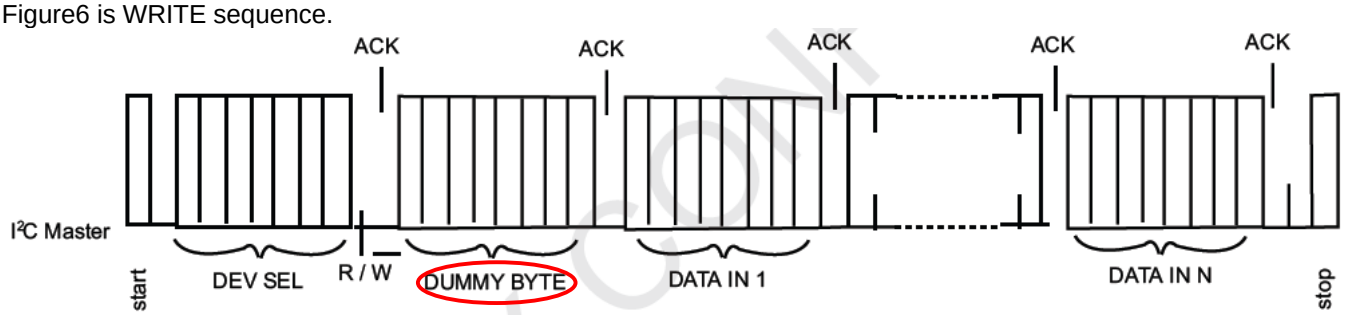


Figure6 I2C WRITE Sequence Diagram

Note: there is one DUMMY byte to be added into sequence.

Figure 7 is one sample for write sequence at Address=**C0** (A4, A1, A0 are pulled down) and Data byte[0..11]=00,00,F0,00,00,FF,FF,FF,00,00,00,EF.

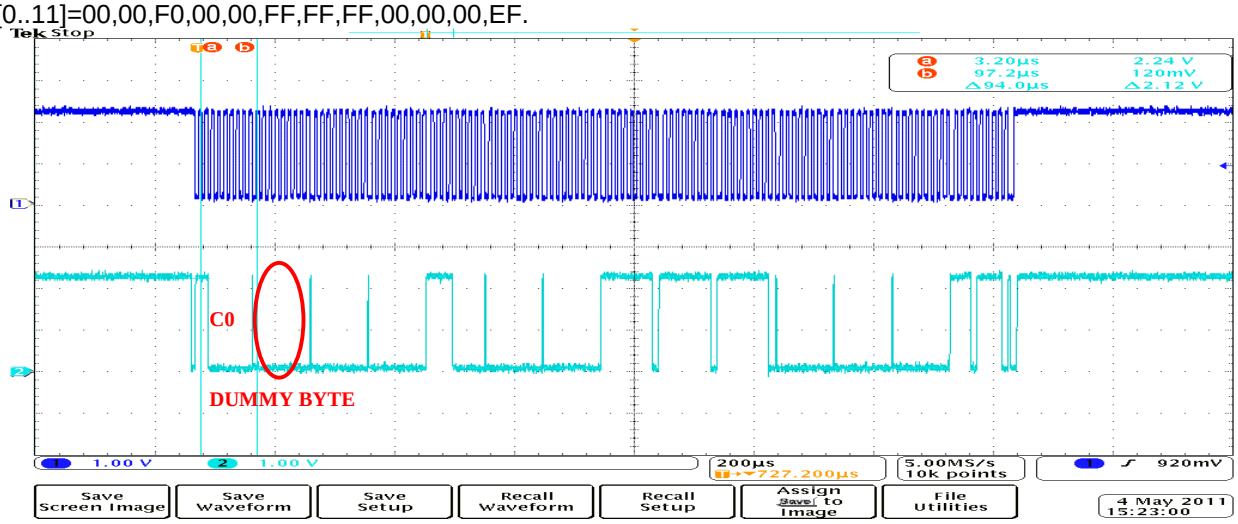


Figure7 I2C WRITE Sequence Sample

Figure8 is READ sequence.

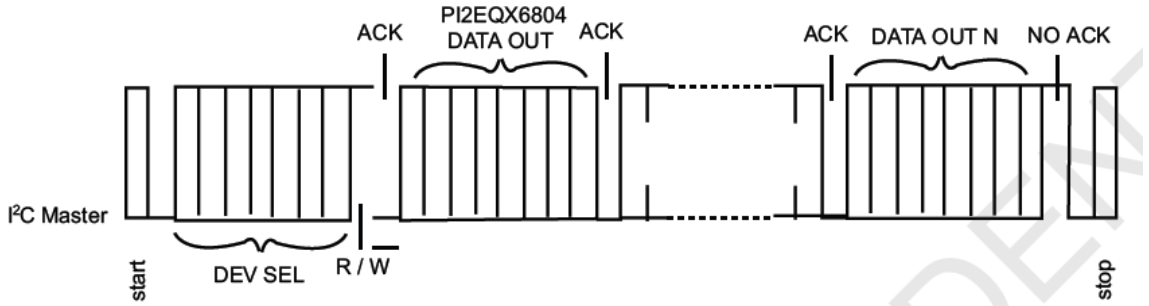


Figure8 I2C READ Sequence Diagram

Note: there is NO DUMMY byte to be added into sequence.

Figure9 is one sample for read sequence sample at Address=**C1** (A4, A1, A0 are pulled down) and Data byte[0..11]=**08**,00,F0,00,00,FF,FF,FF,00,00,00,EF.

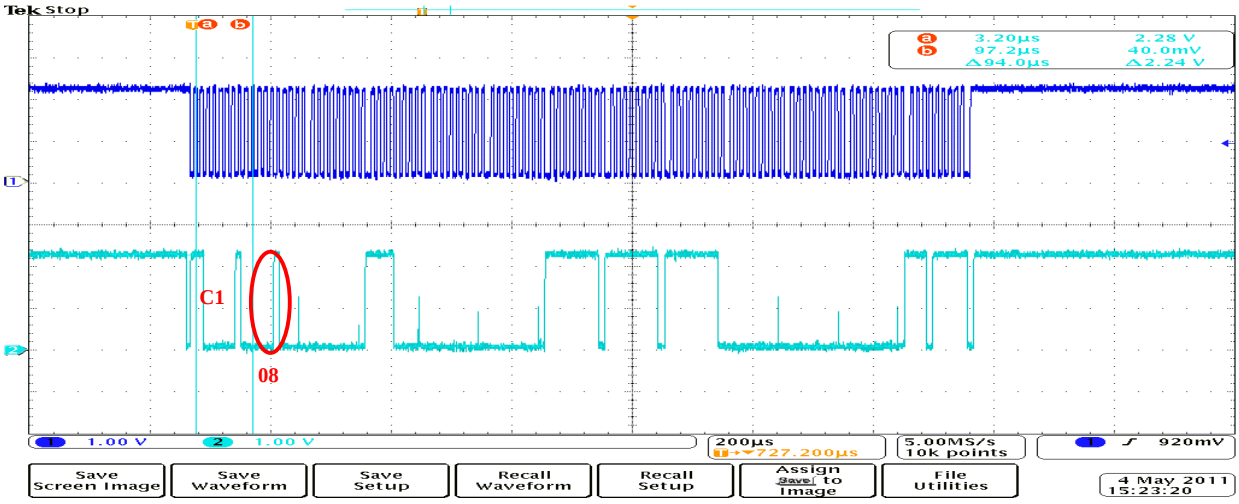
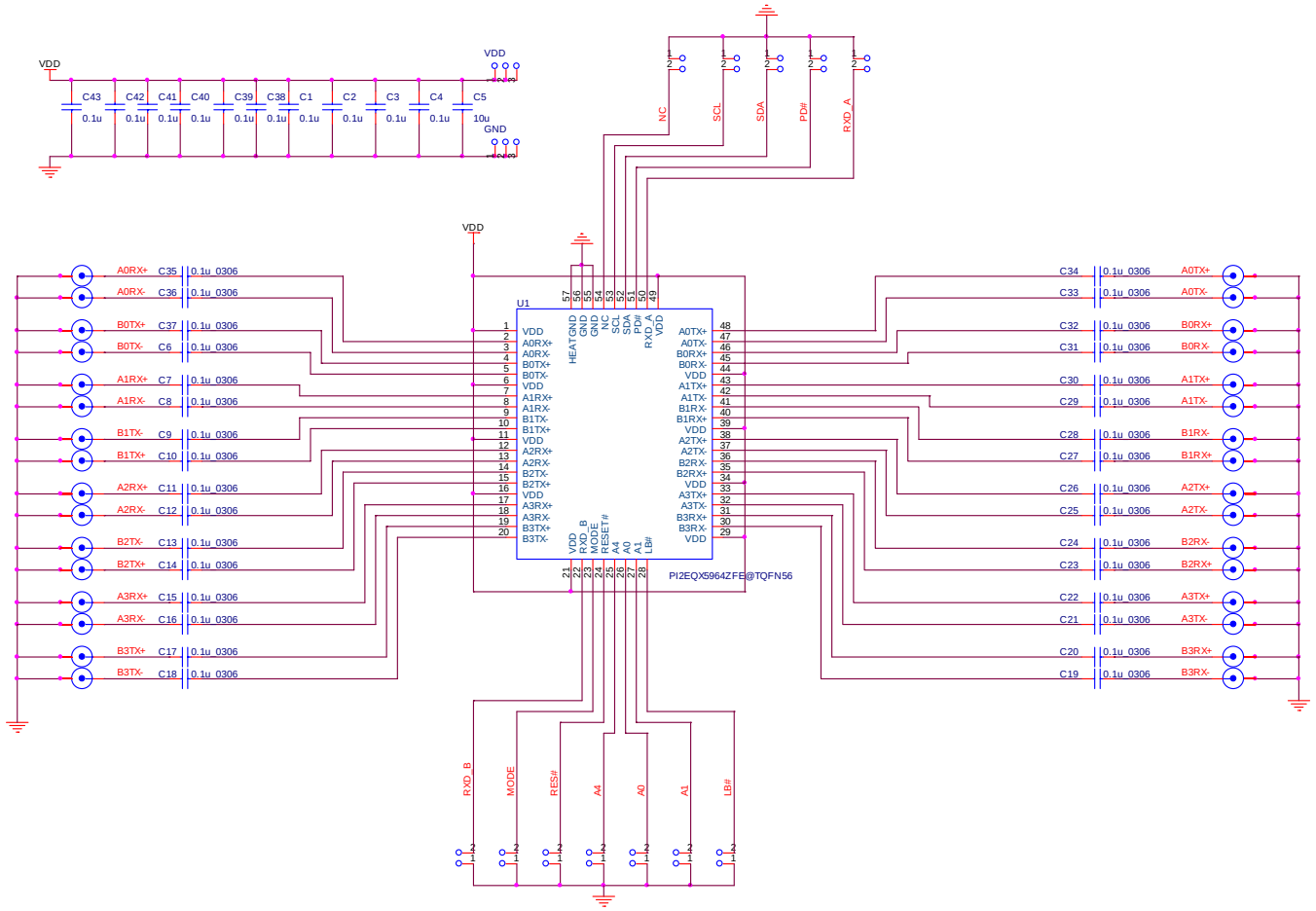


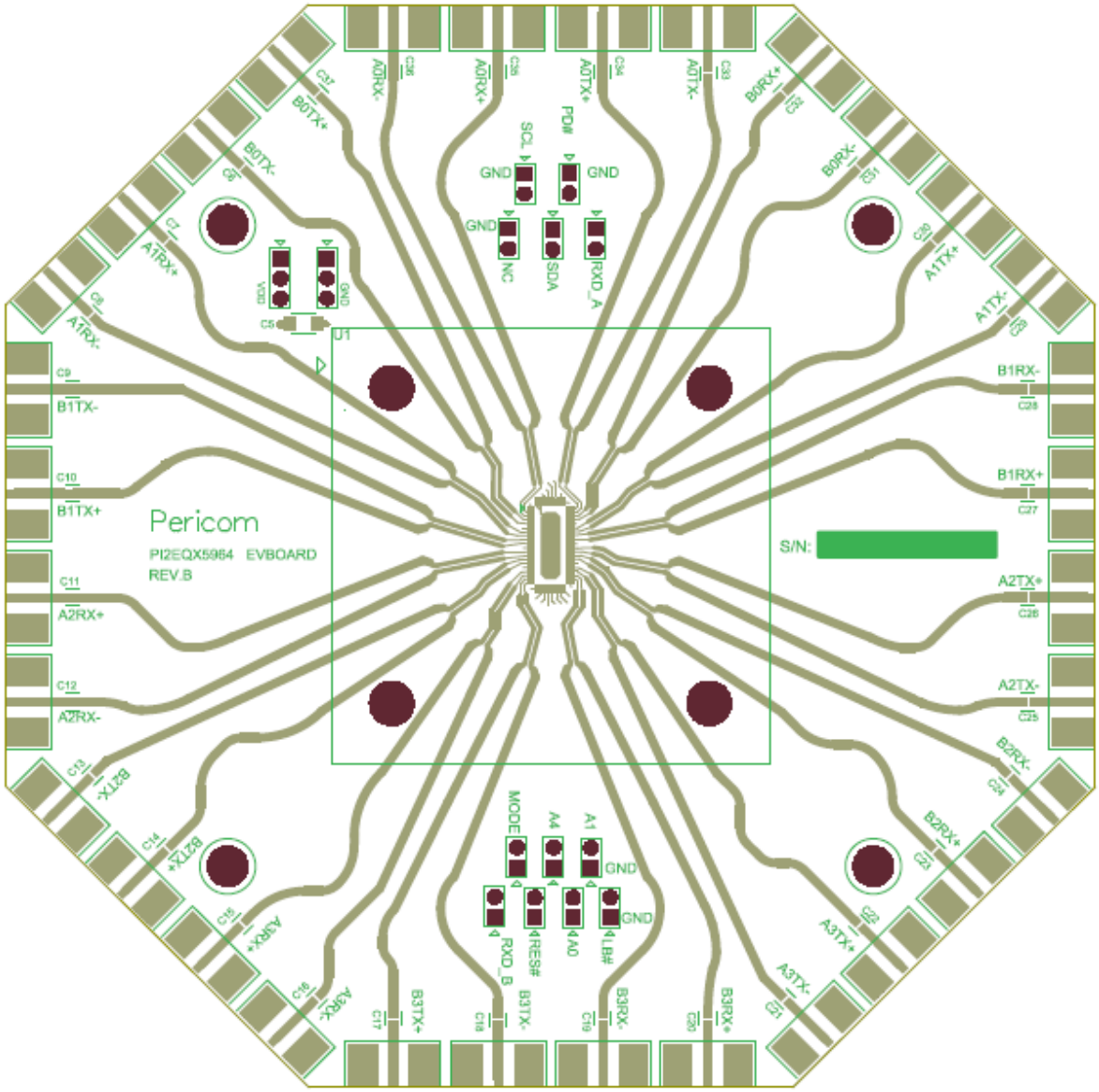
Figure9 I2C READ Sequence Sample

Note: Byte0=**08** means Channel-A2 has signal input.

Appendix A: PCB Schematic



Appendix A: PCB TOPVIEW



History

Version 1.0	Original Version	Nov. 4, 2010