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1. AP2004 Specifications

1.1 Features

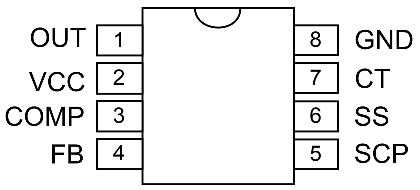
- Operating Voltage can be up to 27V
- Under Voltage Lockout (UVLO) Protection
- Short Circuit Protection (SCP)
- Soft-Start Circuit
- Variable Oscillator Frequency --- 300kHz Max
- 1.25V Voltage Reference Output
- 8-pin PDIP and SOP packages

1.2 General Description

The AP2004 integrates Pulse-Width-Modulation (PWM) control circuit into a single chip, mainly designed for power-supply regulator. All the functions include an on-chip 1.25V reference output, an adjustable oscillator, UVLO, SCP, soft-start circuitry, and a push-pull output circuit. Switching frequency is adjustable by trimming the CT. During low V_{CC} situation, the UVLO makes sure that the outputs are off until the internal circuit is operating normally.

1.3 Pin Assignments

(Top View)

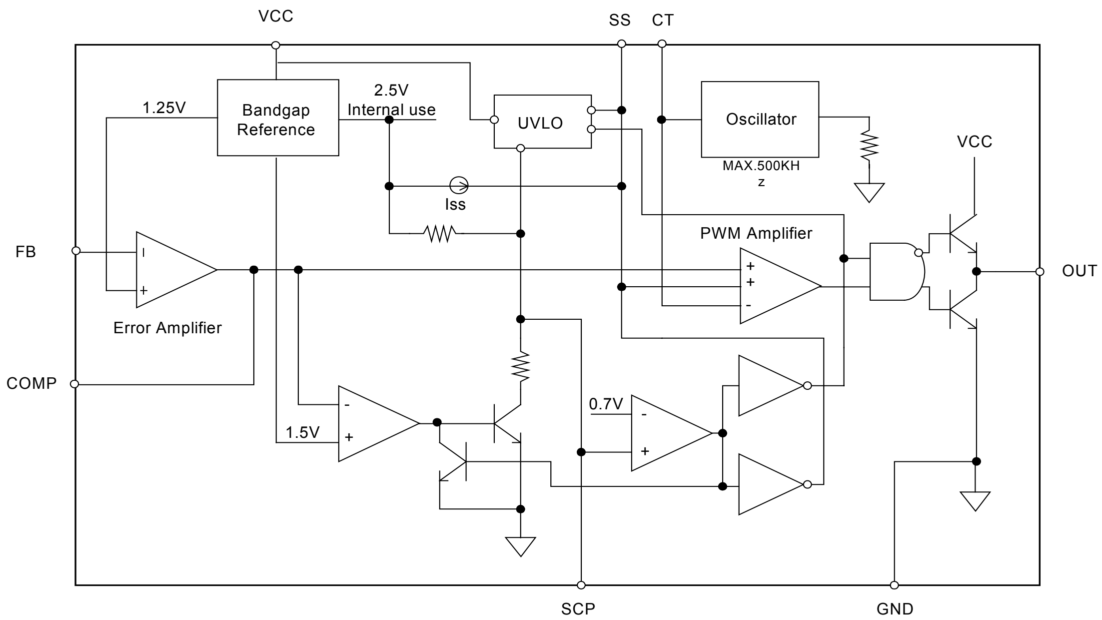


PDIP/SOP

1.4 Pin Descriptions

Name	Description
CT	Timing Capacitor
FB	Voltage Feedback
SS	Soft-Start
COMP	Feedback Loop Compensation
OUT	PWM Output
GND	Ground
V_{CC}	Supply Voltage
SCP	Short Circuit Protection

1.5 Block Diagram



1.6 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	Supply Voltage	27	V
V_I	Amplifier Input Voltage	20	V
V_O	Collector Output Voltage	V_{CC}-1.0V	V
I_{SOURCE}	Source Current	200	mA
I_{SINK}	Sink Current	200	mA
T_{OP}	Operating Temperature Range	-20 to +85	^oC
T_{ST}	Storage Temperature Range	-65 to +150	^oC
T_{LEAD}	Lead Temperature 1.6 mm (1/16 inch) from Case for 10 Seconds	260	^oC

2. Hardware

2.1 Introduction

The demo board supplies a constant DC output voltage of 3.3V, and supplies the output power up to 10W (3.3V / 3A). Using a DC input voltage of 12V, full load efficiency varies from 80 percent to 86 percent depending on the input voltage. This type of converter converts an unregulated input voltage to a regulated output voltage that is always lower than the input voltage. The control method used in the board is a fixed frequency, variable on-time pulse-width-modulation (PWM). The feedback method is used voltage-mode control. Other features of the board include Under-Voltage Lockout (UVLO), Short-Circuit Protection (SCP), and Soft-Start.

2.2 Typical Application

The AP2004 may operate in either the CCM (Continuous Conduction Mode) or the DCM (Discontinuous Conduction Mode). The following applications are designed for CCM operation. That is, the inductor current is not allowed to fall to zero. To compare the disadvantages and advantages for CCM and DCM, the main disadvantage of CCM is the inherent stability problems (caused by the right-half-plane zero and the double pole in the small-signal control to output voltage transfer function). However, the main disadvantage of DCM is that peak currents of switch and diode are larger than CCM when converting. Using a power switch and output diode with larger current and power dissipation ratings should solve this issue of large peak currents. The designer has to use larger output capacitors, and take more effort on EMI/RFI solution too. The designer could make a choice for each mode. For a light load, DCM is preferred for a buck frame, but for a heavy load, CCM is preferred.

- **Buck (Step Down)**

The Buck or Step-down converter converts a DC voltage to a lower DC voltage. *Figure 1* shows the basic buck topology. When the switch SW is turned on, energy is stored in the inductor L and it has constant voltage "$V_L = V_I - V_O$", the inductor current *iL* ramps up at a slope determined by the input voltage. Diode D is off during this period. Once the switch, SW, turns off, diode D starts to conduct and the energy stored in the inductor is released to the load. The current in the inductor ramps down at a slope determined by the difference between the input and output voltages.

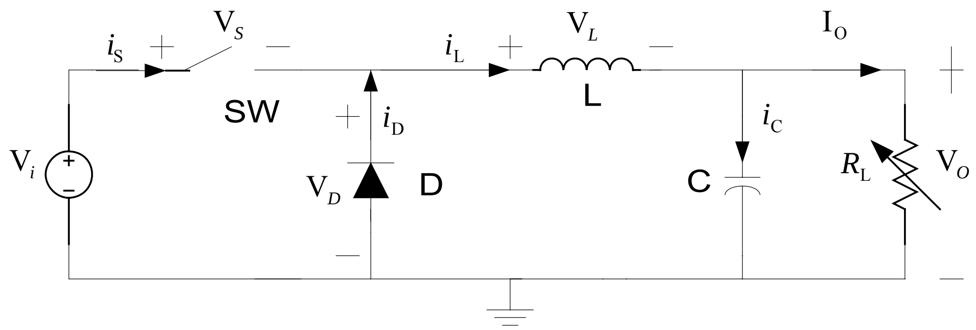


Figure 1. Typical Buck Converter Topology

2.3 Schematic

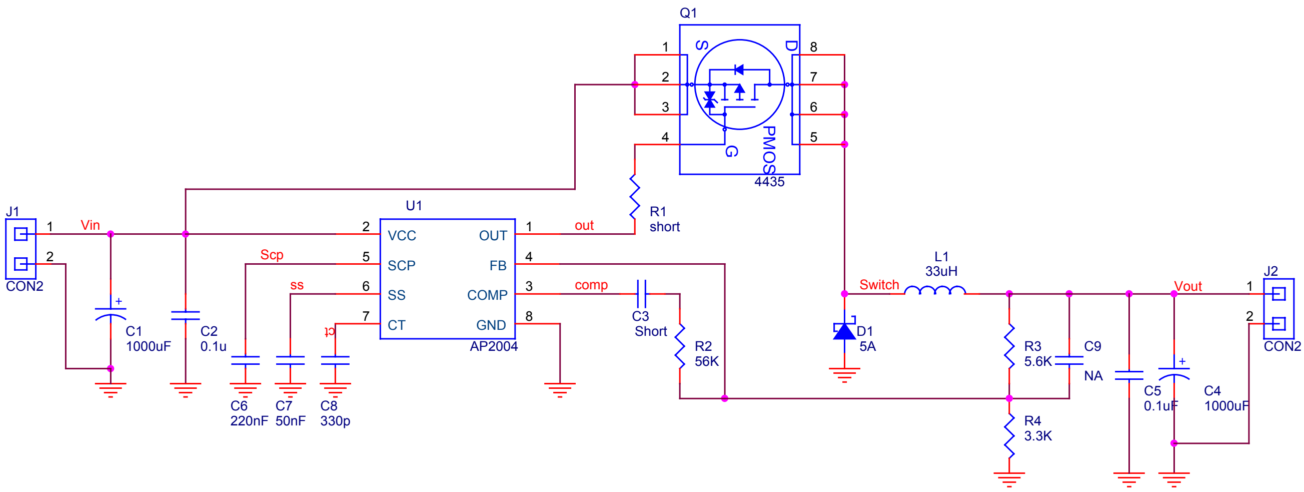


Figure 2. Demo board schematic

2.4 Board of Materials

Part Reference	Value	Description	Manufacturers	Part Number	Q'ty
U1	AP2004	PWM Buck Controller	Anachip	AP2004S	1
Q1	30V, 8.8A	PMOS	Fairchild	SI4435DY	1
D1	5A, 40V	Schottky Diode		B540A	1
R1	0Ω ±5%	Resister 0805			1
L1	33uH, 3A	Inductor	AXIS Power		1
R2	56KΩ ±1%	Resister 0805			1
R3	5.6KΩ ±1%	Resister 0805			1
R4	3.3KΩ ±1%	Resister 0805			1
C1	1000uF, 25V	Aluminum electrolytic	OST	OST RLX series	1
C2, C5	0.1uF, ±10%	Ceramic, 50V, 0805 X7R			2
C3	Short				1
C4	1000uF, 16V	Aluminum electrolytic	OST	OST RLX series	1
C6	220nF, ±10%	Ceramic, 50V, 0805 X7R			1
C7	50nF, ±10%	Ceramic, 50V, 0805 X7R			1
C8	330pF, ±10%	Ceramic, 50V, 0805 X7R			1
C9	NA	Option			
J1, J2	Pitch = 5.08mm, 3pin	Terminal Block			2

2.5 Board Layout

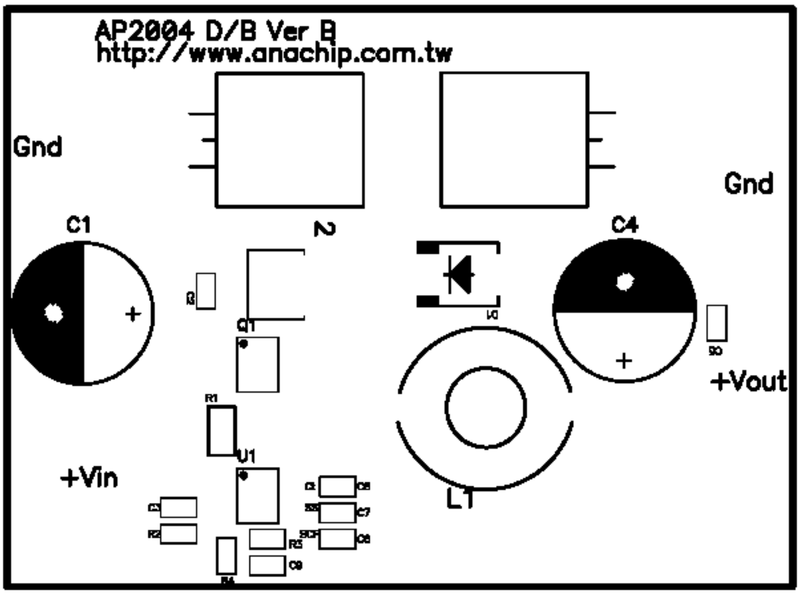


Figure 3. Silkscreen Layer

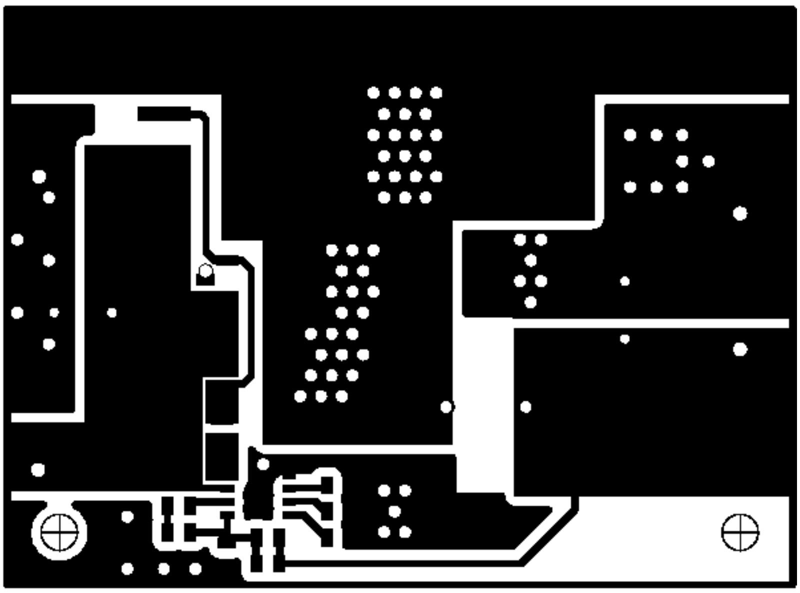


Figure 4. Top Layer

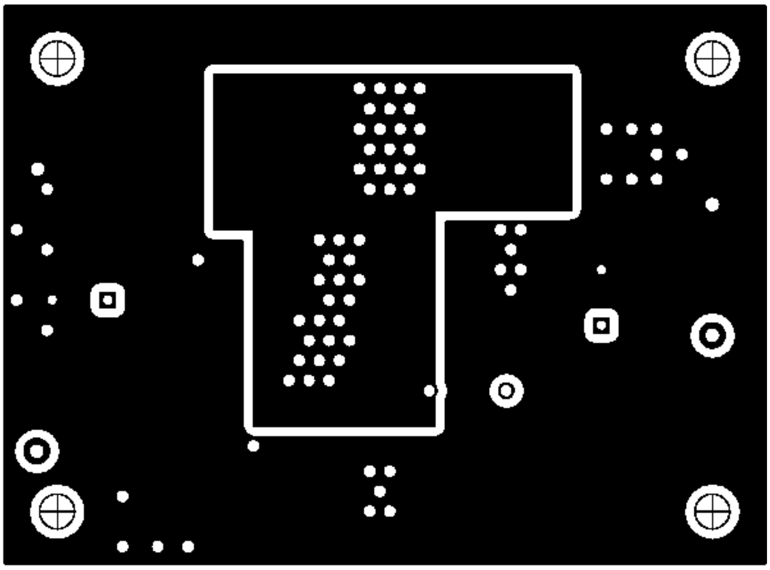


Figure 5. Bottom Layer

3. Design Procedure

3.1 Introduction

The AP2004 integrated circuit is a PWM controller, it operates over a wide input voltage range. This section will describe the AP2004 to design procedure. The operation and the design of the Buck converter will also be discussed in detail.

3.2 Operating Specifications

Specifications	Min.	Typ.	Max.	Units
Input Voltage Range	11.4	12	12.6	V
Output Voltage Range		3.3		V
Output Power Range	0	7	10	W
Output Current Range	0	2	3	A
Operating Frequency	194	215	263	kHz
Output Ripple		50		mV
Efficiency	82.34	84.9	84.6	%

Table 1. Operating Specifications

3.3 Design Procedures

This section describes the steps to design continuous-mode Buck converter, and explains how to construct basic power conversion circuits including the design of the control chip functions and the basic loop. A switching frequency of 215 kHz was chosen.

3.3.1 Buck converter

Example calculations accompany the design equations. Since this is a fixed output converter, all example calculations apply to the converter with output voltage of 3.3V and input voltage set to 12 V, unless specified otherwise. The first quantity to be determined is the duty cycle value.

$$\text{Duty cycle} = \frac{V_o + V_D}{V_{IN} - (I_O \times R_{DS(ON)}) + V_D} = \frac{T_{ON}}{T_S}, \quad 0 \le D \le 1$$

Assuming the commutating diode forward voltage V_D = 0.5 V, and the P-MOS $R_{DS(ON)}$ = 30mΩ

When V_{IN} = 12V , I_O = 0.3~3A , and the duty cycle is equal to 0.32.

3.3.1.1 Selection of the buck inductor (L)

A buck converter uses a single-stage LC filter. Choose an inductor to maintain continuous-mode operation down to 10 percent ($I_{o(min)}$) of the rated output load:

$$\Delta I_L = 2 \times 10\% \times I_o = 2 \times 0.1 \times 3 = 0.6A$$

The inductor value "L" is:

$$L \ge \frac{[\,V_{IN} - (I_O \times R_{DS(ON)}) - V_O\,] \times D}{\Delta I_L \times f_S} = \frac{\lfloor 12 - (0.3 \times 0.03\,) - 3.3 \rfloor \times 0.32}{0.6 \times 215 \times 10^3} = 22\mu H$$

So we can choose 33µH.

3.3.1.2 Selection of the output capacitor (C_{out})

Assuming that all of the inductor ripple current flows through the capacitor and the effective series resistance (ESR) is zero, the capacitance needed is:

$$C_{out} \ge \frac{\Delta I_L}{8 \times fs \times \Delta V_o} = \frac{0.6}{8 \times (215 \times 10^3) \times 0.05} = 7\mu F$$

Assuming the capacitance is very large, the ESR needed to limit the ripple to 50 mV is:

$$ESR \le \frac{\Delta V_o}{\Delta I_o} = \frac{0.05}{0.6} = 0.083\Omega$$

The output filter capacitor should be rated at least ten times the calculated capacitance and 30–50 percent lower than the calculated ESR. This design used a 1000µF/16V OS-Con capacitor in parallel with a ceramic to reduce ESR.

3.3.1.3 Selection of the power switch (MOSFET)

Based on the preliminary estimate, the $R_{DS(on)}$ of MOSFET is 30mΩ. The SI4435DY is a -30V p-channel MOSFET with $R_{DS(on)}$ = 35mΩ. Power dissipation (conduction + switching losses) can be estimated as:

$$P_{MOSFET} = I_o^2 \times R_{ds(on)} \times D_{max} + [0.5 \times V_{in} \times I_o \times (t_r + t_f) \times f_s]$$

Assuming total switching time (t_r + t_f) is 20 ns, a 55°C maximum ambient temperature, and thermal impedance $R_{\theta JA}$ = 50°C/W, thus:

$$P_{MOSFET} = (3 \times 3 \times 0.035 \times 0.32) + [0.5 \times 12 \times 3 \times (20 \times 10^{-9}) \times (215 \times 10^{3}) = 1.0854W$$

$$T_J = T_A + (R_{\theta JA} \times P_{MOSFET}) = 55 + (50 \times 1.0854) = 109.27°C$$

3.3.1.4 Selection of the Rectifier (D)

The catch rectifier conducts during the time interval when the MOSFET is off. The **B540A**(*DIODES*) is a 5A, 40V Schottky Rectifier in a SOP-8 package. The power dissipation is:

$$P_D = I_o \times V_d \times (1 – D_{min}) = 3 \times 0.5 \times (1 – 0.32) = 1.02W$$

Assuming a 55°C maximum ambient temperature, and thermal impedance $R_{\theta JA}$ = 15°C/W, thus:

$$T_J = T_A + (R_{\theta JA} \times P_D) = 55 + (15 \times 1.02) = 70.3°C$$

3.3.1.5 Selection of the input capacitor (C_{in})

The RMS current rating of the input capacitor can be calculated from the following formula. The capacitor manufacturer's datasheet must be checked to assure that this current rating is not exceeded.

$I_{in(rms)} = \sqrt{[D \times (I_{o(max)} + I_{o(min)}) \times (I_{o(max)} - I_{o(min)}) + (\Delta I_L^2)/3]} = \sqrt{[0.32 \times (3 + 0.3) \times (3 – 0.3) + 0.36/3]} = 1.72A$

This capacitor should be located close to the IC using short leads and the voltage rating should be approximately 2 times the Maximum Input Voltage. The input capacitor value is "1000uF/25V".