

## ZXGD3103EV1 EVALUATION BOARD USER GUIDE

### Description

This document describes how to connect and evaluate the ZXGD3103EV1 evaluation board shown in Figure 1. The purpose of this board is to demonstrate the driving of a synchronous MOSFET as a Schottky/ultra-fast recovery diode replacement in high efficiency power converters. End applications include offline Flyback converter, resonant LLC converters, asymmetrical half-bridge converters etc. . When the board is used to drive a synchronous MOSFET, it will yield efficiency improvement, whilst maintaining design simplicity and incurring minimal component count. The ZXGD3103 senses the voltage across the MOSFET and generates the gate drive voltage when a negative voltage is detected across the drain-source pin.

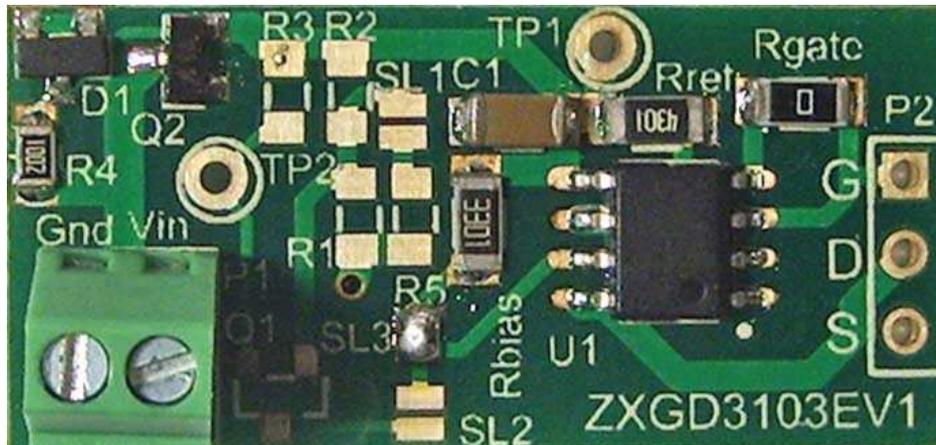


Figure 1 Evaluation board layout and connection diagram

### Evaluation board design

The circuit schematic of the ZXGD3103EV1 is shown in Figure 2. The evaluation board will work with VIN voltage of up to 40V. Power, which could be sourced directly from the output of the power supply, is applied to the terminal block P1. At the other end of the board is a location for a three way header, P2. This is not fitted, so as to allow flexibility of mounting (forward or reverse). The purpose of the header is to allow the board to be soldered directly across a TO220 packaged MOSFET. The board can be used with surface mounted MOSFET as well by connecting the pin-outs accordingly.

R4, Q2, D1 and C1 are configured as a simple series regulator to maintain a stable Vcc around 10V. The circuit is required to support VIN voltage of up to 40V. The values of Rref and Rbias in Figure 2 are suggested for Vcc around 10V. Please refer to the device datasheet for more information on selection of Rref and Rbias.

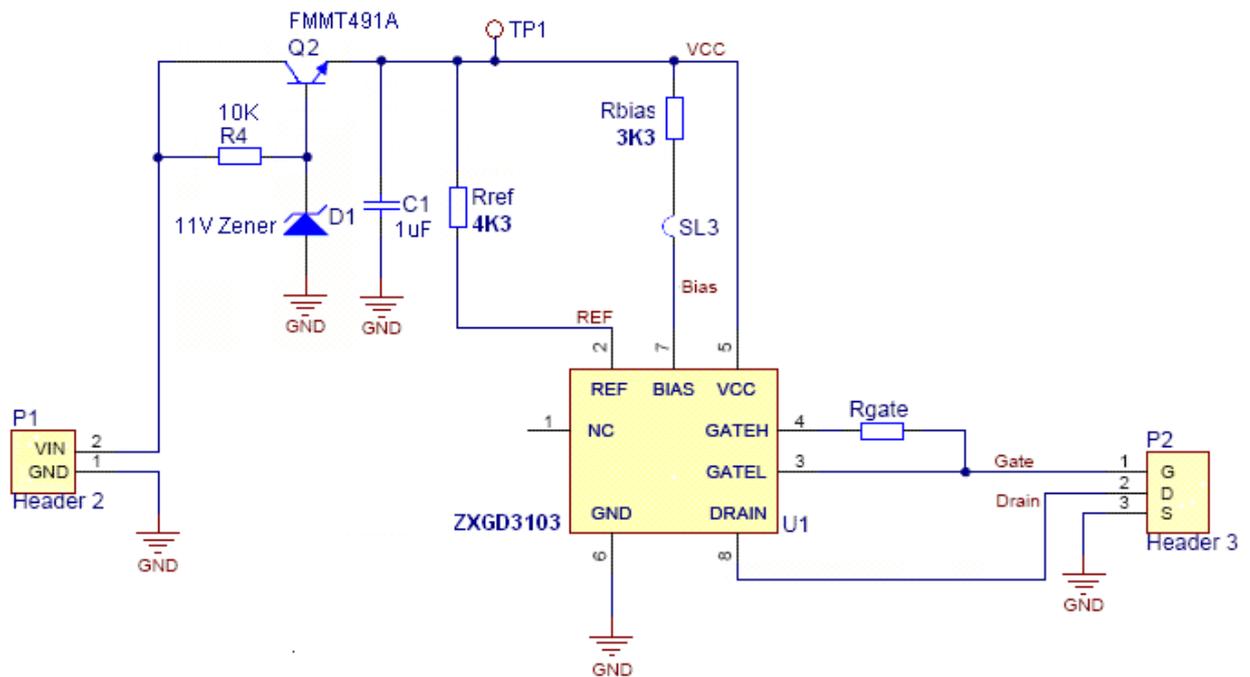


Figure 2: Evaluation board schematic diagram and connection

Please note that the component part numbers are given as a guide only. Due to continual component development, all parts quoted should be checked for suitability and availability with their respective manufacturers.

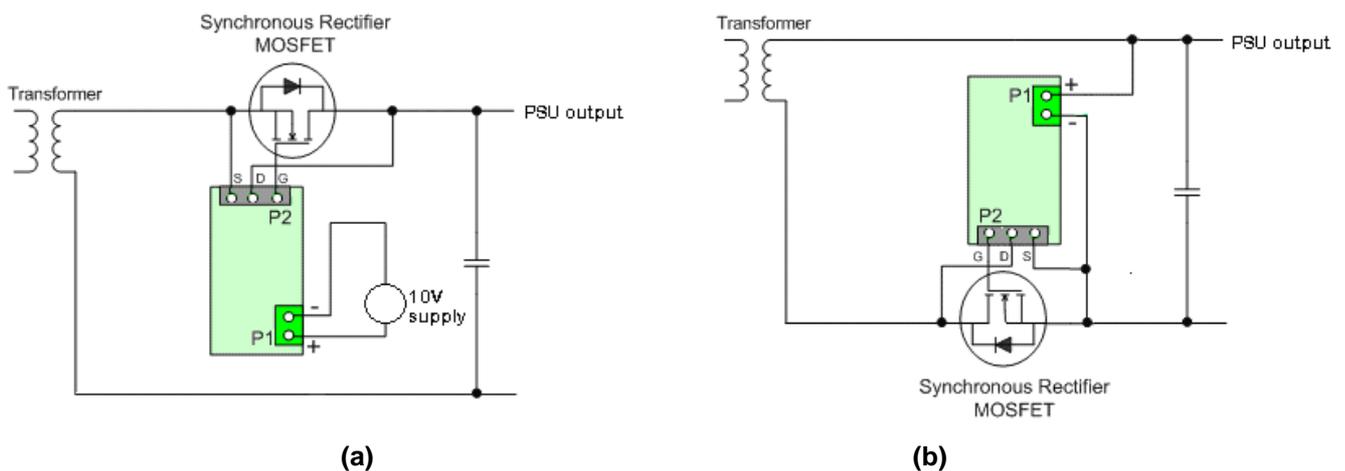
Table 1: Evaluation board component details (BOM)

Ref.	Value	Package	Part number	Manufacturer	Notes
U1	ZXGD3103	SO8	ZXGD3103N8	Diodes Inc.	
Q2	FMMT491A	SOT23	FMMT491A	Diodes Inc.	500mW
D1	11V Zener	SOT23	BZX84C11	Diodes Inc.	300mW
C1	1uF 50V	1206	C1206X105K5RAC	Kemet	X7R
P1	2-way terminal				
P2	3-way header				
R4	10kΩ	0805	Generic		125mW, 1%
Rbias	3.3kΩ	1206	Generic		5%, 200ppm/°C
Rgate	0R	1206	Generic		5%, 200ppm/°C
Rref	4.3KΩ	1206	Generic		5%, 200ppm/°C

## Evaluation procedure and operation

To perform a quick functional test of the ZXGD3103, the evaluation board can be used to drive a MOSFET in a high-side-configuration (see Fig. 3a), as the board can be floated to any potential. In practice, the supply voltage could be derived from an auxiliary supply winding across the transformer secondary. If the board is used for comparison against an existing synchronous rectification solution, the original controller must be disabled before proceeding with the testing.

The recommended device implementation is low side synchronous rectification (Fig. 3b), due to the ease of acquiring the supply voltage to the board directly from the output of the power supply under evaluation. Before doing the test, it is important that the incumbent diode has been removed and/or a short has been applied across its cathode and anode terminals. The track linking the negative terminal of the converter's output capacitor to the transformer secondary-side output should then be cut, and a MOSFET should be inserted. It is recommended that the selected MOSFET should drop between 50 to 150mV at the peak of the secondary-side current at full load. The breakdown voltage of the MOSFET must be higher than the maximum drain-source voltage stress, plus some margin. Designers interested in squeezing the last percent of efficiency out of the module can place an additional Schottky or Ultra-fast-recovery diode in parallel with MOSFET. The diode prevents body-diode conduction, so the trace inductance between it and the MOSFET should be kept small to create an efficient circulating energy flow path.



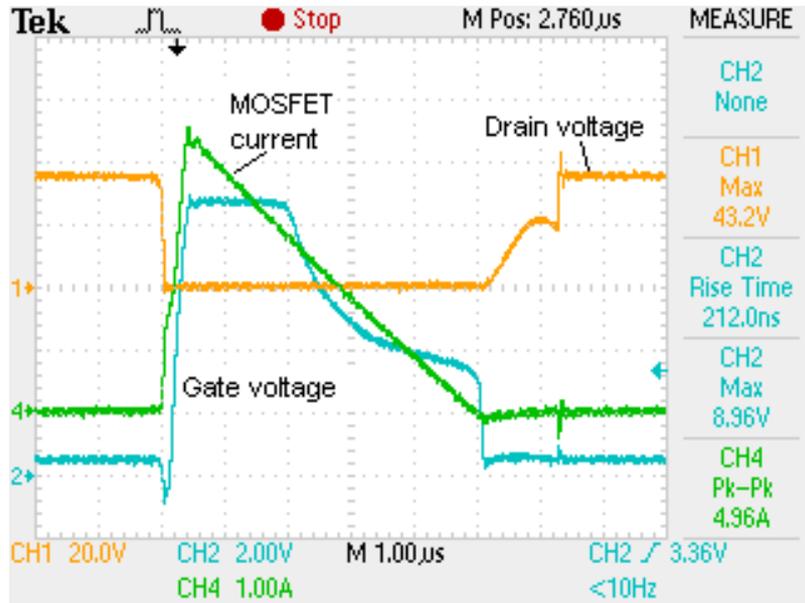
**Figure 3: Test options for ZXGD3103EV1 a) high side and b) low side**

The operating waveforms of the controller can be probed using an oscilloscope probe with a minimal length for the ground pin. If a current probe or transformer is used to measure the MOSFET current, minimal wire length should be used to avoid excessive wire-loop inductance and injection of noise, which could disturb normal functioning of the controller.

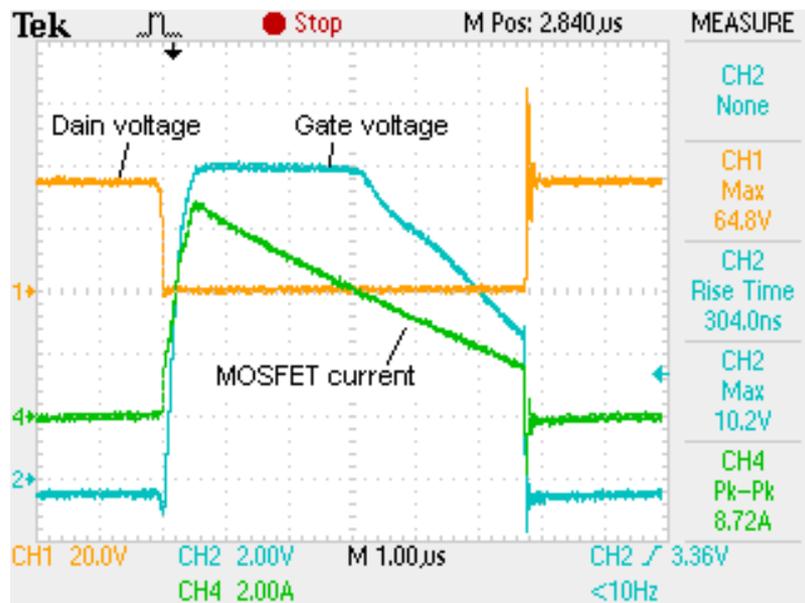
Figure 4 gives an illustration of typical device operation in a Flyback converter. The ZXGD3103 senses the forward voltage drop of the parasitic diode within the MOSFET, and when the diode is in conduction applies a voltage to the MOSFET gate, turning on the MOSFET after an initial 80ns delay.

The gate drive voltage of the ZXGD3103 is proportional to the sensed voltage. In DCM and CrCM operation, as the drain current through the MOSFET decreases, the voltage drive to the MOSFET gate is reduced, thereby minimizing turn-off time. This ensures that the MOSFET is turned off precisely when the sinusoidal current goes to zero, with little or no reverse current, see Figure 4a. Another advantage of this technique is it prevents early termination of the gate drive voltage. With the early termination of the gate drive voltage, MOSFET turns off and the parasitic diode conducts. As current flows through the parasitic diode for the remaining of the cycle, there will be an increase in power developed within the MOSFET.

In continuous conduction mode of operation, the synchronous MOSFET current will not decay to zero prior to the primary MOSFET's turn-on. The ZXGD3103 turns off the synchronous MOSFET quickly when the primary MOSFET current starts to rise, as shown in Fig. 4b, so the possibility of cross conduction is minimized. This is critical because cross conduction due to the primary side MOSFET and secondary side MOSFET conducting simultaneously will degrade power supply efficiency.



(a)

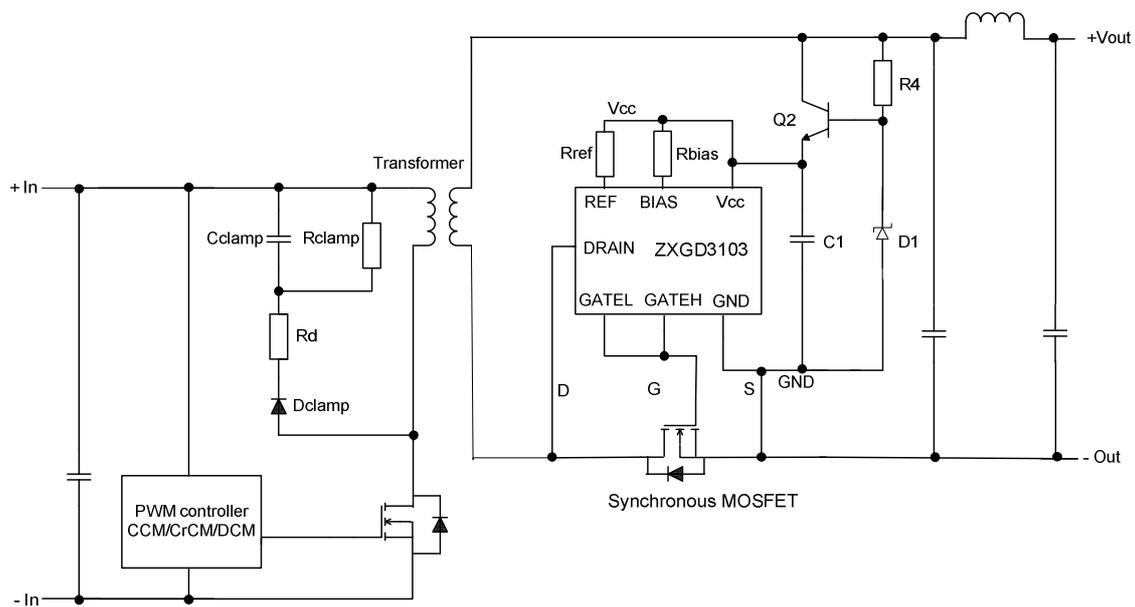


(b)

Figure 4: Synchronous rectification operating waveforms (a) Proportional gate voltage as current reduces in DCM mode and (b) CCM mode

## Conditioning the power supply to maximize efficiency of ZXGD3103

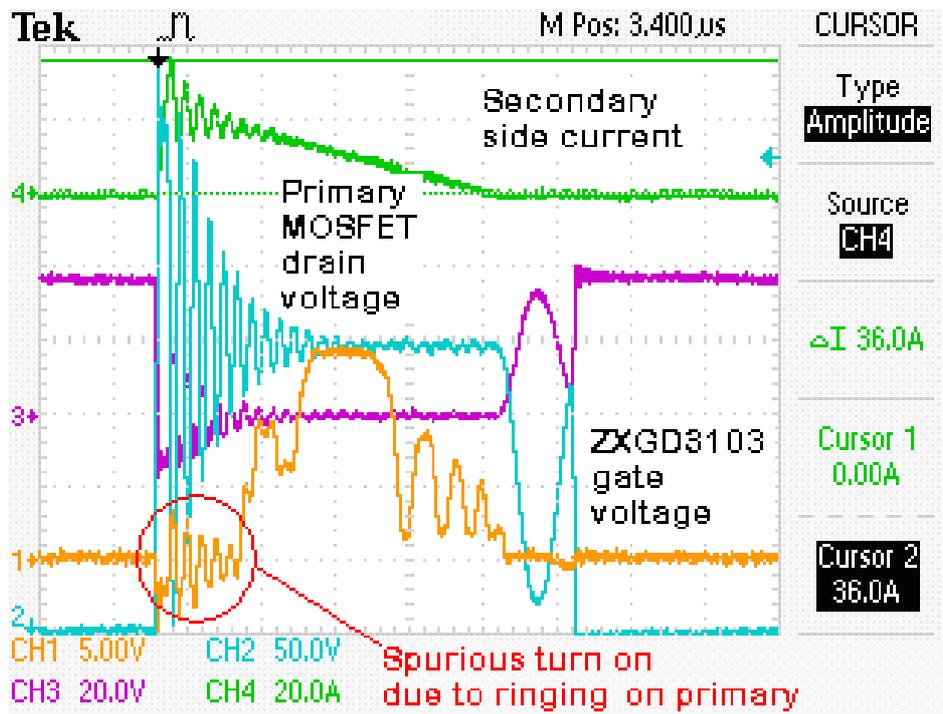
In a Flyback converter, the ZXGD3103 could be susceptible to noise if a proper snubbing circuit on the primary side is not devised. Any high-frequency-resonance-ringing on the Drain of the primary MOSFET during the turn-off transition will be reflected across the transformer as oscillation on the synchronous MOSFET drain, which could trigger spurious turn-on of the device. The ZXGD3103 will not be able to fully enhance the MOSFET until the oscillation stabilizes. To circumvent this, the user is advised to strengthen the primary switch snubber circuit through either a damping resistor  $R_d$  (see Fig. 5) or alternatively an additional snubbing R-C network. These have the effects of eliminating the oscillations by limiting the peak clamp diode's reverse recovery current and soften the recovery characteristic. The improvement on the rising edge of the gate drive can be observed as in Figure 6.



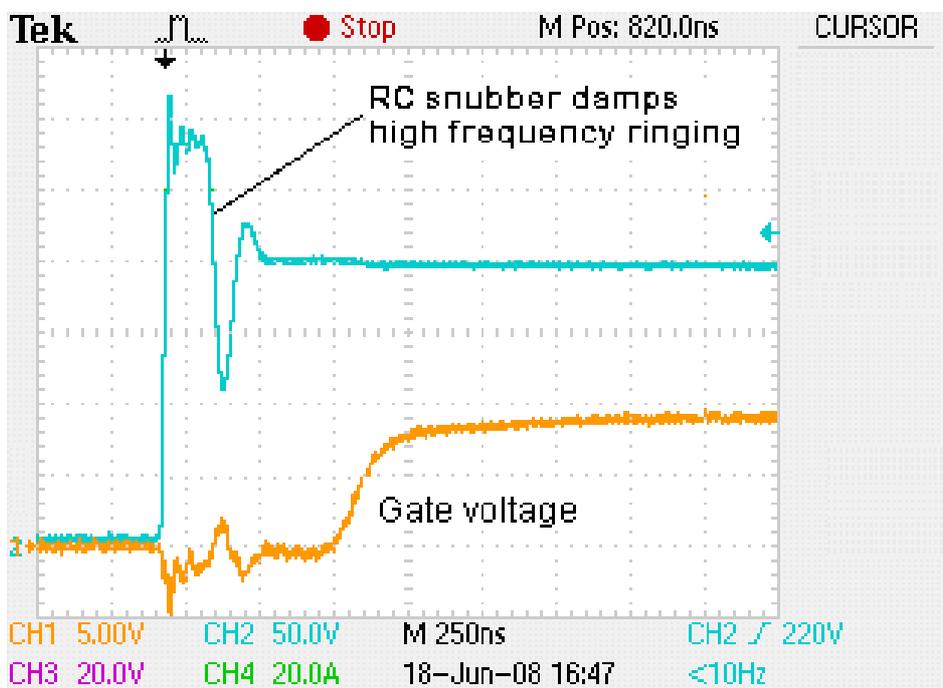
**Figure 5: Recommended design for a synchronous rectified Flyback converter**

Another snubber network comprising of  $R_{snub}$  and  $C_{snub}$  should be fitted across the synchronous MOSFET to dampen out high frequency oscillations at the turn on edge of the MOSFET's. If the amplitude of oscillations is high, then the drain voltage could ring below the turn-on threshold. The controller could then be falsely triggered and provide an output high to drive the MOSFET gate. Apart from preventing premature turn-on of the controller, this also has the added benefit of reducing conducted EMI generation and device voltage stress.

Furthermore, any parasitic inductance due to a combination of printed circuit board traces and component leads can also cause the voltage at the drain input of the ZXGD3103 to ring about ground. Proper layout attention must be paid to ensure the integrity of the  $V_{SD}$  differential voltage. To mitigate noise induced malfunction, it is important to keep the drain input on the controller as close as possible to the synchronous MOSFET, preferably within 10mm. A minimal gate drive loop will also negate the effect of loop inductance inducing oscillation to the controller's output gate drive voltage, reducing the requirement for series gate resistor damping.



(a)



(b)

Figure 6: Oscillation-induced spurious turn on reduces efficiency of synchronous rectification  
 (a) Oscillation due to clamp diode recovery (b) Improved clamp circuit

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**Sales offices****The Americas**

3050 E. Hillcrest Drive  
Westlake Village,  
CA 91362-3154  
Tel: (+1) 805 446 4800  
Fax: (+1) 805 446 4850

**Europe**

Kustermannpark  
Balanstraße 59,  
D-81541 München  
Germany  
Tel: (+49) 894 549 490  
Fax: (+49) 894 549 4949

**Taiwan**

7F, No. 50,  
Min Chuan Road  
Hsin-Tien  
Taipei, Taiwan  
Tel: (+886) 289 146 000  
Fax: (+886) 289 146 639

**Shanghai**

Rm. 606, No.1158  
Changning Road  
Shanghai, China  
Tel: (+86) 215 241 4882  
Fax (+86) 215 241 4891

**Shenzhen**

Room A1103-04,  
ANLIAN Plaza, #4018  
Jintian Road  
Futian CBD,  
Shenzhen, China  
Tel: (+86) 755 882 849 88  
Fax: (+86) 755 882 849 99

**Korea**

6 Floor, Changhwa B/D,  
1005-5 Yeongtong-dong,  
Yeongtong-gu, Suwon-si,  
Gyeonggi-do, Korea 443-813  
Tel: (+82) 312 731 884  
Fax: (+82) 312 731 885