Table of Contents

Chapter 1 Summary 3

1.1 General Description 3

1.2 Key Features 3

1.2.1 System Key Features 3
1.2.2 AP33510 Key Features 3
1.2.3 APR349 Key Features 3
1.2.4 AP43771V Key Feature 3

1.3 Applications 3

1.4 Main Power Specifications 3

1.5 Evaluation Board Pictures 4

Chapter 2 Power Supply Specification 5

2.1 Specification and Test Results 5

2.2 Compliance 5

Chapter 3 Schematic 6

3.1 Board Schematic 6

3.2 Bill of Material (BOM) 7

3.3 Transformer Design 9

3.4 Schematics Description 10

3.4.1 AC Input Circuit & Differential Filter 10
3.4.2 AP33510 PWM Controller 10
3.4.3 APR349 Synchronous Rectification (SR) MOSFET Driver 10
3.4.4 AP43771V PD 3.0 Decoder & Protection on/off N MOSFET and Interface to Power Devices 10

Chapter 4 The Evaluation Board (EVB) Connections 11

4.1 EVB PCB Layout 11

4.2 Quick Start Guide before Connection 13

4.3 Connection with E-Load 14

Chapter 5 Testing the Evaluation Board 15

5.1 Input & Output Characteristics 15

5.1.1 Input Standby Power 15
5.1.2 Multiple Output Full Load Efficiency at Different AC Line Input Voltage 15
5.1.3 Multiple Output Average Efficiency at Different Loading 16
5.1.4 PD3.0 & PPS Compatible Mode Testing 18

5.2 Key Performance Waveforms 18

5.2.1 65W PD3.0 System Start-up Time 18
5.2.2 Q1 / Q2 MOSFET Voltage Stress at Full Load @264Vac 19
5.2.3 System Output Ripple & Noise with the Cable 19
Connect 47uF AL Cap and 104MLCC to the cable output unit in parallel 19

5.2.4 Dynamic load ----0% Load~100% Load, T=20mS, Rate=15mA/uS (PCB End) 21
5.2.5 Output Voltage Transition Time from Low to High 22
5.2.6 Output Voltage Transition Time from High to Low 23
5.2.7 Thermal Testing 25

5.3 EMI (Conduction) Testing 26

Chapter 1 Summary

1.1 General Description

The 65W 52CC PD3.0 PPS Evaluation Board (EVB3) is composed of three main controllers, AP33510, APR349 and AP43771V. The AP33510, a highly integrated Quasi-Resonant (QR) controller with direct Enhancement Gallium Nitride (E-GaN) driver integration, is optimally designed to meet ultra-low standby power and high power density (HPD) charger applications. The APR349, a secondary side Synchronous Rectification (SR) Controller, is adopted for efficiency optimization. The AP43771V, a PD3.0 PPS protocol controller, automatically manages the PD3.0 PPS attachment process for the attached Type C-equipped Device Under Charged (DUC), regulates the feedback information of the charger to fulfill voltage and current requirements from DUC. By adopting growing popularity of E-GaN FETs, the 65W 52CC EVB3 exemplifies HPD charger design with system BOM optimization to meet market trend.

1.2 Key Features

1.2.1 System Key Features

- Quasi-Resonant operation for Critical E-GaN switch Operation and Efficiency Improvement Approaches
- Cost-Effective Implementation for HPD Chargers
- High-Voltage Startup low standby power (<20mW)
- Meets DOE VI and COC Tier 2 Efficiency Requirements
- USB Type-C Port - Support the Maximum Output of 65W PD3.0 PPS (3.3V to 21V@20mV/step, 50mA/step)
- SSR Topology Implementation with an Opto-coupler for Accurate Step Voltage / Current Control
- Low overall system BOM cost

1.2.2 AP33510 Key Features

- QR Flyback Topology with Valley-on and Valley lock
- High-Voltage Startup
- Embedded VCC LDO for VCCIN pin to Guarantee Wide Range Output Voltage
- Integration of Accurate E-GaN direct-driver
- Low Constant Output Current for Output Short
- Non-Audible-Noise QR Control
- Soft Start During Startup Process
- Frequency Fold Back for High Average Efficiency
- Secondary Winding Short Protection with FOCP
- Frequency Dithering for Reducing EMI
- Integration of X-CAP Discharge Function
- Useful Pin fault protection:
  SENSE Pin Floating Protection/
  FB/Opto-Coupler Open/Short Protection
- Comprehensive System Protection Feature:
  VOVP/OLP/BNO/SOVP/SUVP

1.2.3 APR349 Key Features

- SR Works with CCM / DCM / QR operation modes
- Eliminate Resonant Ringing Interference
- Fewest External Components used

1.2.4 AP43771V Key Feature

- Support USB PD Rev 3.0 V1.2
- USB-IF PD3.0/PPS Certified TID 4312
- Qualcomm QC5 Certified: QC20201127203
- MTP for System Configuration
- OTP for Main Firmware
- Operating Voltage Range: 3.3V to 21V
- Built-In Regulator for CV and CC Control
- Programmable OVP/UVP/OCP/OTP
- Support Power Saving Mode
- External N -MOSFET Control for VBUS Power Delivery
- Support e-Marker Cable Detection
- QFN-14 and QFN-24

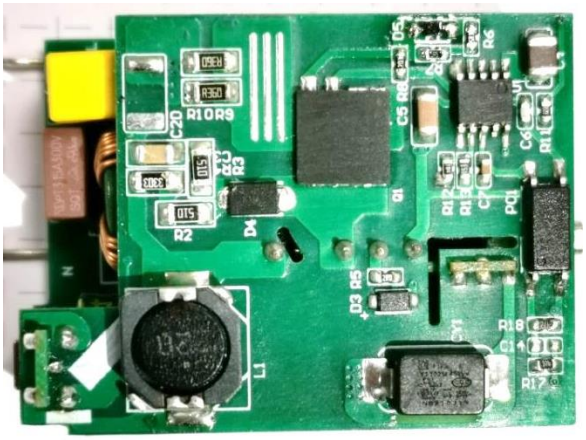
1.3 Applications

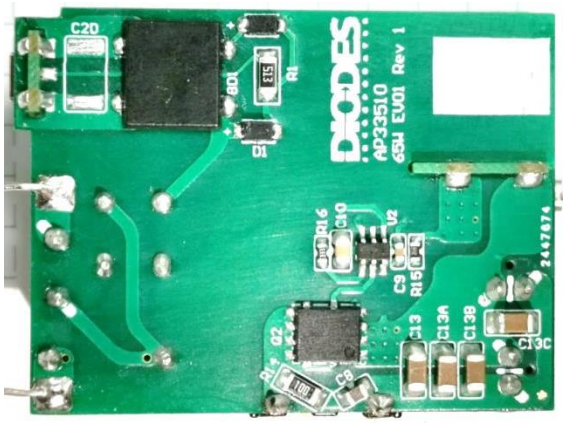
- Quick Charger with full power range of PD3.0 PPS

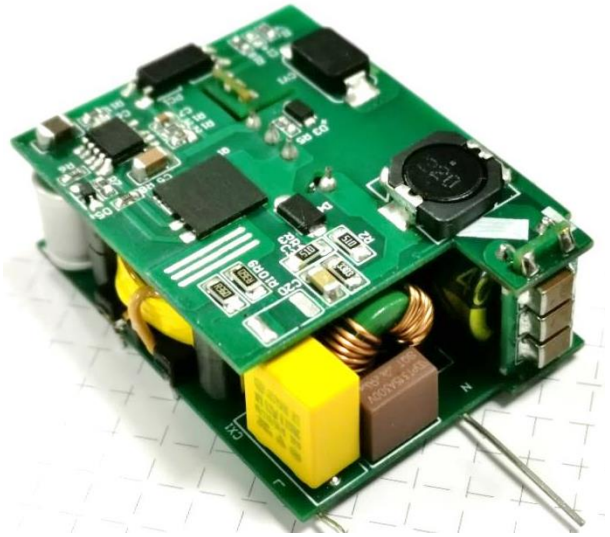
1.4 Main Power Specifications

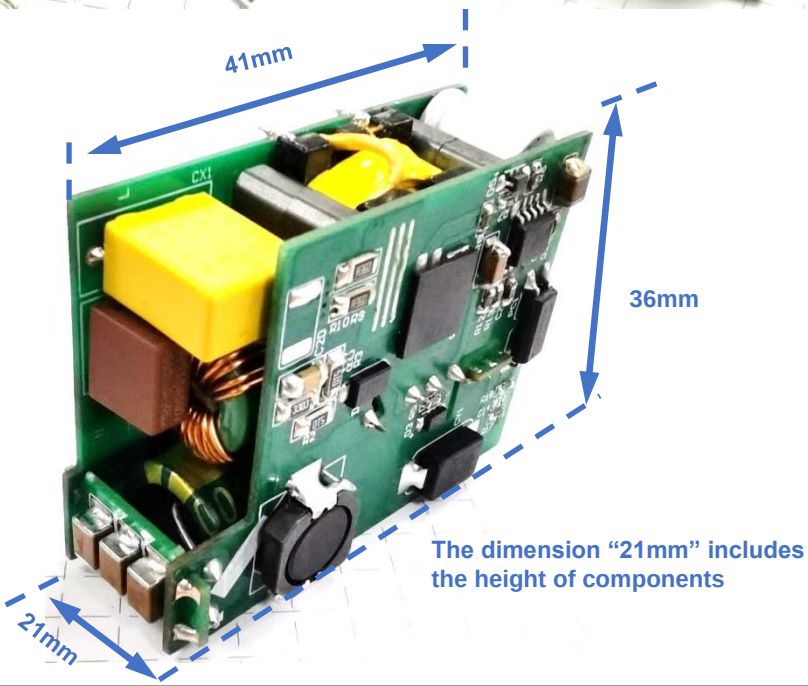
Parameter	Value
Input Voltage	$90V_{AC}$ to $264V_{AC}$
Input standby power	< 30mW
Main Output (Vo / Io)	PDO: 5V/3A, 9V/3A, 15V/3A, 20V/3.25A,
	APDO: 3.3V to 21V/3A
Voltage Step	PPS 20mV step voltage, 3.3V-21V
Efficiency	Comply with CoC version 5 tier-2
Total Output Power	65W (at PDO 20V/3.25A)
Protections	OCP, OVP, UVP, OLP, OTP, SCP
Dimensions	PCB: 36 * 48 * 21 mm^3, 1.417" * 1.89" * 0.827" $inch^3$ Case: 40 * 52 * 25 mm^3, 52CC, 3.17 CI
Power Density Index	1.25 W/CC; 20.48 W/CI

1.5 Evaluation Board Pictures









Chapter 2 Power Supply Specification

2.1 Specification and Test Results

Parameter	Value	Test Summary
Input Voltage / Frequency	90V_{AC} to 264V_{AC} / 50Hz or 60Hz	Test Condition
Input Current	<2A_{RMS}	
Standby Power	< 30mW, load disconnected	**PASS,** 28mW@230V_{AC}/50Hz
5V/3A Average Efficiency	CoC Version 5, Tier-2 Efficiency >81.84%	**PASS,** 91.82@115VAC/60Hz 89.37@230VAC/50Hz
5V/0.3A Efficiency (10% Load)	CoC Version 5, Tier2 Efficiency >72.48%	**PASS,** 89.93@115VAC/60Hz 87.74@230VAC/50Hz
9V/3A Average Efficiency	CoC Version 5,Tier2 Efficiency >87.30%	**PASS,** 92.97@115VAC/60Hz 91.30@230VAC/50Hz
9V/0.3A Efficiency (10% Load)	CoC Version 5,Tier2 Efficiency >77.30%	**PASS,** 91.67@115VAC/60Hz 87.94@230VAC/50Hz
15V/3A Average Efficiency	CoC Version 5,Tier2 Efficiency >88.85%	**PASS,** 93.09@115VAC/60Hz 92.15@230VAC/50Hz
15V/0.3A Efficiency (10% Load)	CoC Version 5,Tier2 Efficiency >78.85%	**PASS,** 90.27@115VAC/60Hz 86.97@230VAC/50Hz
20V/3.25A Average Efficiency	CoC Version 5,Tier2 Efficiency >89%	**PASS,** 92.81@115VAC/60Hz 92.48@230VAC/50Hz
20V/0.325A Efficiency (10% Load)	CoC Version 5,Tier2 Efficiency >79%	**PASS,** 90.12@115VAC/60Hz 87.24@230VAC/50Hz
Output Voltage Regulation Tolerance	+/- 5%	**PASS,**
16V PPS	3.3V – 16V +/- 5%, 0~2.8A +/-150mA	**PASS,**
21V PPS	3.3V – 21V +/- 5%, 0~2.1A +/-150mA	**PASS,**
Conducted EMI	>5dB Margin; according to EN55032 Class B	

2.2 Compliance

Parameter	Test conditions	Low to High	High to Low	standard	Test Summary
Output Voltage Transition time	5V/3A to 9V/3A, 90Vac/60Hz	59.49ms	63.51ms	275ms <	Pass
	5V/3A to 9V/3A, 264Vac/50Hz	57.59ms	61.96ms		Pass
	9V/3A to 12V/3A, 90Vac/60Hz	50.08ms	46.55ms		Pass
	9V/3A to 12V/3A, 2640Vac/50Hz	48.51ms	48.22ms		Pass
	12V/3A to 15V/3A, 2640Vac/50Hz	47.01ms	47.82ms		Pass
	12V/3A to 15V/3A, 2640Vac/50Hz	46.72ms	48.18ms		Pass
	15V/3A to 20V/3A, 90Vac/60Hz	76.51ms	70.83ms		Pass
	15V/3A to 20V/3A, 264Vac/50Hz	74.09ms	71.87ms		Pass
Output Connector	USB Type-C *1-				
Temperature	90Vac , Full Load				
Dimensions (W /D/ H)	L46mm x46mm x 22mm (with foldable AC pin)				

Chapter 3 Schematic

3.1 Board Schematic

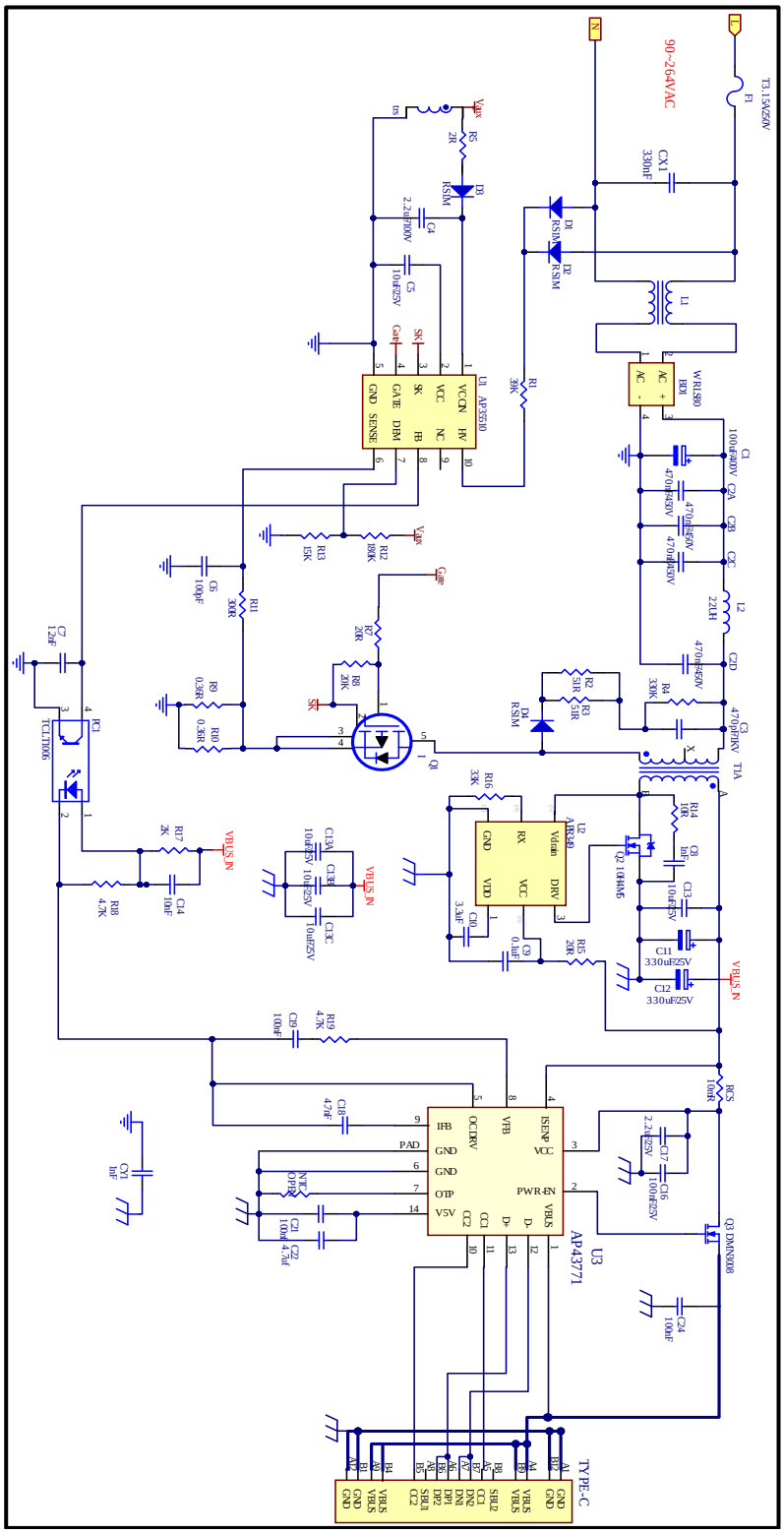


Figure 3: 65W PD3.0 PPS Adapter EVB3 Schematic

3.2 Bill of Material (BOM)

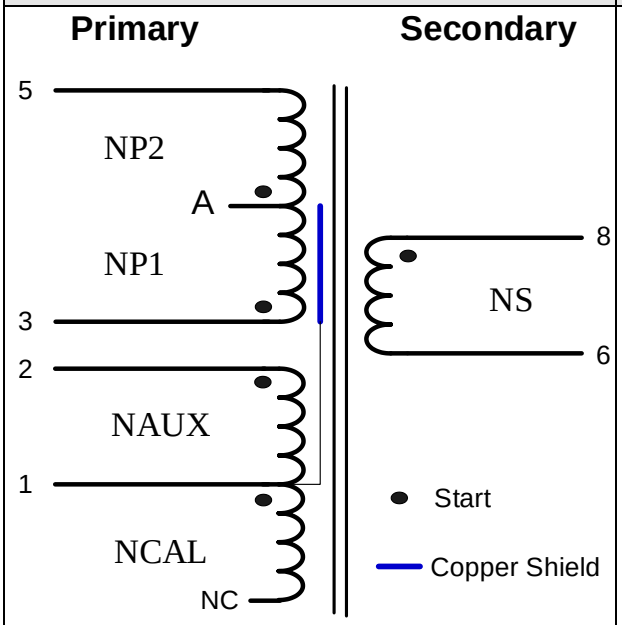
Item	Quantity	Reference	Description	Manufacturer Part Number	Manufacturer
1	**1**	**U1**	**AP33510, Quasi-Resonant Flyback Controller**	**AP33510**	**Diodes Inc.**
2	**1**	**U2**	**APR349, SR Controller**	**APR349**	**Diodes Inc.**
3	**1**	**U3**	**AP43771V, Decoder IC**	**AP43771VFBZ-13**	**Diodes Inc.**
4	**1**	**Q2**	**MOSFET, N-CH, 100V, POWERDI5060-8, DMTH10H4M5LPS**	**DMTH10H4M5LPS**	**Diodes Inc.**
5	**1**	**Q3**	**MOSFET, N-CH, 30V, POWERDI3333-8, DMN3008SFG-13**	**DMN3008SFG-13**	**Diodes Inc.**
6	**4**	**D1,D2, D3,4**	**Fast Rectifier, 1A, 1000V, SOD-123, RS1MWF**	**RS1MWF-7**	**Diodes Inc.**
8	1	Q1	Primary GaN Switch, 650V, DFN 8X8, 260mOhm	INN650D260A*Note	InnoScience
10	1	BD1	Bridge 8A 700V WRLSB80M	WRLSB80M	WRL(沃尔德)
11	1	C1	EC 100uF 400V 12.5x42	SD400M101I40TA09S00R	Su'scon (冠坤)
12	3	C2A, C2B, C2C	MLCC 470nF 450V 1812 X7R C4532X7T2W474K230KE	C4532X7T2W474K230KE	TDK
13	1	C3	MLCC 470pF 1000V 1206 X7R		
13	1	C4	MLCC 2.2uF 100V 1206 X7R		
14	1	C5	MLCC 10uF 25V 0805 X7R		
15	1	C6	MLCC 100pF 16V 0603 X7R		
	1	C7	MLCC 1.2nF 16V 0603 X7R		
16	1	C8	MLCC 1nF 100V 0805 X7R		
17	1	C9	MLCC 100nF 16V 0603 X7R		
	1	C10	MLCC 3.3uF 16V 0603 X7R		
18	2	C11, C12	EC 330uF 25V 6.3x12 polymer		
19	4	C13, C13A, C13B, C13C	MLCC 10uF 25V 1206 X7R		
20	1	C14	MLCC 10nF 16V 0603 X7R		
21	4	C16, C19, C21, C24	MLCC 100nF 50V 0603 X7R		
22	1	C17	MLCC 2.2uF 50V 0805 X7R		
23	1	C18	MLCC 4.7nF 50V 0603 X7R		
	1	C22	MLCC 4.7uF 10V 0805 X7R		
27	1	CX1	X2 0.22uF AC275V 13mm x 12.5mm x 6mm lead space 10mm		TENTA
28	1	CY1	Y1 1000pF AC300V	SMDDK1E3EA102M86RBH01	MuRata
29	1	F1	Fuse T3.15A 250V Time Lag	40013150000	Littlefuse
31	1	L2	Inductor 22uH	7447713220	Wurth Elektronik
32	1	NTC	NTC 100K 0603	NTCG103JF103FT1S	TDK
33	1	PC1	Optocoupler	TLV-1009	LITE ON
	1	R1	RES 39K 0603 5%		

34	1	R2,3	RES 510R 0603 5%		
35	1	R4	RES 330K 0805 5%		
36	3	R5	RES 2R 0603 5%		
37	1	R6	RES 5.1R 0603 5%		
38	1	R7	RES 20R 0603 5%		
39	1	R8	RES 20K 0603 5%		
40	1	R9,10	RES 360mR 1206 1% 250mW, 0.36Ohm		
41	1	R11	RES 300R 0603 5%		
42	1	R12	RES 180K 0603 1%		
43	1	R13	RES 15K 0603 1%		
44	2	R14	RES 10R 1206 5%		
45	1	R15	RES 20R 0603 5%		
46	1	RCS	RES 10mR 1206 1% Low CTR type		
47	1	T1	ATQ23/12.3 280uH		

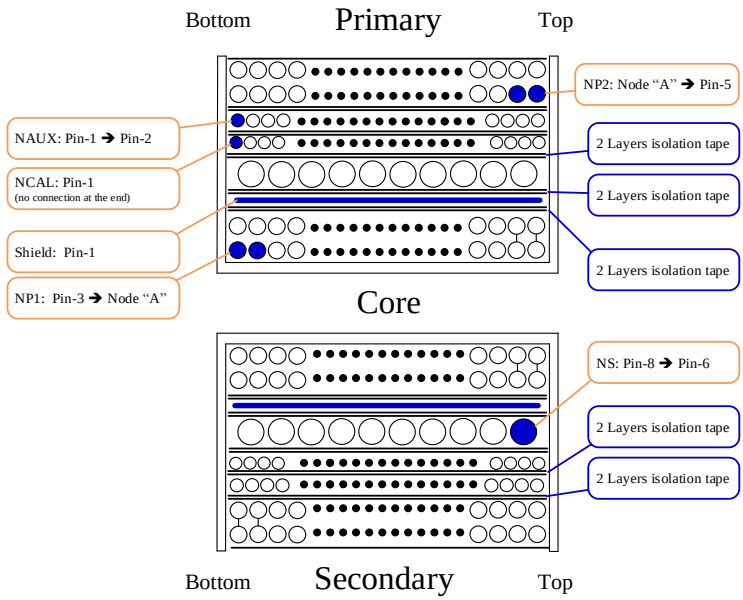
* Note: GaN device spec can find in InnoScience website http://www.innoscience.com.cn/

3.3 Transformer Design

Schematic

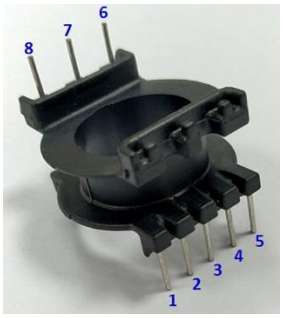


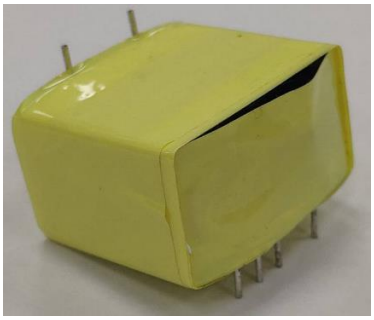
Structure



Definition	Pin define (Start >> End)	Wire (φ)	No. of Turns	Layers	Layers of Tape
NP1	3 → Node A	2UEW Litz Wire, 0.1mmx15, 1P, Bot -> Top -> Bot	16	2	1 L
Shield	1 → NC	5mm width copper shielding, solder to pin-1.	1	1	1 L
NS	8 → 6	TRW(B), Triple Insulated Litz Wire 0.25x7, 1P	5	1	1 L
NCAL	1 → NC	2UEW, 0.13, 1P	20	1	1 L
NAUX	2 → 1	2UEW, 0.13, 2P	12	1	1 L
NP2	Node A → 5	2UEW Litz Wire, 0.1mmx15, 1P, Bot -> Top -> Bot	14	2	2L

BOBBIN PIN Define:





Item	Test Condition	Rating
Primary Inductance	Pin 3-5,all other windings open, measured at 100kHz / 1V	280uH+/- 5%
Note	Bobbin: 裕龍鑫科技, ATQ2327 Core： A-Core(安磁), ATQ-23/12.3 (JPP-96F)	

3.4 Schematics Description

3.4.1 AC Input Circuit & Differential Filter

The Fuse F1 protects against over-current conditions which occur when some main components fails. The NF1 and NF2 are common mode chocks for the common mode noise suppression. The BD is a bridge rectifier which converts alternating current and voltage into direct current and voltage. The CE1~CE4, L1, CE5~CE6 are composed of the Pi filter for filtering the differential switching noise back to AC source.

3.4.2 AP33510 PWM Controller

AP33510, a highly integrated Quasi Resonant Flyback (QR) controller, integrates high-voltage start-up function through HV pin and X-Cap discharging function. It also integrates a VCC LDO circuit, which allows the LDO to regulate the wide range VCCL to an acceptable value. This makes the AP33510 an ideal candidate for wide range output voltage applications such as USB PD3.0 PPS. With embedded E-GaN drive, the AP33510 provides safely and accurately Gate signal to control switch Q4 (GaN FET) operations and achieve high-power density charger applications. At no load or light load, the AP33510 enters the burst mode to minimize standby power consumption.

3.4.3 APR349 Synchronous Rectification (SR) MOSFET Driver

As a high performance solution, the APR349 is a secondary side SR controller to effectively reduce the secondary side rectifier power dissipation which works in both QR/DCM/CCM operation.

3.4.4 AP43771V PD 3.0 Decoder & Protection on/off N MOSFET and Interface to Power Devices

Few important pins provide critical protocol decoding and regulation functions in AP43771V:

1) **CC1 & CC2 (Pin 11, 10)**: CC1 & CC2 (Configuration Channel 1 & 2) are defined by USB Type-C spec to provide the channel communication link between power source and sink device.
2) **Constant Voltage (CV)**: The CV is implemented by sensing VFB (pin 8) and comparing with internal reference voltage to generate a CV compensation signal on the OCDRV pin (pin 5). The output voltage is controlled by firmware through CC1/CC2 channel communication with the sink device.
3) **Constant Current (CC)**: The CC is implemented by sensing the current sense resistor (RCS, 10mΩ, 1%, Low TCR) and compared with internal programmable reference voltage. The output current is controlled by firmware through CC1/CC2 channel communication with the sink device.
4) **Loop Compensation:**
   R19 & C19 form the voltage loop compensation circuit, and C18 form the current loop compensation circuit.
5) **OCDRV (Pin5)**: It is the key interface link from secondary decoder (AP43771V) to primary regulation circuit (AP33510). It is connected to Opto-coupler PC1 Pin 2 (Cathode) for feedback information based on all sensed CC1 & CC2 signals for getting desired Vbus voltage & current.
6) **PWR_EN (Pin2) to N-MOSFET Gate**: The pin is used to turn on/off N-MOSFET (Q1) to enable/disable voltage output to the Vbus.

Chapter 4 The Evaluation Board (EVB) Connections

4.1 EVB PCB Layout

Main Board – 1

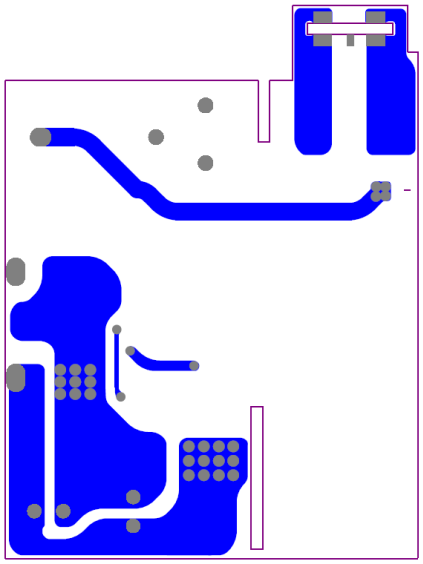


Figure 4: PCB Layout Top View

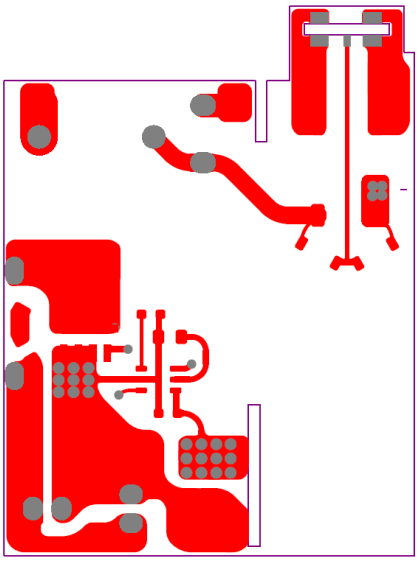


Figure 5: PCB Layout Bottom View

Main Board – 2

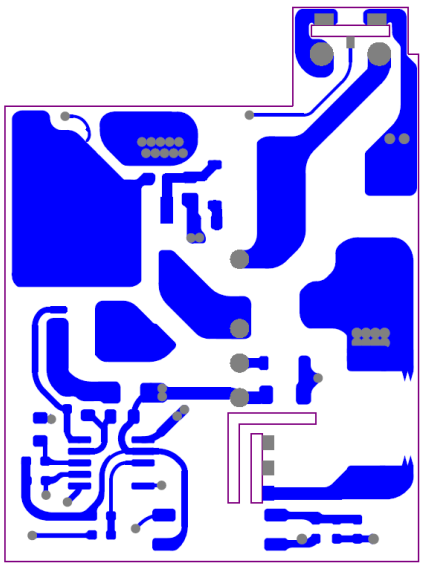


Figure 6: PCB Layout Top View

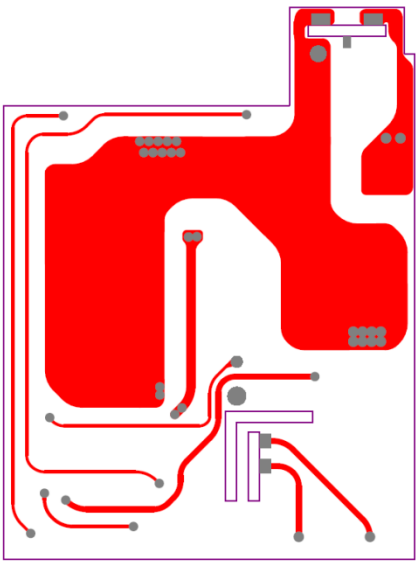


Figure 7: PCB Layout Bottom View

Main Board – 3

Figure 8: PCB Layout Top View

Figure 9: PCB Layout Bottom View

Daughter Board

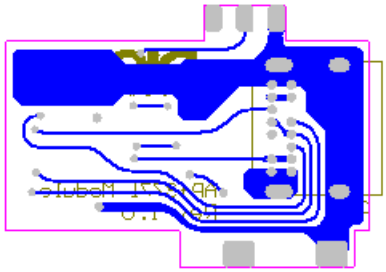


Figure 10: PCB Layout Top View

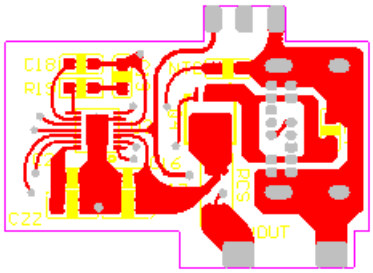


Figure 11: PCB Layout Bottom View

4.2 Quick Start Guide before Connection

1) Before starting the 65W EVB test, the end user needs to prepare the following tool, software and manuals.

For details, please consult USBCEE sales through below link for further information.

USBCEE PD3.0 Test Kit: USBCEE Power Adapter Tester. https://www.usbcee.com/product-details/4

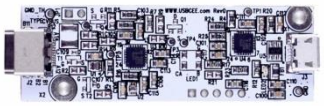
USBCEE PAT Tester	GUI Display	USB-A to Micro-B Cable	Type-C Cable
			

Figure 12: Test Kit / Test Cables

2) Prepare a certified three-foot Type-C cable and a Standard-A to Micro-B Cable.

3) Connect the AC inputs: L & N wires of EVB to AC power supply output “L and N “wires.

4) Ensure that the AC source is switched OFF or disconnected before the connection steps.

5) A type-C cable for the connection between EVB’s and Type-C receptacles of test kit.

6) Output of Type-C port & USB A-port are connected to E-load + & - terminals by cables.

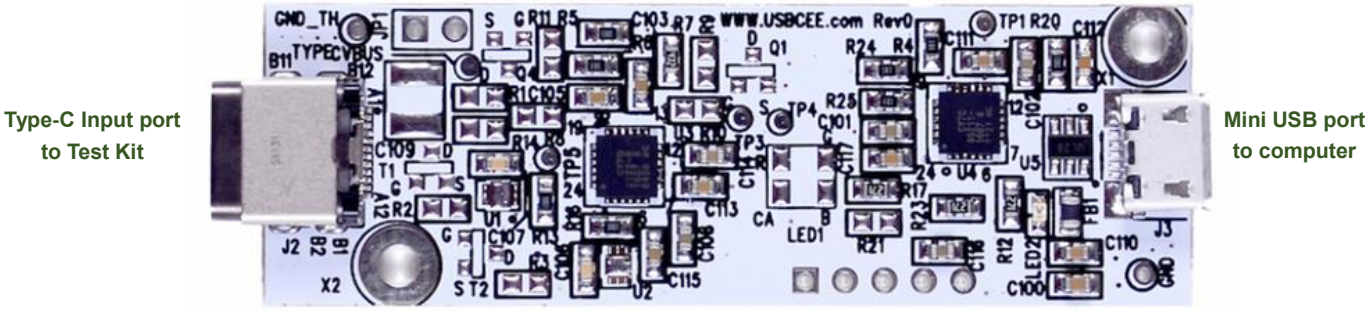


Figure 13: The Test Kit Input & Output and E-load Connections

4.3 Connection with E-Load

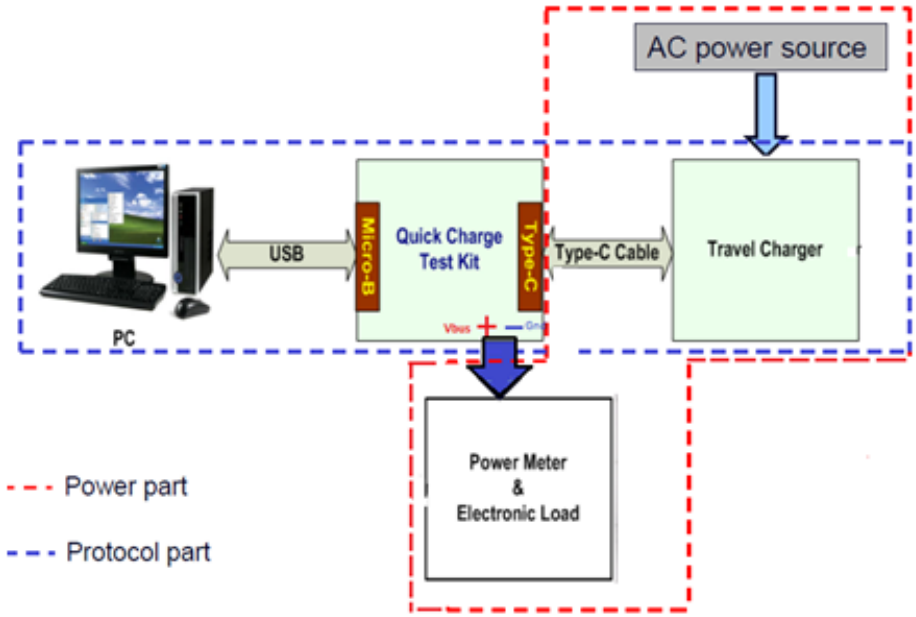


Figure 14: Diagram of Connections in the Sample Board

Chapter 5 Testing the Evaluation Board

5.1 Input & Output Characteristics

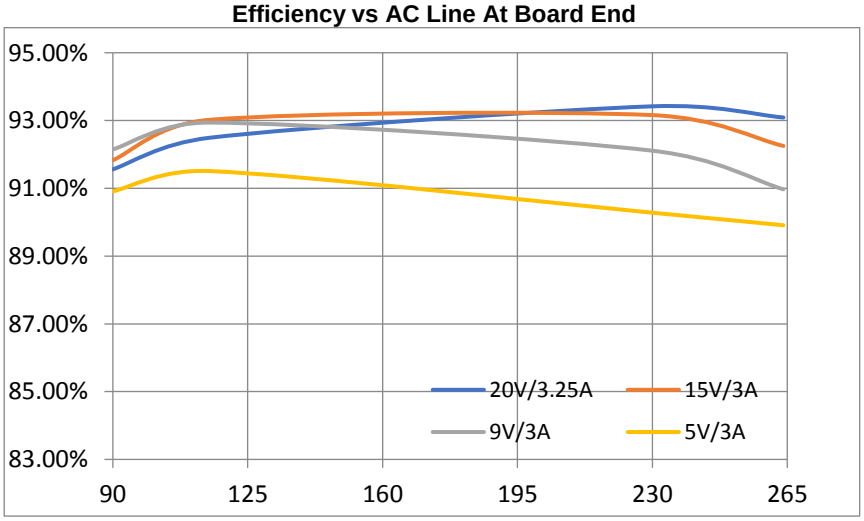
5.1.1 Input Standby Power

Vin(Vac)	F(Hz)	Pin(mW)
90	**63**	19
115	**60**	21
230	**50**	28
264	**47**	37

5.1.2 Multiple Output Full Load Efficiency at Different AC Line Input Voltage

PDO Mode	Vin(Vac)	F(Hz)	Iout(A)	Vout_Board (V)	Pin(W)	Pout(W)	Eff(%)
20V/3.25A	90	60	3.25	20.655	73.47	67.128	91.56%
	115	60	3.250	20.565	72.26	66.84	92.49%
	230	50	3.250	20.575	71.580	66.87	93.42%
	264	50	3.25	20.61	71.953	66.982	93.09%
15V/3A	90	60	3.00	15.300	49.98	45.90	91.83%
	115	60	3.00	15.313	49.387	45.94	93.02%
	230	50	3.00	15.303	49.280	45.91	93.16%
	264	50	3.00	15.330	49.85	45.99	92.25%
9V/3A	90	60	3.00	9.182	29.89	27.546	92.15%
	115	60	3.00	9.179	29.630	27.54	92.94%
	230	50	3.00	9.168	29.86	27.50	92.11%
	264	50	3.00	9.188	30.30	27.564	90.97%
5V/3A	90	60	3.00	5.140	16.961	15.42	90.91%
	115	60	3.00	5.155	16.899	15.47	91.51%
	230	50	3.00	5.153	17.123	15.46	90.28%
	264	50	3.00	5.148	17.177	15.444	89.91 %

Efficiency vs AC Line At Board End



5.1.3 Multiple Output Average Efficiency at Different Loading

Port-C PD3.0_PDO_20V / 15V Average Efficiency

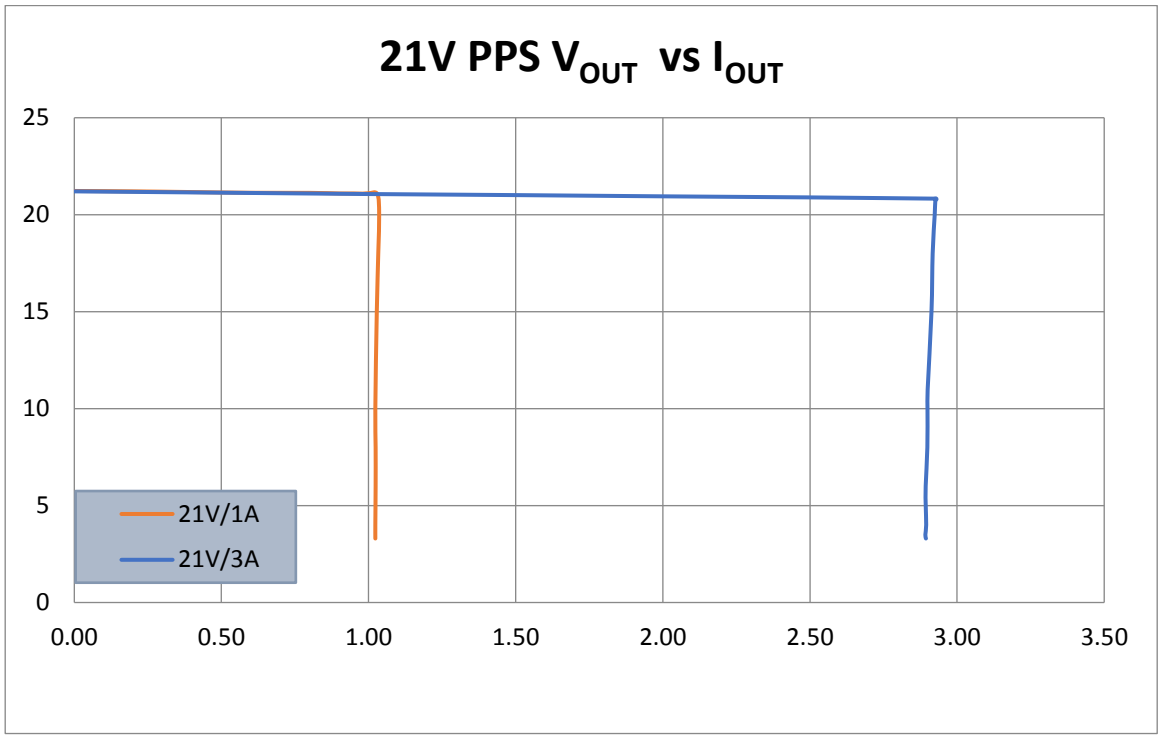
PDO Mode	Vin (Vac)	F(Hz)	Remarks	Iout(A)	Vout(V)	Pin(W)	Pout(W)	Eff(%)	Average Efficiency
20V/3.25A	115	60	100%	3.250	20.565	72.26	66.84	92.49%	92.81%
			75%	2.435	20.550	53.71	50.04	93.17%	
			50%	1.625	20.521	35.81	33.35	93.12%	
			25%	0.810	20.484	17.945	16.59	92.46%	
			10%	0.325	20.456	7.377	6.65	90.12%	
	230	50	100%	3.250	20.575	71.580	66.87	93.42%	92.48%
			75%	2.435	20.530	53.640	49.99	93.20%	
			50%	1.625	20.495	35.980	33.30	92.56%	
			25%	0.810	20.461	18.260	16.57	90.76%	
			10%	0.325	20.450	7.618	6.65	87.24%	
15V/3A	115	60	100%	3.000	15.313	49.387	45.94	93.02%	93.09%
			75%	2.250	15.288	36.841	34.40	93.37%	
			50%	1.500	15.258	24.537	22.89	93.28%	
			25%	0.750	15.218	12.31	11.41	92.72%	
			10%	0.300	15.196	5.050	4.56	90.27%	
	230	50	100%	3.000	15.303	49.280	45.91	93.16%	92.15%
			75%	2.250	15.267	37.017	34.35	92.80%	
			50%	1.500	15.235	24.890	22.85	91.81%	
			25%	0.750	15.204	12.550	11.40	90.86%	
			10%	0.300	15.190	5.240	4.56	86.97%	

Port-C PD3.0_PDO_9V / 5V Average Efficiency

PDO Mode	Vin (Vac)	F(Hz)	Remarks	Iout(A)	Vout(V)	Pin(W)	Pout(W)	Eff(%)	Average Efficiency
9V/3A	115	60	100%	3.000	9.179	29.630	27.54	92.94%	92.97%
			75%	2.250	9.147	22.102	20.58	93.12%	
			50%	1.500	9.114	14.681	13.67	93.12%	
			25%	0.750	9.078	7.343	6.81	92.72%	
			10%	0.300	9.054	2.963	2.72	91.67%	
	230	50	100%	3.000	9.168	29.86	27.50	92.11%	91.30%
			75%	2.250	9.140	22.42	20.57	91.73%	
			50%	1.500	9.106	14.988	13.66	91.13%	
			25%	0.750	9.072	7.538	6.80	90.26%	
			10%	0.300	9.052	3.088	2.72	87.94%	
5V/3A	115	60	100%	3.000	5.155	16.899	15.47	91.51%	91.82%
			75%	2.250	5.122	12.515	11.52	92.09%	
			50%	1.500	5.086	8.286	7.63	92.07%	
			25%	0.750	5.051	4.135	3.79	91.61%	
			10%	0.300	5.030	1.678	1.51	89.93%	
	230	50	100%	3.000	5.153	17.123	15.46	90.28%	89.37%
			75%	2.250	5.117	12.809	11.51	89.88%	
			50%	1.500	5.082	8.509	7.62	89.59%	
			25%	0.750	5.049	4.316	3.79	87.74%	
			10%	0.300	5.028	1.786	1.51	84.46%	

5.1.4 PD3.0 & PPS Compatible Mode Testing

CC Mode current limitation function testing
The test is by USBCEE Tester and with E-Load set at CR mode.
To Port-C PPS Mode set 21V-1A & 21V-3A and then increase the current (by reducing R) to see the CC-CV curve



5.2 Key Performance Waveforms

5.2.1 65W PD3.0 System Start-up Time

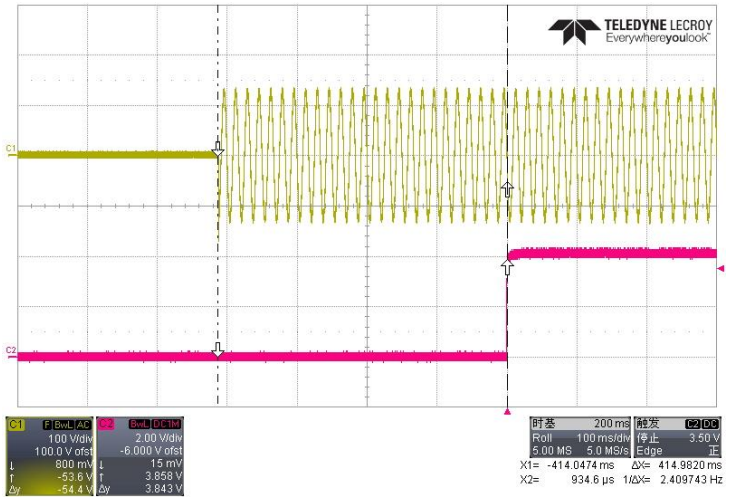


Figure 15: Turn on time is 415ms at Full Load@ 90Vac

5.2.2 Q1 / Q2 MOSFET Voltage Stress at Full Load @264Vac

Primary side MOSFET : Q1 and Secondary side SR MOSFET- Q2

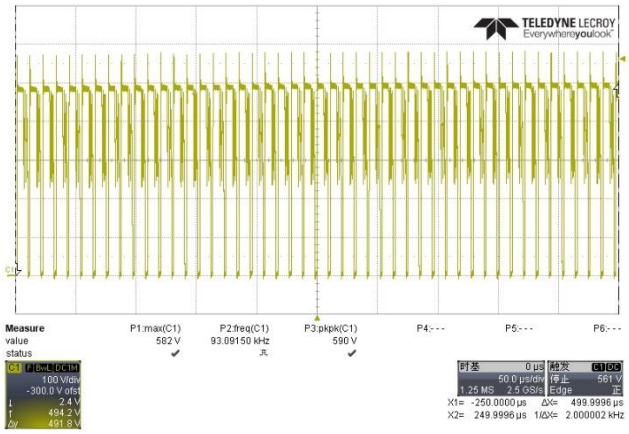


Figure 16: Q1 Vds Voltage stress

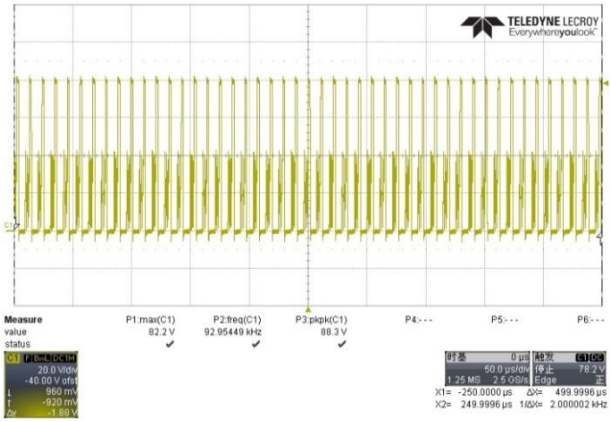


Figure 17: Q2 Vds Voltage stress

Component	Vout	Vds	Vds_Max_Spec	Ratio of voltage stress
Q1	20V	590V	650V	90.76%
Q2		88V	100V	88.00%

5.2.3 System Output Ripple & Noise with the Cable

Connect 47uF AL Cap and 104MLCC to the cable output unit in parallel

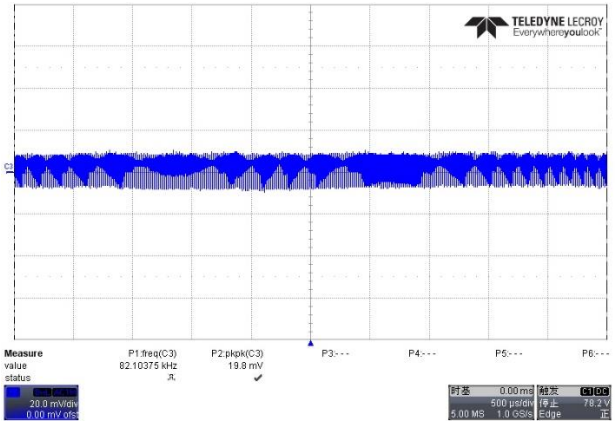


Figure 19: 90Vac/60Hz@ 5V/3A ΔV=19.8mV

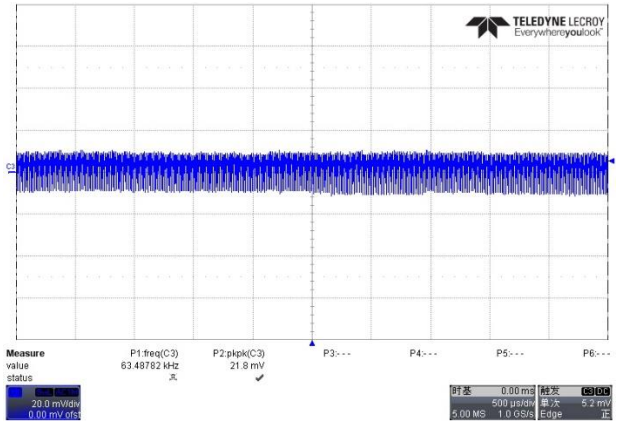


Figure 20: 264Vac/50Hz@5V/3A ΔV=21.8mV

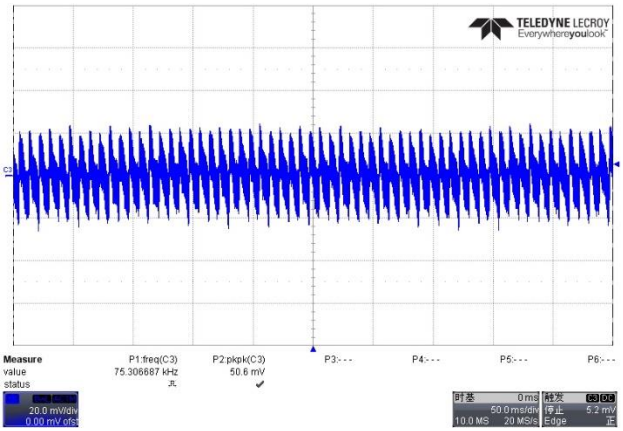


Figure 21: 90Vac/60Hz@9V/3A ΔV=50.6mV

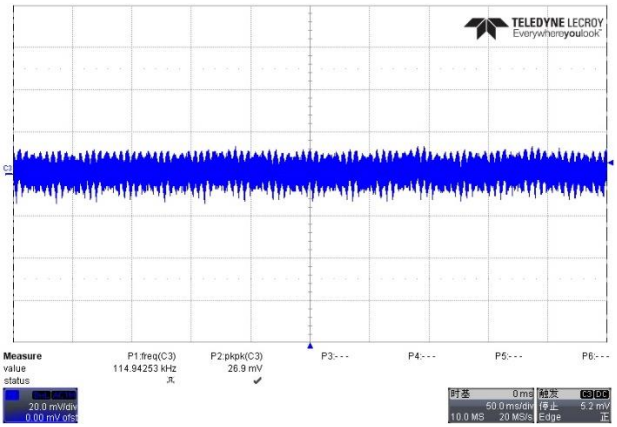


Figure 22: 264Vac/50Hz@9V/3A ΔV=26.9mV

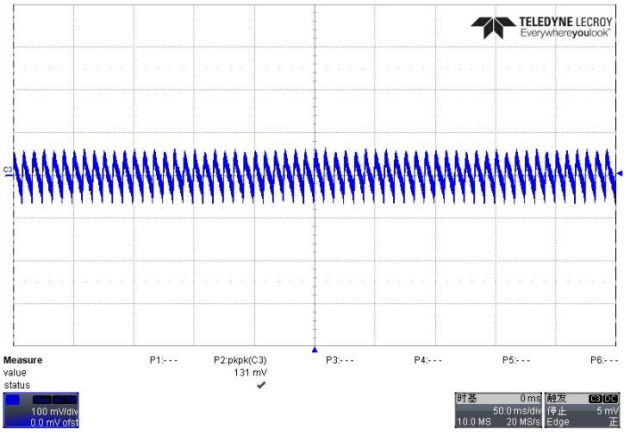


Figure 23: 90Vac/60Hz@15V/3A ΔV=131mV

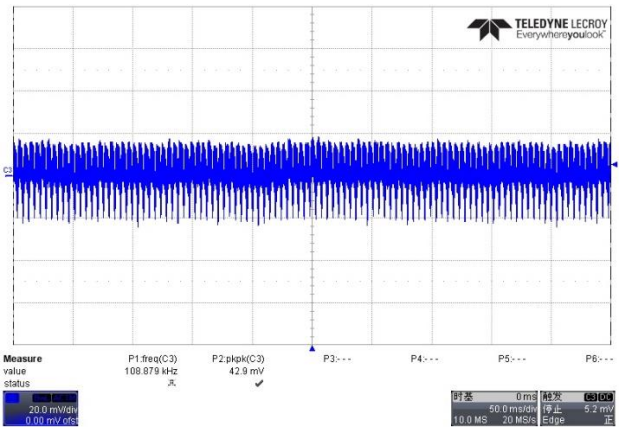


Figure 24: 264Vac/50Hz@15V/3A ΔV=42.9mV

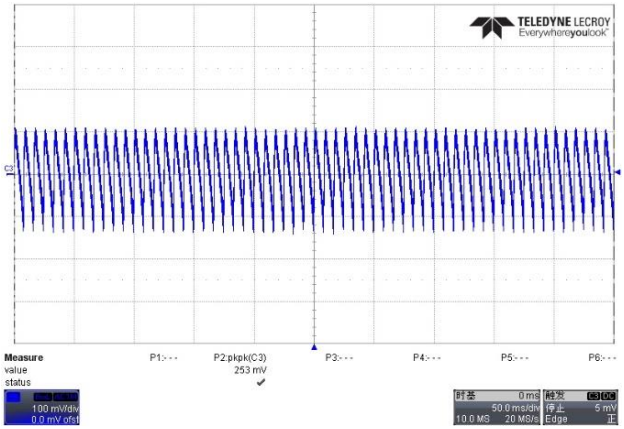


Figure 25: 90Vac/60Hz@20V/3.25A ΔV=253mV

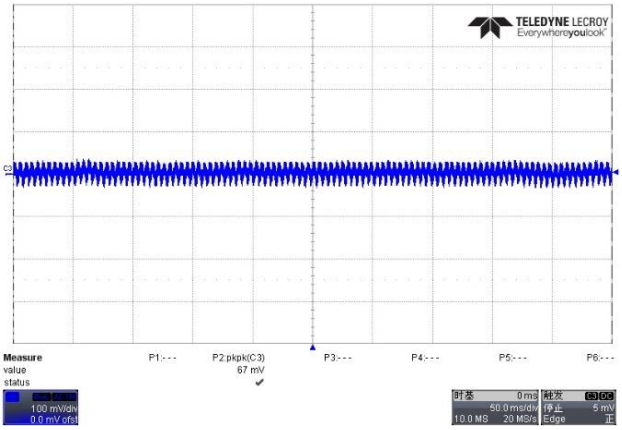


Figure 26: 264Vac/50Hz@20V/3.25A ΔV=67mV

5.2.4 Dynamic load ----0% Load~100% Load, T=20mS, Rate=15mA/uS (PCB End)

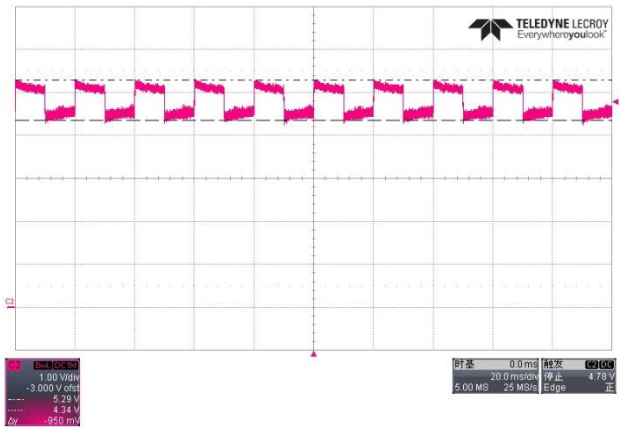


Figure 27: 90Vac/60Hz Port-C@ Vout=5V

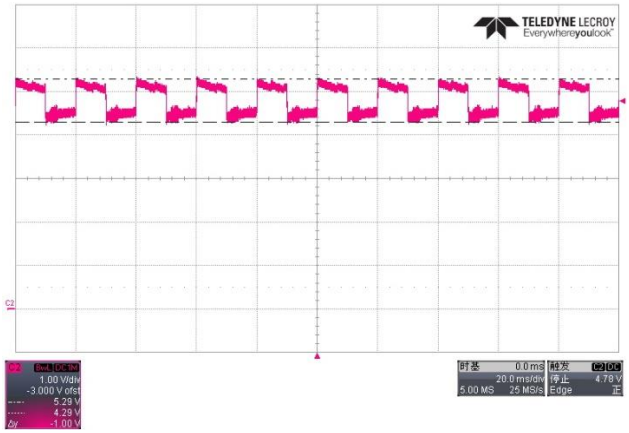


Figure 28: 264Vac/50Hz Port-C@ Vout=5V

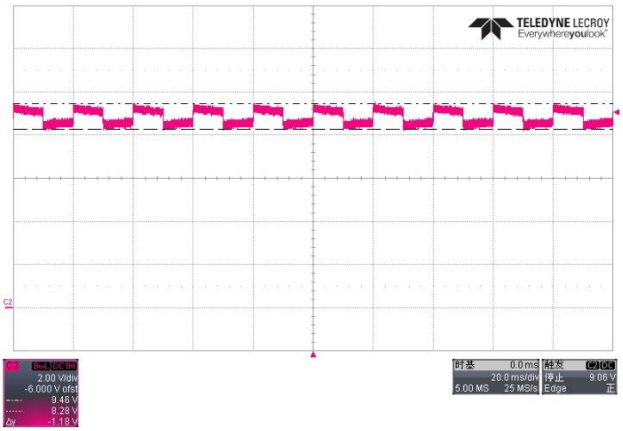


Figure 29: 90Vac/60Hz Port-C@ Vout=9V

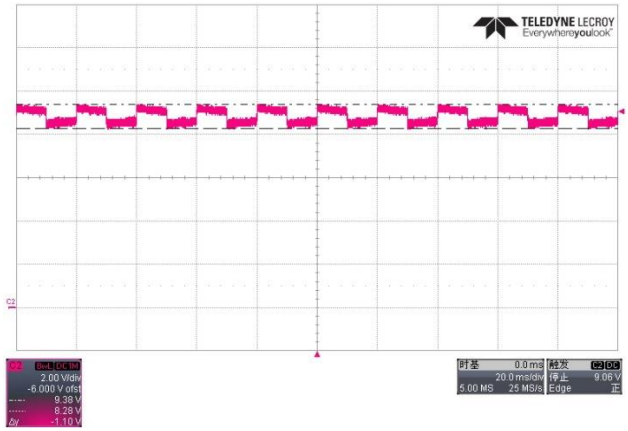


Figure 30: 264Vac/50Hz Port-C@ Vout=9V

	Vo_ Undershoot(V)	Vo_ Overshoot(V)		Vo_Undershoot(V)	Vo_Overshoot(V)
Vin=90Vac@5V	4.34	5.29	Vin=90Vac@9V	8.28	9.45
Vin=264Vac@5V	4.29	5.29	Vin=264Vac@9V	8.28	9.38

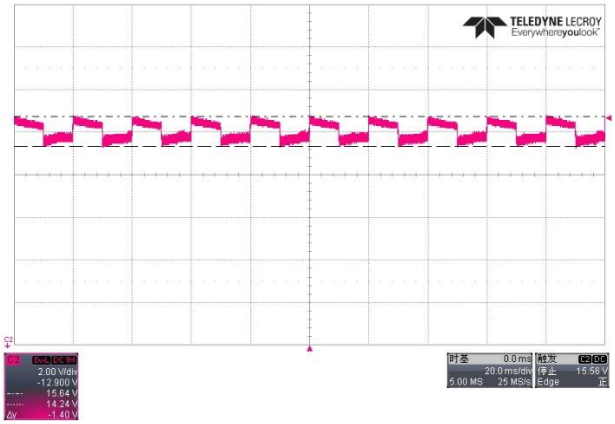


Figure 31: 90Vac/60Hz Port-C@ Vout=15V

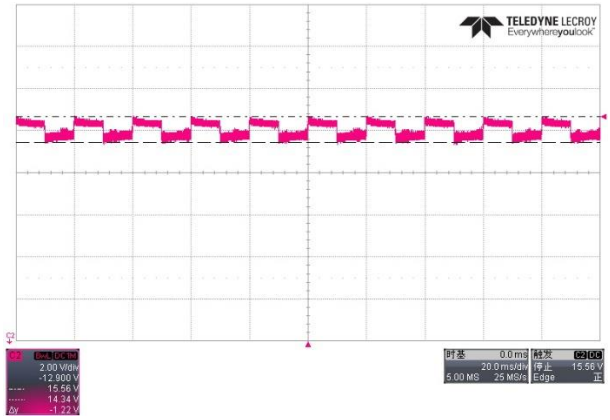


Figure 32: 264Vac/50Hz Port-C@ Vout=15V

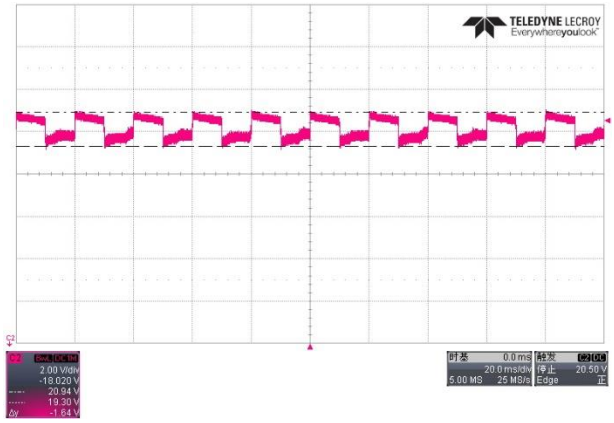


Figure 33: 90Vac/60Hz Port-C@ Vout=20V

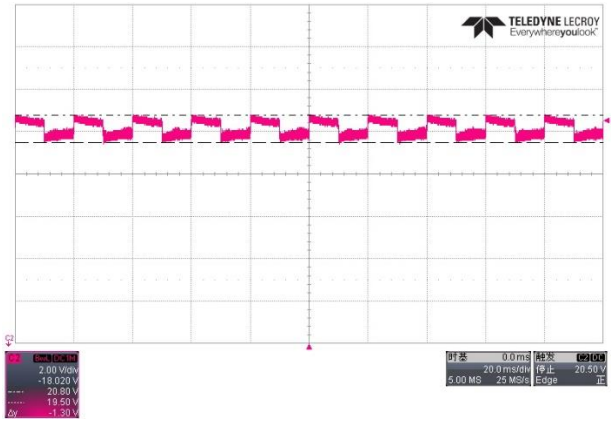


Figure 34: 264Vac/50Hz Port-C@ Vout=20V

	Vo_ Undershoot(V)	Vo_ Overshoot(V)		Vo_Undershoot(V)	Vo_Overshoot(V)
Vin=90Vac@15V	14.24	15.64	Vin=90Vac@20V	14.34	15.55
Vin=264Vac@15V	19.30	20.94	Vin=264Vac@20V	19.50	20.80

5.2.5 Output Voltage Transition Time from Low to High

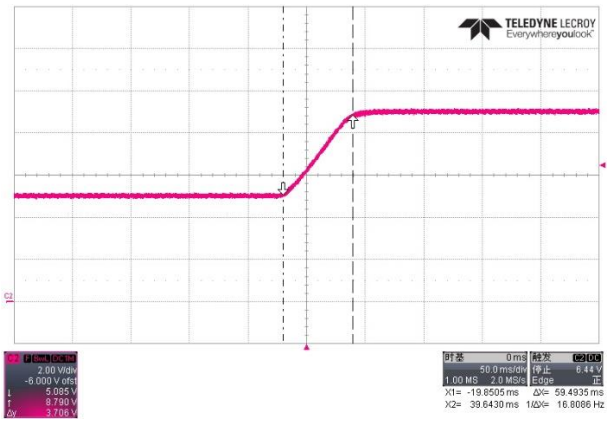


Figure 35: 5V→9V Rise Time = 59.49ms @90Vac

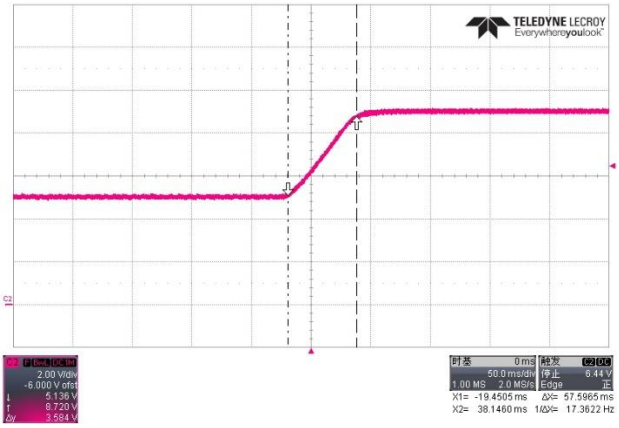


Figure 36: 5V→9V Rise Time = 57.59ms @264Vac

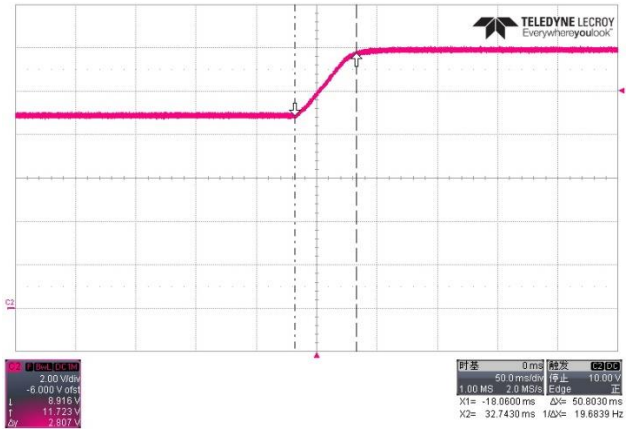


Figure 37: 9V→12V Rise Time = 50.08ms @90Vac

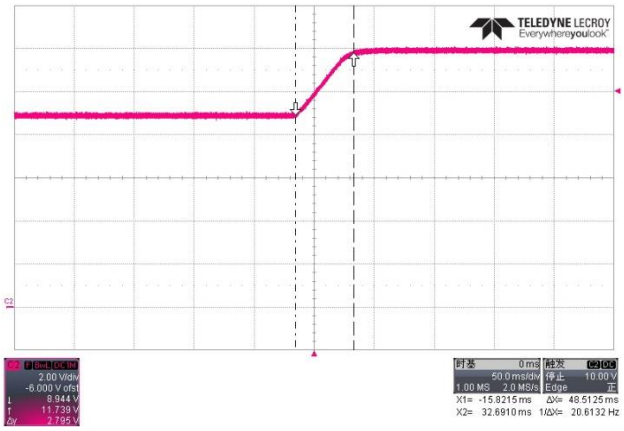


Figure 38: 9V→12V Rise Time = 48.51ms @264Vac

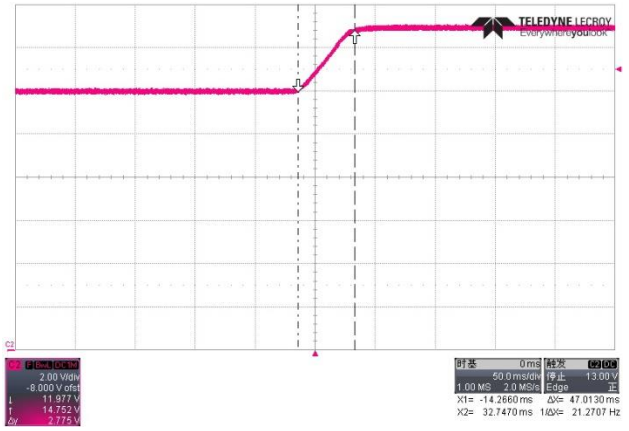


Figure 39: 12V→15V Rise Time = 47.01ms @90Vac

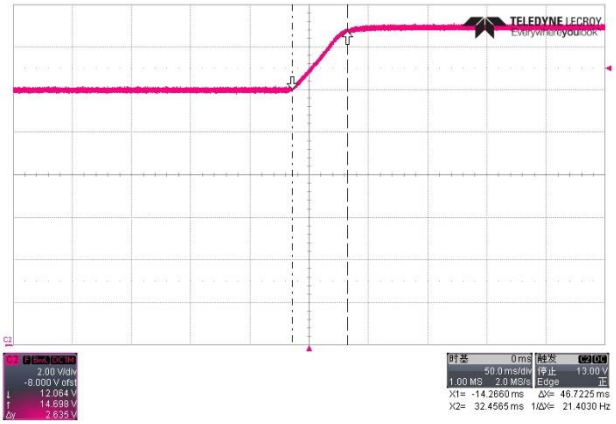


Figure 40: 12V→15V Rise Time = 46.72 ms@264Vac

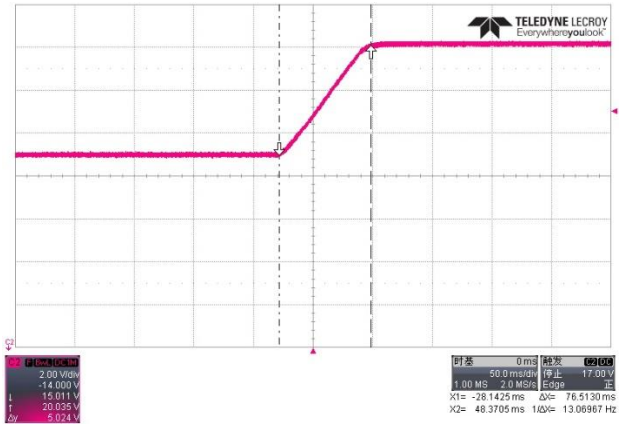


Figure 39: 15V→20V Rise Time = 76.51ms @90Vac

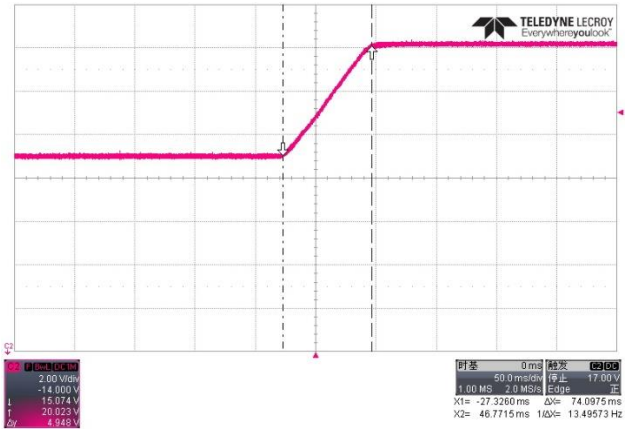


Figure 40: 15V→20V Rise Time = 74.09 ms@264Vac

5.2.6 Output Voltage Transition Time from High to Low

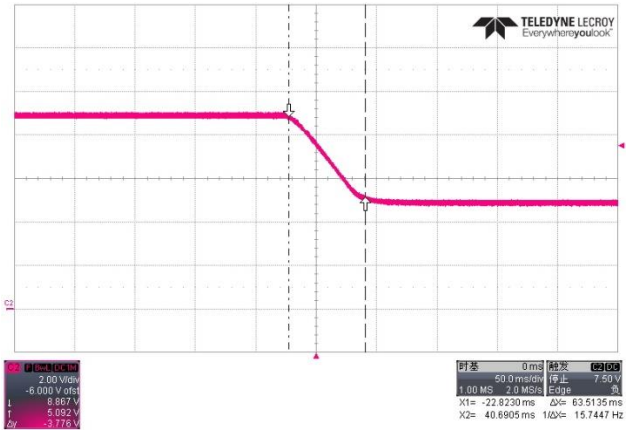


Figure 41: 9V→5V Fall Time = 63.51ms @90Vac

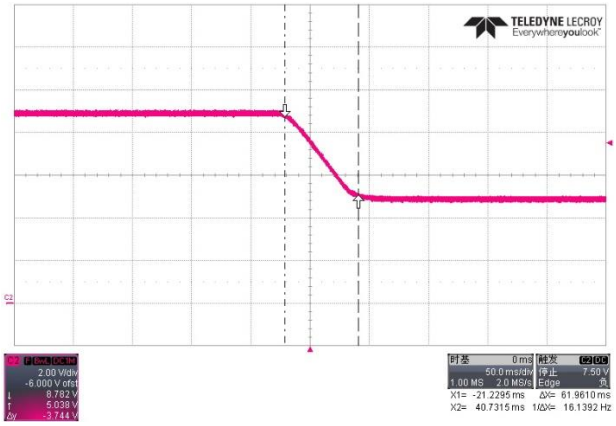


Figure 42: 9V→5V Fall Time = 61.96ms @264Vac

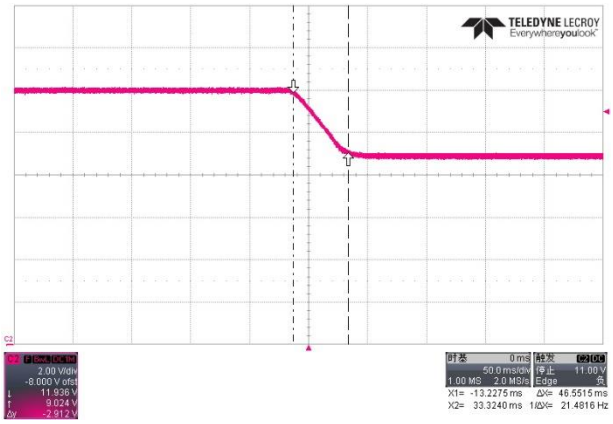


Figure 43: 12V→9V Fall Time = 46.55ms @90Vac

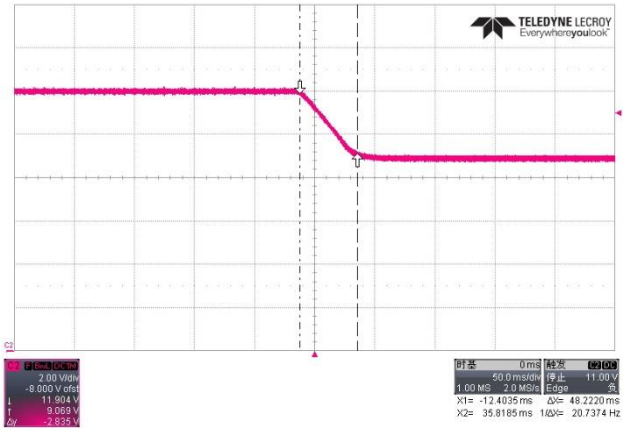


Figure 44: 12V→9V Fall Time = 48.22ms @264Vac

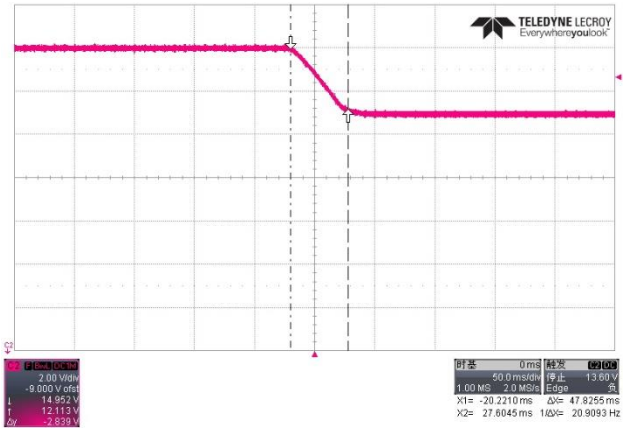


Figure 45: 15V→12V Fall Time = 47.82ms @90Vac

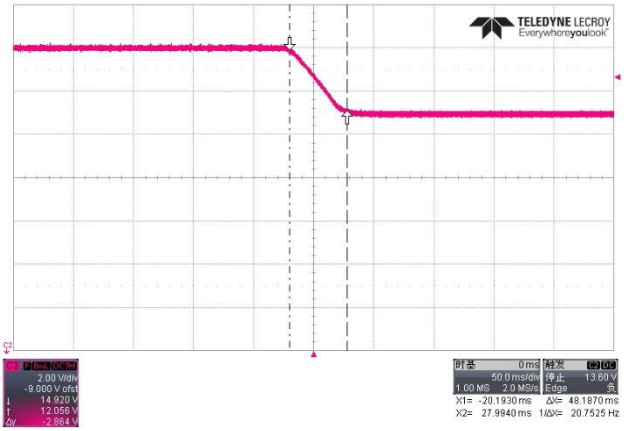


Figure 46: 15V→12V Fall Time = 48.18ms @264Vac

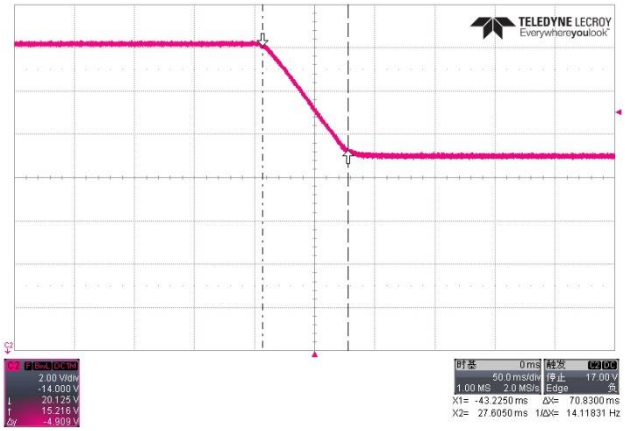


Figure 45: 20V→15V Fall Time = 70.83ms @90Vac

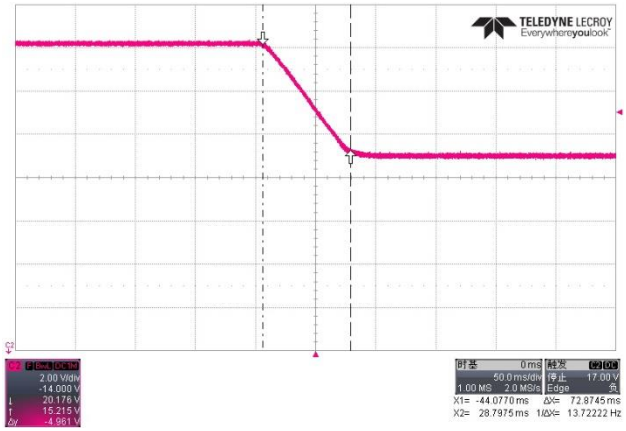


Figure 46: 20V→15V Fall Time = 71.87ms @264Vac

5.2.7 Thermal Testing

Output Condition : 20V/3.25A

Main Voltage	Temperature (°C)					
	BD1	Q1	D3	Q2	U1	U2
90Vac/60Hz	101.2	102.0	117.9	95.3	90.1	95
264Vac/60Hz	-	118.0	111	97.3	91.3	96

Test Condition: Vin=90Vac @ 20V-3.25A Full load Open Frame

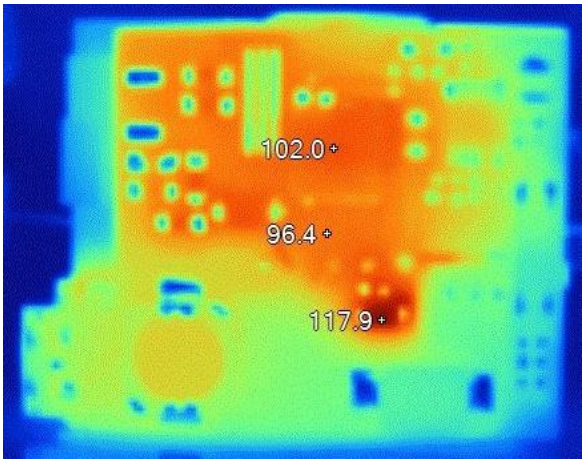


Figure 47: Top Components side

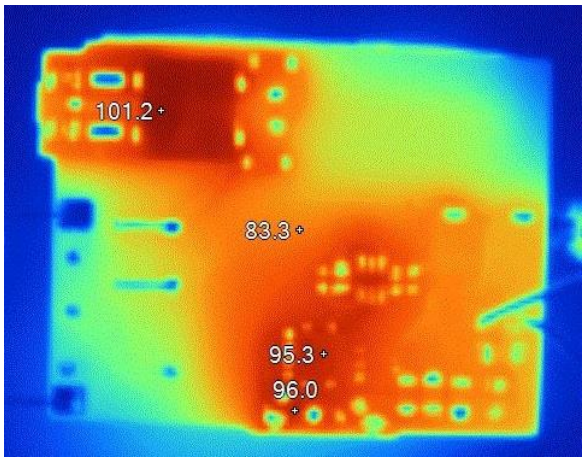


Figure 48: Bottom Suface Mount side

Test Condition: Vin=264Vac @ 20V-3.25A Full load Open Frame

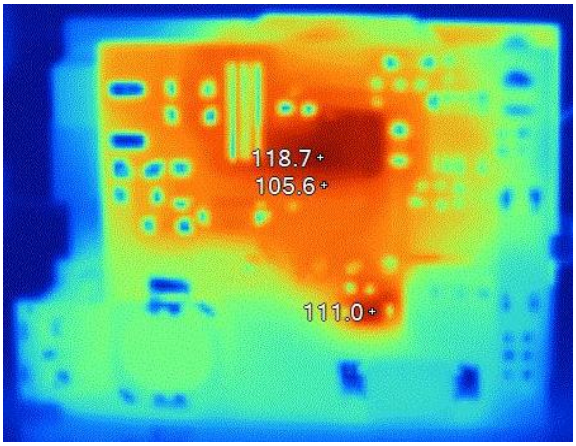


Figure 49: Top Components side

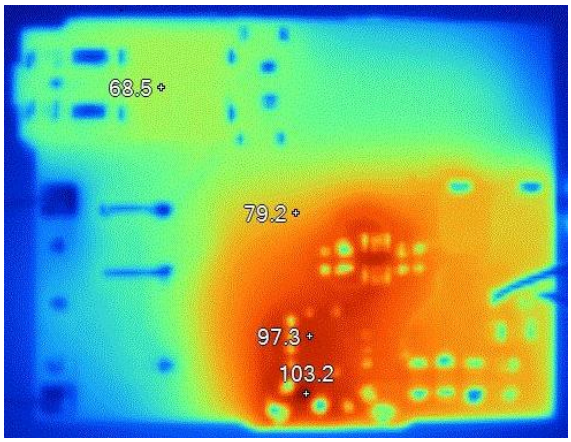


Figure 50: Bottom Suface Mount side

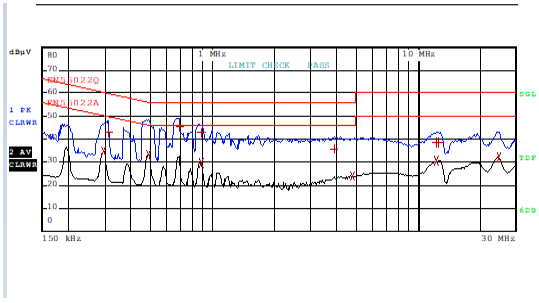
BD1: Bridge Rectifier
Q1 : Primary Side High Voltage GaN FET
D3 : Vcc diode
Q2 : Secondary Side Sync-Rectifier
U1 : AP33510, QR Controller
U2 : APR349, Sync-Rectifier Controller

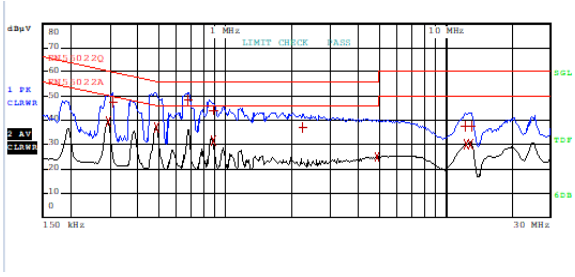
Note: Component temperature can be further optimized with various system design and thermal management approaches by manufacturers.

5.3 EMI (Conduction) Testing

115Vac testing results

Output Condition : 20V/3.25A





TRACE		FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
2	Average	292.16171188 kHz	34.75	-15.70
1	Quasi Peak	313.236901241 kHz	42.90	-16.97
2	Average	485.30343514 kHz	33.45	-12.79
1	Quasi Peak	687.48218373 kHz	45.61	-10.38
1	Quasi Peak	881.64914842 kHz	42.81	-13.18
2	Average	881.64914842 kHz	29.52	-16.47
1	Quasi Peak	3.88311708723 MHz	35.95	-20.04
2	Average	4.73814079378 MHz	23.89	-22.10
1	Quasi Peak	12.1937832503 MHz	38.40	-21.59
2	Average	12.1937832503 MHz	30.45	-19.54
1	Quasi Peak	12.4388782936 MHz	38.38	-21.61
2	Average	24.4700375488 MHz	31.83	-18.16

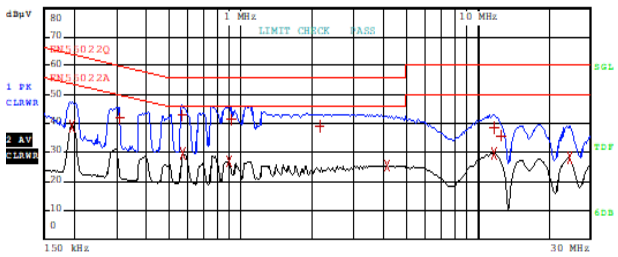
Figure 49: 115Vac/60Hz L line

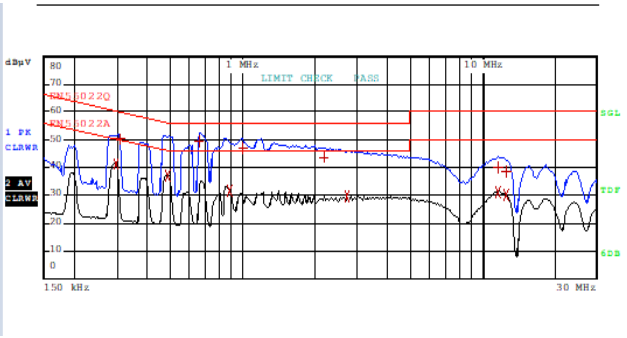
TRACE		FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
2	Average	292.16171188 kHz	39.44	-11.01
1	Quasi Peak	310.135545783 kHz	47.66	-12.29
2	Average	485.30343514 kHz	37.36	-8.88
1	Quasi Peak	673.936068749 kHz	48.29	-7.70
1	Quasi Peak	881.64914842 kHz	44.23	-11.76
2	Average	881.64914842 kHz	31.37	-14.62
1	Quasi Peak	2.24649226677 MHz	37.12	-18.87
2	Average	4.83337742374 MHz	24.79	-21.20
1	Quasi Peak	12.1937832503 MHz	37.49	-22.50
2	Average	12.3157210828 MHz	30.07	-19.92
2	Average	12.8157887448 MHz	30.38	-19.61
1	Quasi Peak	12.9439466322 MHz	37.77	-22.23

Figure 50: 115Vac/60Hz N line

230Vac testing results

Output Condition : 20V/3.25A





TRACE		FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
2	Average	194.288447245 kHz	39.23	-14.61
1	Quasi Peak	307.064896815 kHz	41.94	-18.11
1	Quasi Peak	563.422222132 kHz	42.70	-13.29
2	Average	569.056444353 kHz	29.61	-16.38
2	Average	890.465639904 kHz	27.12	-18.87
1	Quasi Peak	908.363999266 kHz	41.53	-14.46
1	Quasi Peak	2.1374603093 MHz	39.14	-16.85
2	Average	4.12200703523 MHz	25.64	-20.35
1	Quasi Peak	11.7179860284 MHz	38.42	-21.58
2	Average	11.7179860284 MHz	29.66	-20.33
1	Quasi Peak	12.4388782936 MHz	35.86	-24.13
2	Average	24.2277599493 MHz	28.22	-21.77

Figure 49: 230Vac/50Hz L line

TRACE		FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
2	Average	295.08333032 kHz	41.32	-9.05
1	Quasi Peak	307.064896815 kHz	50.14	-9.90
2	Average	485.30343514 kHz	37.26	-8.98
1	Quasi Peak	654.11570866 kHz	49.29	-6.70
2	Average	881.64914842 kHz	31.73	-14.26
1	Quasi Peak	1.00339897152 MHz	47.17	-8.82
1	Quasi Peak	2.1588349124 MHz	43.61	-12.38
2	Average	2.71400741459 MHz	29.76	-16.23
1	Quasi Peak	11.6019663647 MHz	39.97	-20.02
2	Average	11.6019663647 MHz	31.24	-18.75
1	Quasi Peak	12.4388782936 MHz	38.74	-21.25
2	Average	12.4388782936 MHz	30.20	-19.79

Figure 50: 230Vac/50Hz N line

IMPORTANT NOTICE

DIODES INCORPORATED MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

Diodes Incorporated and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. Diodes Incorporated does not assume any liability arising out of the application or use of this document or any product described herein; neither does Diodes Incorporated convey any license under its patent or trademark rights, nor the rights of others. Any Customer or user of this document or products described herein in such applications shall assume all risks of such use and will agree to hold Diodes Incorporated and all the companies whose products are represented on Diodes Incorporated website, harmless against all damages.

Diodes Incorporated does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.
Should Customers purchase or use Diodes Incorporated products for any unintended or unauthorized application, Customers shall indemnify and hold Diodes Incorporated and its representatives harmless against all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized application.

Products described herein may be covered by one or more United States, international or foreign patents pending. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks.

This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes Incorporated.

LIFE SUPPORT

Diodes Incorporated products are specifically not authorized for use as critical components in life support devices or systems without the express written approval of the Chief Executive Officer of Diodes Incorporated. As used herein:

A. Life support devices or systems are devices or systems which:

1. are intended to implant into the body, or
2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

Customers represent that they have all necessary expertise in the safety and regulatory ramifications of their life support devices or systems, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of Diodes Incorporated products in such safety-critical, life support devices or systems, notwithstanding any devices- or systems-related information or support that may be provided by Diodes Incorporated. Further, Customers must fully indemnify Diodes Incorporated and its representatives against any damages arising out of the use of Diodes Incorporated products in such safety-critical, life support devices or systems.

Copyright © 2017, Diodes Incorporated **www.diodes.com**