PAM8303D-3W Mono Class-D Amplifier

AE Department

1. Revision Information

Date	Revision	Description	Comment
22008/03/18	V1.0	Initial Release	

2. PAM8303D Evaluation Board Description

PAM8303D CB81CA for MSOP-8 and DFN3*3 is designed for PAM8303D evaluation, targeted to be used in providing a simple and convenient evaluation environment for the PAM8303D. Requires parts, potentiometer for standard RCA jacks for audio inputs, pin jacks for power supply and signal outputs, low-pass RC output filter for each channel, etc. on the board make it easy to be evaluated.

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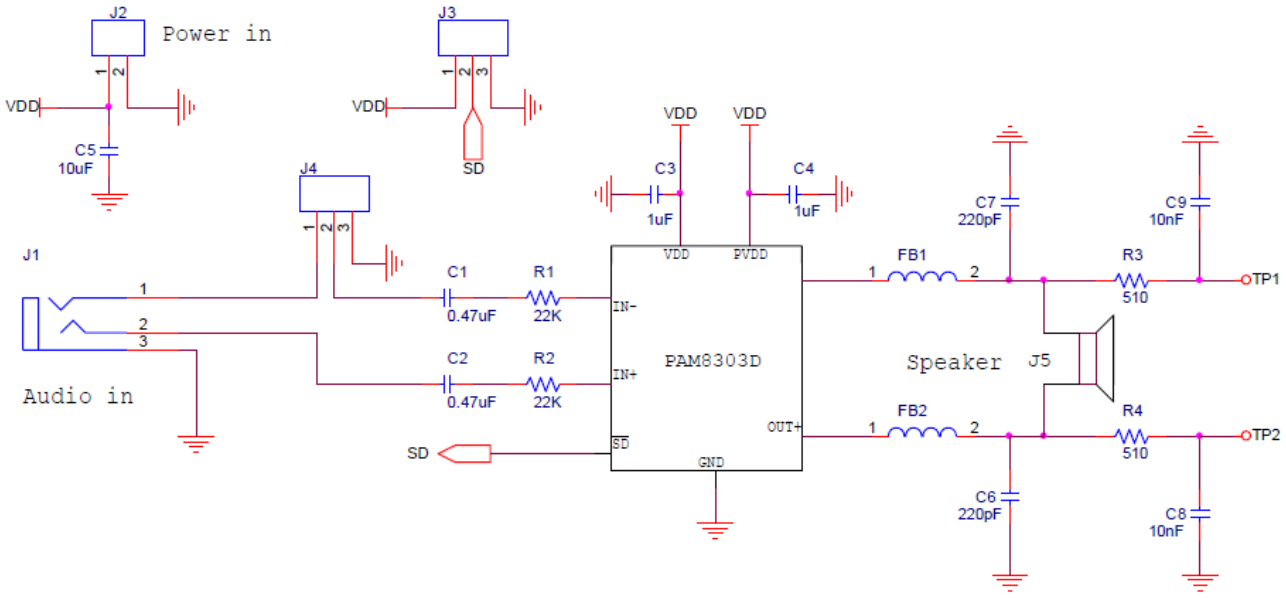
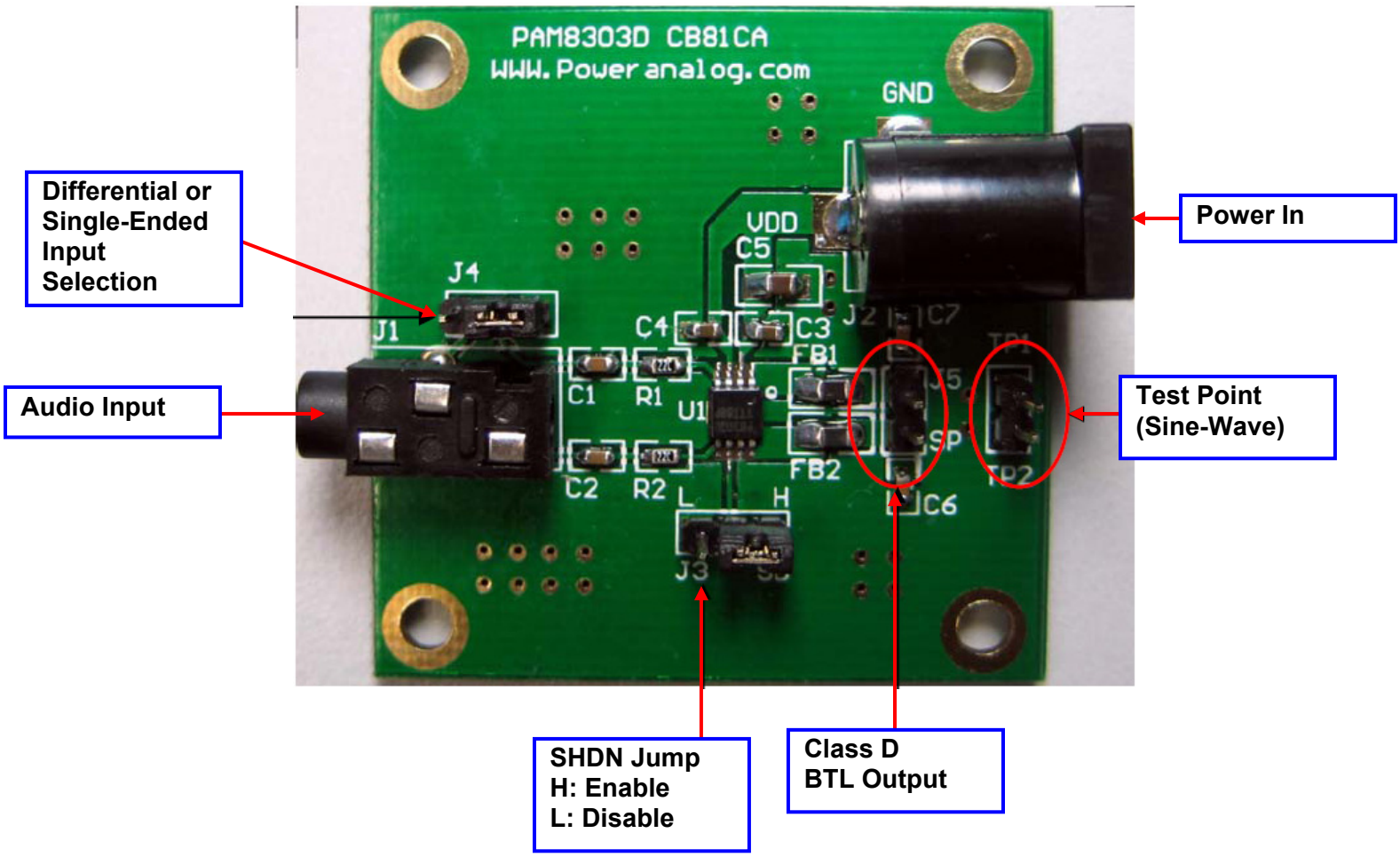
3. EV Board Schematic



4. EVB View

4-1 Top Layer



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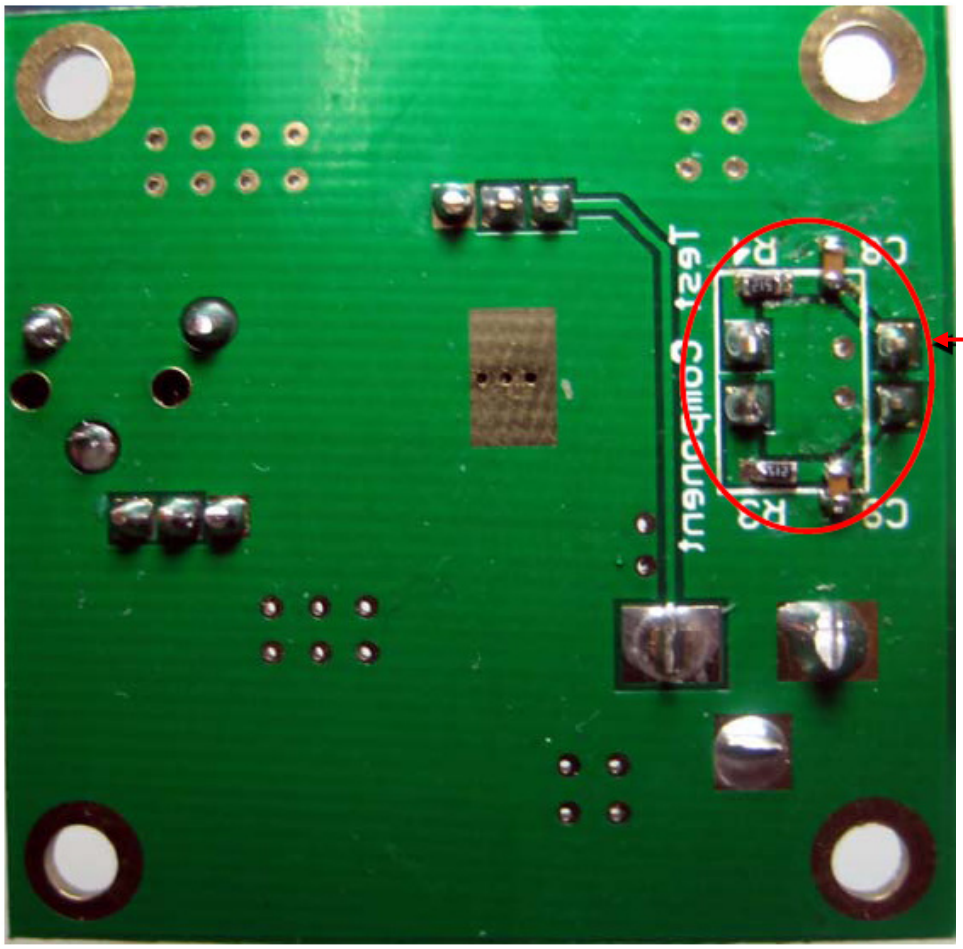
4-2 Bottom Layer



EV Board Operational Sequence:

a. Connect SD to a high for normal operation.

b. Connect audio input from audio input jack (J1).

c. Put the jump J4 to right side: single-ended input.

d. Connect the SPKs to the BTL output jack.

e. Power on: 2.8V to 5V DC power supply.

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5. EVB BOM List

Capacitors	Qty	Value	Description	Rating	Package	Purpose
C1, C2	2	0.47μF	Ceramic X5R/X7R	6V	0603	Input Coupling
C3, C4	2	1.0μF	Ceramic X5R/X7R	6V	0603	VDD/PVDD Bypass
C5	1	10.0μF	Ceramic X5R/X7R	6V	0603	Power in Bypass
Resistors	**Qty**	**Value**	**Description**	**Rating**	**Package**	**Purpose**
R1, R2	2	22kΩ	1% Tolerance		0603	Input Resistor
EMI Components	**Qty**	**Value**	**Description**	**Rating**	**Package**	**Purpose**
FB1, FB2	2	120Ω	PBY201209T-121Y-N		0805	For EMI
C6, C7	2	220pF	Ceramic X5R/X7R	6V	0805	For EMI
Test Components	**Qty**	**Value**	**Description**	**Rating**	**Package**	**Purpose**
C8, C9	2	10nF	Ceramic X5R/X7R	6V	0603	
R3, R4	2	510Ω			0603	
Jack	**Qty**	**Value**	**Description**	**Rating**	**Package**	**Purpose**
J1	1		Input Jack			
J2			Power In			
J3			Shutdown Jump			
J4	1		Input Jump			Jump for Single-Ended or Differential Input
J5	1		Speaker			

6. PCB Layout Guidelines

Grounding

(1) Use plane grounding.

(2) Output noise grounds must tie to system ground at the power in exclusively.

(3) Signal currents for the inputs need to be returned to quite ground.

This ground only ties to the signal components and the GND pin.

Power Supply

(1) Both VDD and PVDD need to be decoupled by 1μF capacitance, and the traces are separated and then tied together in system power supply (Figure 1)

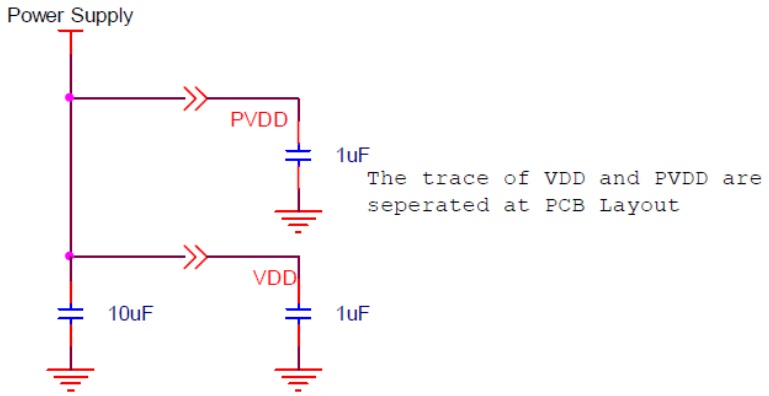

Figure 1 Power Supply Decoupling

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6. PCB Layout Guidelines (cont.)

Power Supply (cont.)

(2) Recommend that the all the trace could be routed as short and thick as possible.

(3) Any barricade placed in the trace could result in the bad performance of the amplifier.

Components Placement

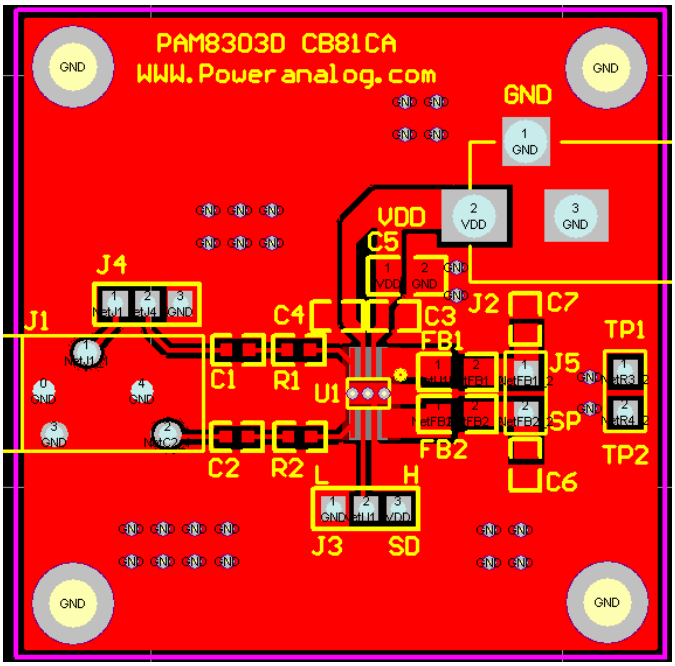
(1) The power supply capacitors(C3 and C4) need to place very close to the PAM8303D

(2) Input resistors (Ri) and input capacitors (Ci) place closed to input pins as soon as possible

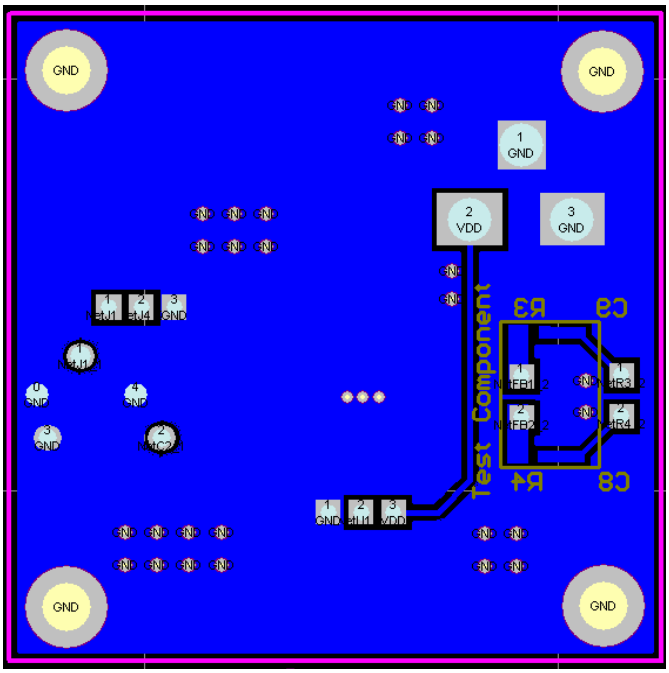
(3) Output filter — The ferrite EMI filter should be placed as close to the output terminals as possible for the best EMI performance, and the capacitors used in the filters should be grounded to PGND.

7. PCB Layout Example

Top Layer



Bottom Layer



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