PAM8006A-EV Board User Guide

AE Department

1. Revision Information

Date	Revision	Description	Comment
2012/10/24	V1.0	Initial Release	

2. PAM8006A General Description

The PAM8006A is a 15W (per channel) stereo class-D audio amplifier which offers low THD+N (0.1%), low EMI, and good PSRR thus high quality sound reproduction.

The PAM8006A runs off of a 8V to 26V supply at much higher efficiency than compete tors'Ics.

The PAM8006A only requires very few external components, significantly saving cost and board space.

The PAM8006A is available in a 32pin QFN 5mm*5mm.

3. Key Features

- 15W@10%THD / Channel Output into a 8ΩLoad
- Low Noise: -90dB
- Over 90% Efficiency
- With Shutdown/Mute Function
- Over Current ,OVP, UVLO, Thermal and Short- Circuit Protection
- Low THD+N
- Power Limit with Non-clip
- Low Quiescent Current
- Pop noise suppression
- Small Package Outlines: Thin 32-pin QFN 5mm*5mm

4. EV Board Schematic

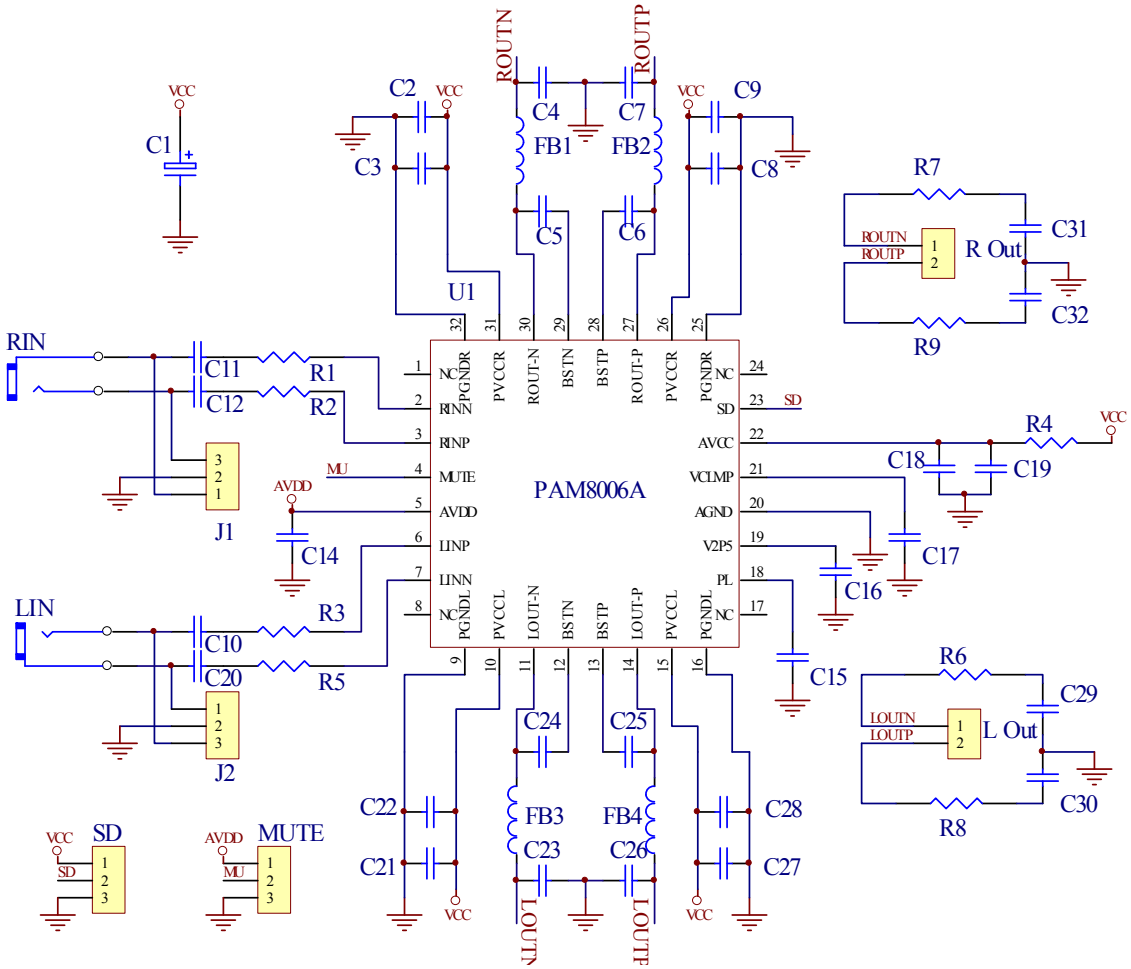


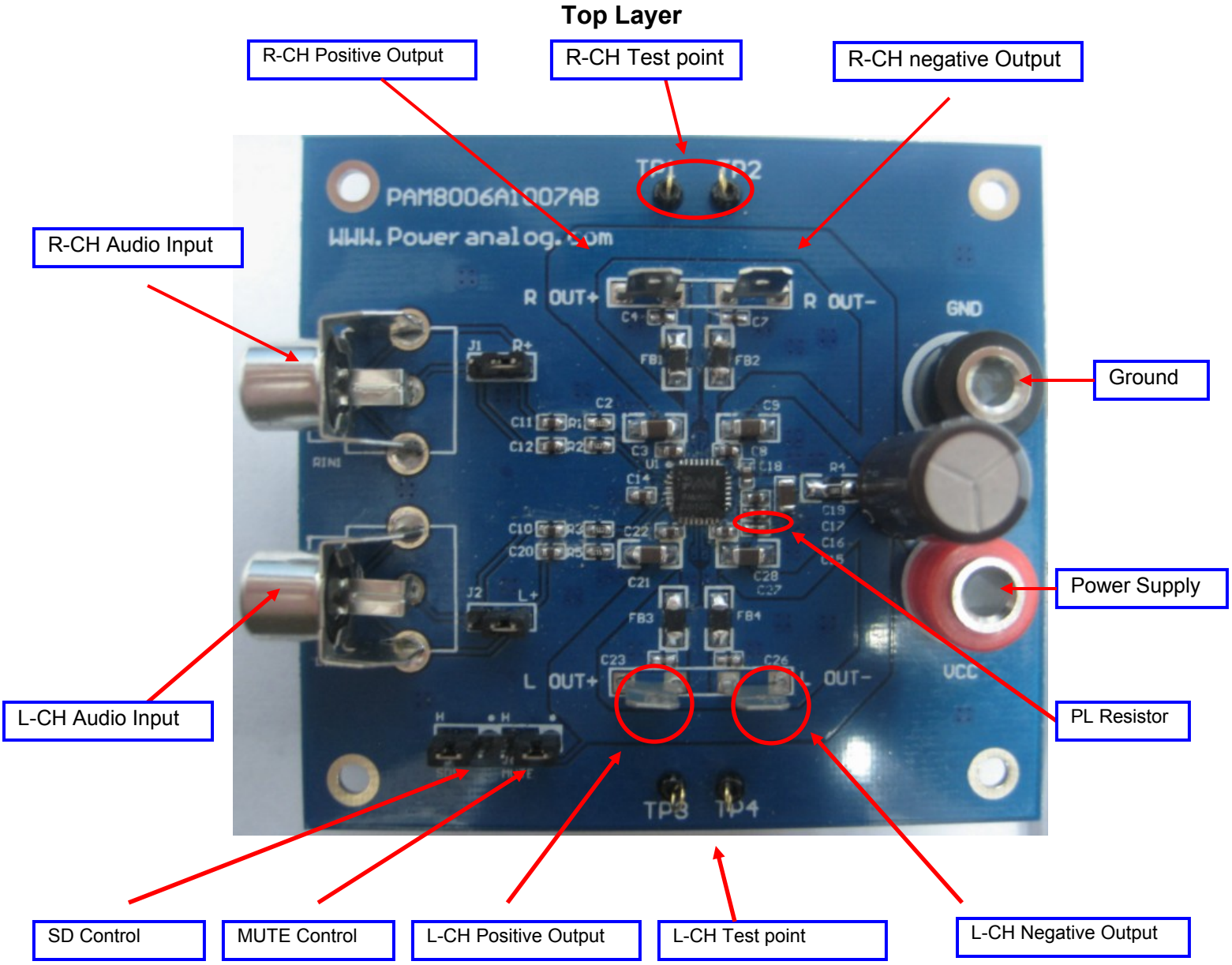
Figure 1

5. EVB PAM8006A EVB Description

PAM8006A 1007AB is an evaluation board for the PAM8006A, a stereo class-D audio power amplifier. The board is targeted to be used in providing a simple and convenient evaluation environment for the PAM8006A. Requires parts, the standard RCA jacks for audio inputs, pin jacks for power supply and signal outputs etc. on the board make it easy to be evaluated.

6. EV Board View and Jack Description

Top Layer



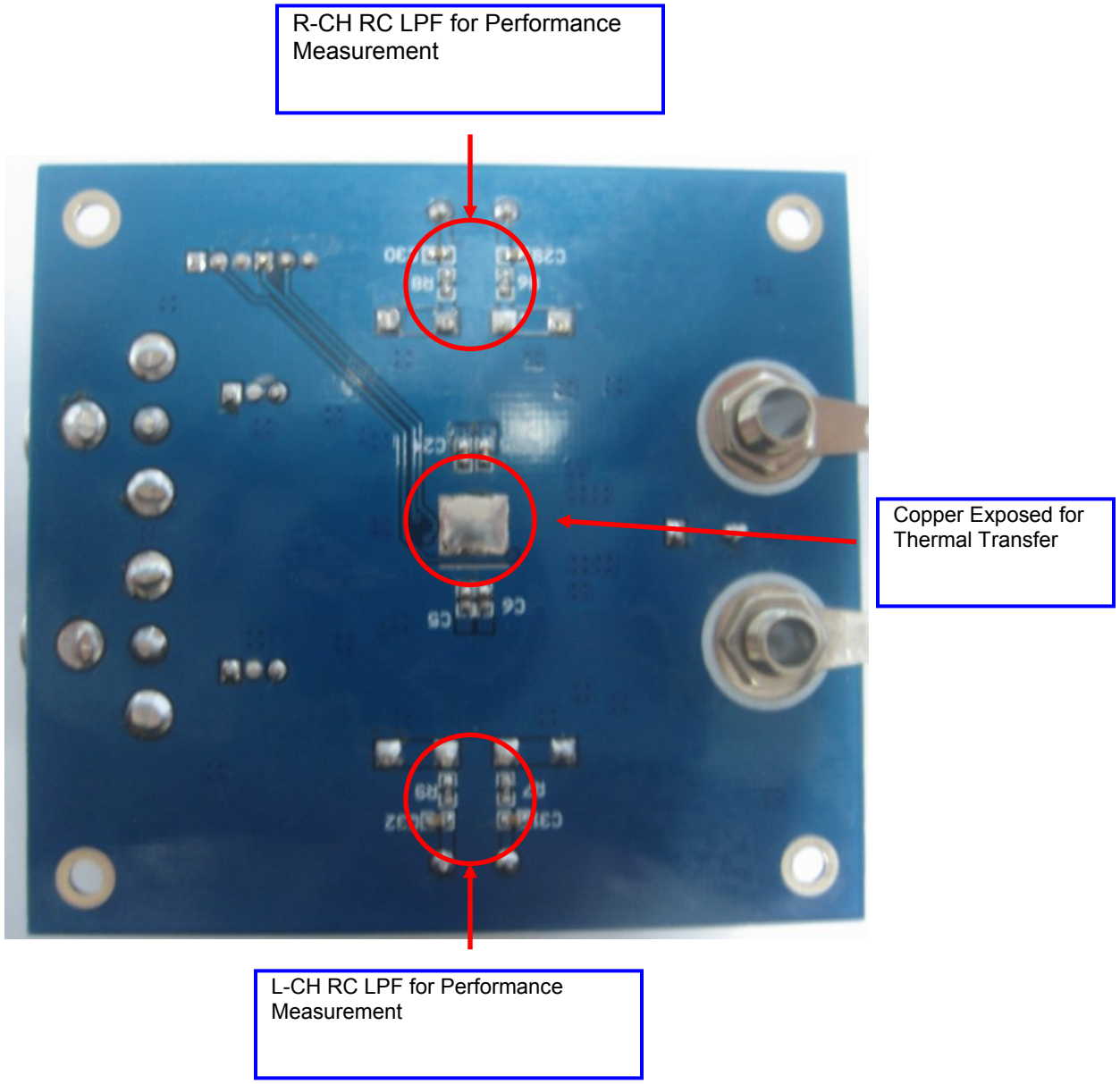
Test Point (TP1~TP4) on Top Layer Description

TP1/TP2/TP3/TP4: Output test point, TP1/TP2 for right channel, TP3/TP4 for left channel

Connect to analyzer (AP or Scope)

Cannot connect loading to these test point directly

Bottom Layer



EV Board Operational Sequence:

a. Connect SD to a high and MUTE to a low for normal operation.

b. Connect audio input from audio input jack (differential or single-end signal).

c. Connect the loading(speaker or power resistor) to the output jack.

d. Power on: 8V to 18V DC power supply.

7. EV Board BOM List

Item	Value	Type	Rating	Description
C10,C11,C12,C20	1μF	X5R/X7R, Ceramic/0603	10V	Input coupling CAP
C14	1μF	X5R/X7R, Ceramic/0603	10V	Internal 5V bias voltage coupling CAP
C5,C6,C24,C25	1μF	X5R/X7R, Ceramic/0603	50V	High side driver bootstrap CAP
C3,C8,C22,C28	1μF	X5R/X7R, Ceramic/0603	25V	PVDD coupling CAP,
C2,C9,C21,C27	10μF	X5R/X7R, Ceramic/0805	25V	PVDD main coupling CAP,
C17	1μF	X5R/X7R, Ceramic/0805	25V	Internal regulators coupling CAP
C16	1.0μF	X5R/X7R, Ceramic/0603	6V	Internal 2.5V bias decoupling CAP
C18	0.1μF	X5R/X7R, Ceramic/0603	25v	AVCC coupling CAP
C19	10μF	X5R/X7R, Ceramic/0805	25V	AVCC main coupling CAP
C15		X5R/X7R, Ceramic/0603	25V	PL Resistor and CAP
R1,R2,R3,R5	5.1k	0603	1%	Input Resistor
FB1,FB2,FB3,FB4	600Ω	0805	4A	For EMI eliminate components form a FB-CAP filter
C4,C7,C23,C26	200pF	0603	25V	
C1	470μF	Electrolytic	35V	Power supply decoupling CAP
R4	10Ω	0805	5%	Separate AVCC from PVDD
R6,R7,R8,R9	1K	0603	5%	Test component
C29,C30,C31,C32	4.7nF	0603	25V	

8. External Compnents Selection

Input Capacitors (C10, C11, C12 and C20)

(1) Form a high pass filter with Ri, and the cut off frequency is fc=1/2*Π*Ri*Ci

(2) Have a tolerance of 10% or better for matching : any mismatch in capacitance causes an importance mismatch at the corner frequency and below

(3) Low leakage current needed, 1.0uF, X5R/X7R ceramic recommend

Input Resistors (R1, R2, R3 and R5)

(1) Limit the closed-loop gain

(2) Form a high pass filter with Ci, and the cut off frequency is fc=1/2*Π*Ri*Ci

(3) 1% tolerance needed for resistor matching to improve CMRR, PSRR

BSN and BSP Capacitors (C5, C6, C24 and C25)

(1) For the high side NMOS of full H-bridge output stages bootstrap

(2) 1uF X5R/X7R ceramic capacitor and rated for at least 50V

(3) One is connected from OUTP to BSP

(4) One is be connected from OUTN to BSN

8. External Compnents Selection (cont.)

Power Supply decoupling Caps (C2, C3, C8, C9, C18, C19, C21,C22 , C27,and C28)

(1) Low ESR for good THD, PSRR

(2) 1uF/0.1uF ceramic for higher frequency transients, spikes, or digital hash on the line of PVDD/AVCC

(3) Additional 10uF or greater for low frequency noise filtering and serves as a local storage capacitor for supplying current during large signal transients on the amplifier outputs

(4) Need place very closed to the IC

VCLAMP Capacitors (C17)

(1) VCLAMP limit the Vgs of the low side NMOS

(2) 1uF, X5R/X7R ceramic and rated 25 at least recommend

(3) Place closed to the device

Internal Regulated 5V-Supply Capacitor (C14)

(1) Internal power supply for pre-amplifier,

(2) 1uF, X5R/X7R ceramic recommend

(3) Place very closed to the device

Internal 2.5V Bias Supply Capacitor (C16)

(1) Internal power supply for pre-amplifier,

(2) 1uF, X5R/X7R ceramic recommend

(3) Place very closed to the device

EMI Eliminate Filter (FB1, FB2, FB3 and FB4)

(1) High impedance at high frequency and very low impedance at low frequency

(2) The current rating is higher than 4A

RC filter for Class D Performance Evaluation (R6, R7, R8, R9, C29, C30, C31 and C32)

(1) R=1KΩ,5% tolerance and C=4.7nF 25V rating need

(2) RC form a LPF, the cut off frequency is 31KHz

9. PCB Layout Guidelines

Grounding

(1) Use plane grounding or separate grounds

(2) Do not use one line connecting power GND and analog GND

(3) Output noise grounds must tie to system ground at the power in exclusively.

(4) Signal currents for the inputs need to be returned to quite ground. This ground only ties to the signal components and the GND pin.

Power Supply

(1) AVCC and each of PVDD need to be separated and tied together at the system power supply.

(2) Recommend that the all the trace could be routed as short and thick as possible.

(3) Any barricade placed in the trace could result in the bad performance of the amplifier.

10. Component Placement

Decoupling Capacitors

(1) The power supply capacitors (C2, C3, C8, C9, C18, C19, C21,C22 , C27,and C28) need to place very close to the PAM8006's pins

(2) C17(V2P5), C14(AVDD) , and C19(VCLAMP) should be place closed as soon as possible

(3) Input resistors (Ri) and input capacitors (Ci) place closed to input pins as soon as possible

Grounding

(1) The decupling capacitors C17 (V2P5), C14(AVDD) ,C18/C19(AVCC) , should each to be grounded to analog ground AGND.

(2) The PVCC decoupling capacitors(C2, C3, C8, C9, C21,C22 , C27,and C28) should each be grounded to power ground PGND

(3) An AGND island should be created with a single connection to PGND

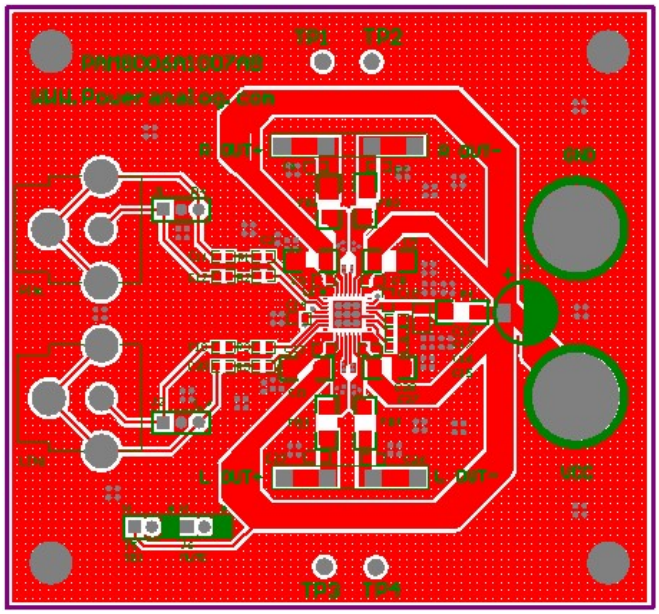
Output filter

(1) The ferrite EMI filter should be placed as close to the output terminals as possible for the best EMI performance

(2) The capacitors used in the filters should be grounded to PGND

11. PCB Layout Example

Top Layer



Bottom Layer