# PAM8003-EV Board User Guide

AE Department

## 1. Revision Information

| Date | Revision | Description | Comment |
|---|---|---|---|
| 2010/09/19 | V1.0 | Initial Release | |
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## 2. Key Features

- 2W Output at 10% THD with 4Ω Load and 5V Power Supply
- Filterless, Low Quiescent Current and Low EMI
- Low THD+N
- 64-step DC Volume Control
- Superior Low Noise
- Short Circuit Protection
- Thermal Shutdown
- Few External Components to Save the Space and Cost
- Pb-Free Package

## 3. EV Board Schematic

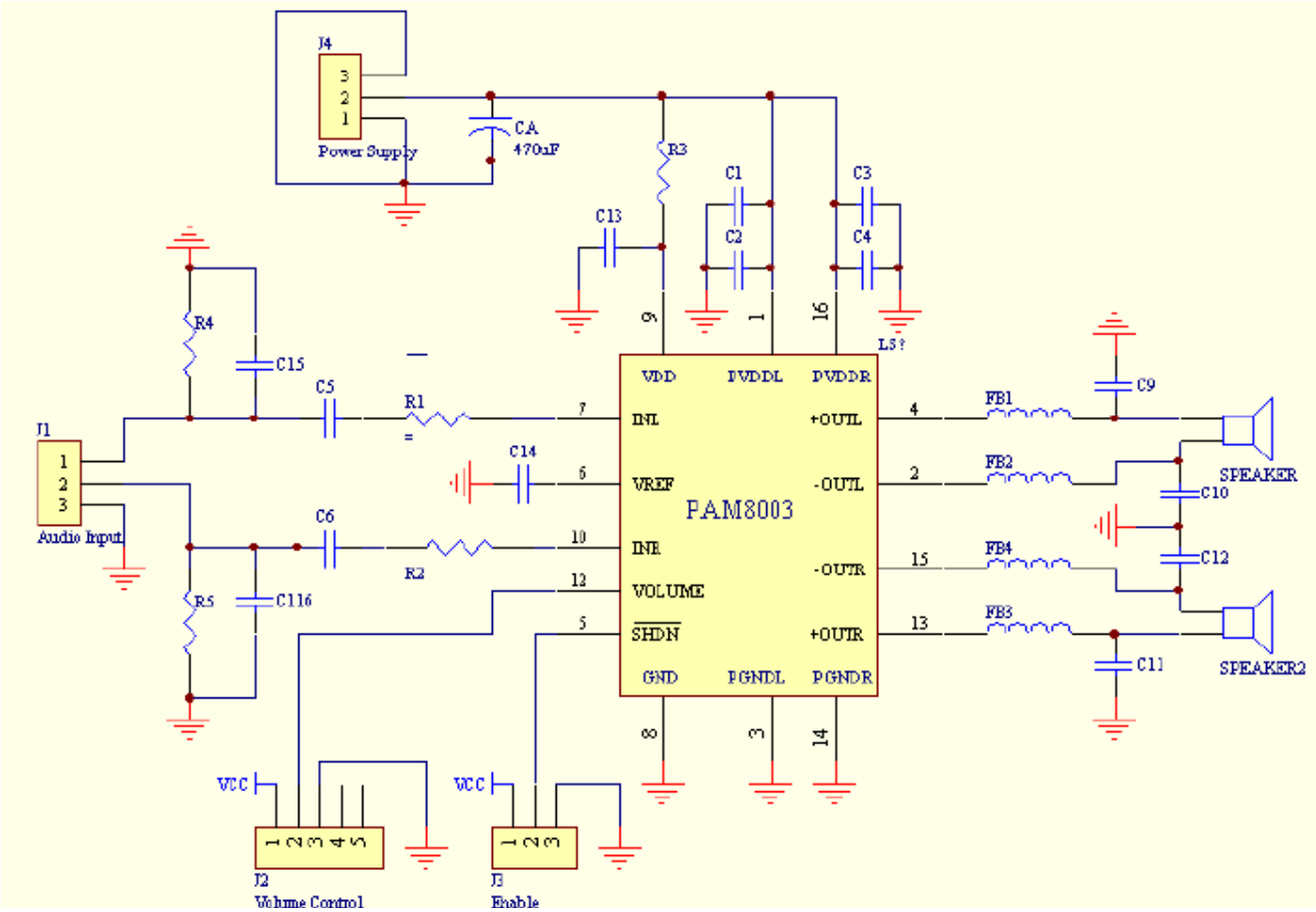
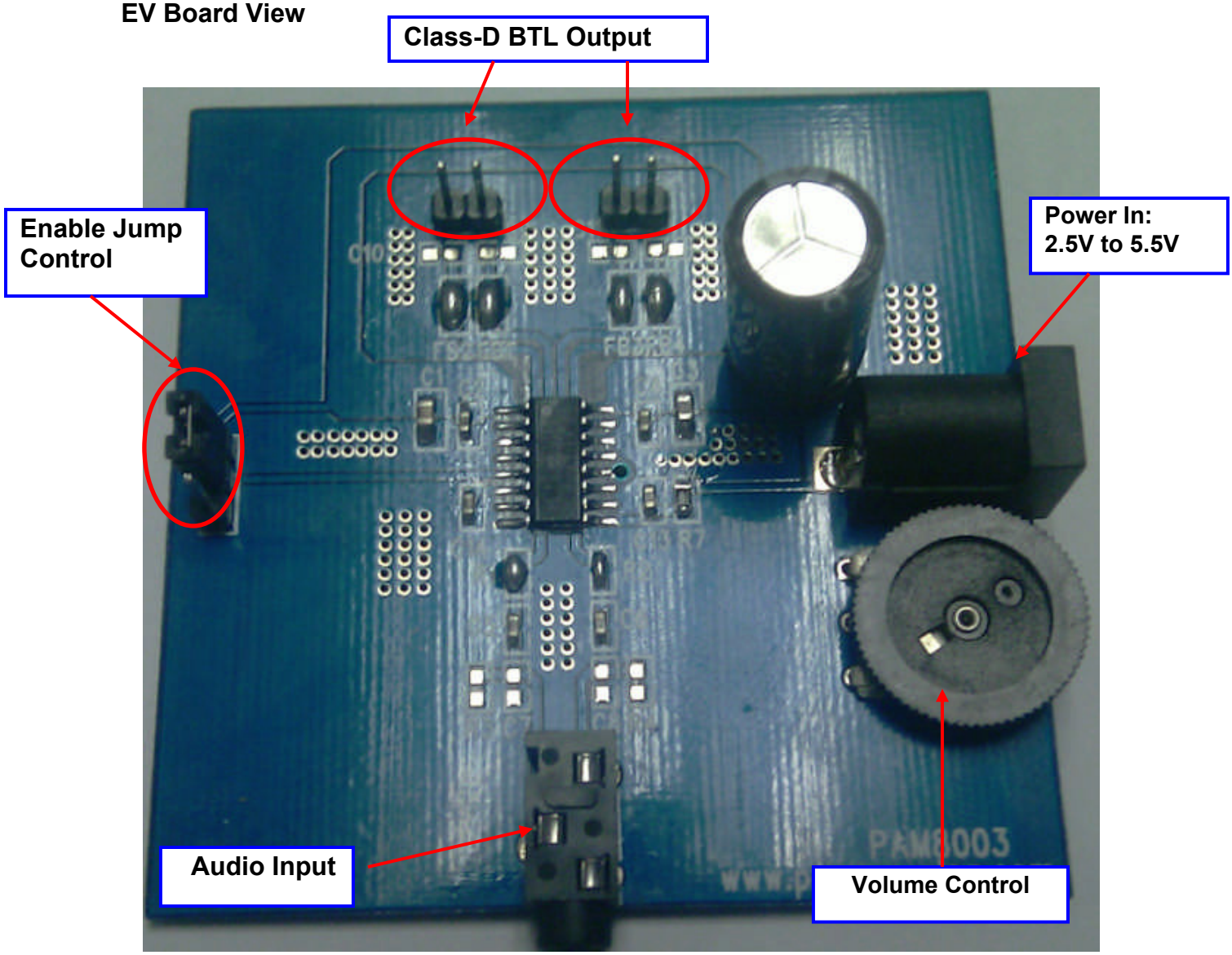



**Figure 1**

## 4. PAM8003 EB08AA Description

PAM8003 EB08AA is design for PAM8003 demo and evaluation, targeted to be used in providing a simple and convenient evaluation environment for the PAM8003. Requires parts, potentiometer for standard RCA jacks for audio inputs, pin jacks for power supply and signal outputs, volume and enable control, etc. on the board make it easy to be evaluated.

## EV Board View




## EV Board Operational Sequence:

a. Preset the power supply to between 2.5V and 5.5V.

b. Turn off the power supply.

c. Connect power supply to EV board power.

d. Connect audio input from audio input jack.

e. Connect the SPKs to the BTL output jack, 4ohm/8ohm speaker recommend.

f. Turn on the power supply, let enable pin at high level and verify that the sound quality of speaker.

## EV Board BOM List

| Item | Value | Type | Rating | Description |
|---|---|---|---|---|
| C1, C3 | 10μF | X5R/X7R, Ceramic/0805 | 10V | VDD decoupling CAP |
| C2, C4, C13 | 1μF | X5R/X7R, Ceramic/0603 | 10V | VDD coupling CAP |
| C14 | 1μF | X5R/X7R, Ceramic/0603 | 10V | VREF Bypass CAP |
| C9, C10, C11, C12 | 220pF | X5R/X7R, Ceramic/0603 | 10V | For EMI |
| C5, C6 | 1μF | X5R/X7R, Ceramic/0603 | 10V | Input coupling CAP |
| C8 | 1μF | X5R/X7R, Ceramic/0603 | 10V | CTRL decoupling CAP |
| R7 | 100Ω | 0805 | | Low-Pass Filter for VDD |
| FB1, FB2, FB3, FB4 | 2A/200Ω | 0805 | | EMI |

## 5. External Components Selection

**Input Capacitors (C5, C6)**

(1) Form a high pass filter with Ri, and the cut off frequency is fc=1/2ΠRi*Ci

(2) Have a tolerance of 10% or better for matching: any mismatch in capacitance causes an importance mismatch at the corner frequency.

(3) Low leakage current needed, 0.1μF, X5R/X7R ceramic.

**Power Supply decoupling Caps (C1, C2, C3, C4, C13)**

(1) Low ESR for good THD, PSRR.

(2) C2, C4 and C13 1uF ceramic for higher frequency transients, spikes.

(3) C1and C3 Additional 10uF or greater for low frequency noise filtering and serves as a local storage capacitor for supplying current during large signal transients on the amplifier outputs.

(4) Need place very closed to the IC.

**VREF Bypass Capacitor (C14)**

(1) 1μF ceramic recommended.

(2) Need place very closely to the pin for good THD, PSRR.

## 6. PCB Layout Guidelines

**Grounding**

(1) Use plane grounding or separate grounds

(2) Do not use one line connecting power GND and analog GND

(3) Output noise grounds must tie to system ground at the power in exclusively.

(4) Signal currents for the inputs need to be returned to quite ground. This ground only ties to the signal components and the GND pin.

**Power Supply**

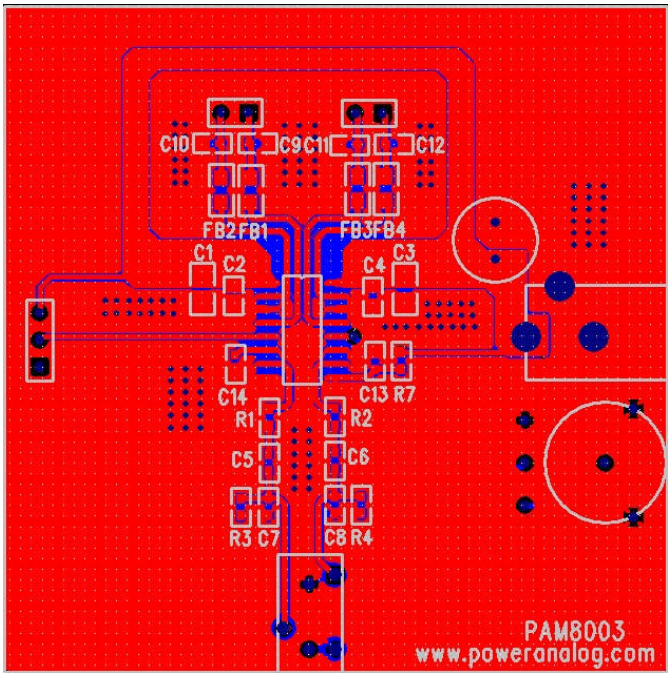
**Others**

(1) The power supply capacitors (C1, C2, C3, C4,C13) need to place very close to the PAM8003's pins.

(2) Input capacitors (C5, C6) place closed to input pin as near as possible

## 7. PCB Layout Example

**Top Layer**




**Bottom Layer**