DESCRIPTION

The AP63356Q/AP63357Q is a 3.5A, synchronous buck converter with a wide input voltage range of 3.8V to 32V and fully integrates an 74mΩ high-side power MOSFET and a 40mΩ low-side power MOSFET to provide high-efficiency step-down DC/DC conversion.

The AP63356Q/AP63357Q device is easily used by minimizing the external component count due to its adoption of peak current mode control along with the integrated compensation network.

The AP63356Q/AP63357Q has optimized design for Electromagnetic Interference (EMI) reduction. The converter features Frequency Spread Spectrum (FSS) with a switching frequency jitter of ±6%, which reduces EMI by not allowing emitted energy to stay in any one frequency for a significant period of time. It also has a proprietary gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off times, which reduces high-frequency radiated EMI noise caused by MOSFET switching.

The device is available in a 2x3mm W-QFN2030-13 package.

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results
  - Device Temperature Grade 1: -40C to 125C T_A Range
  - Device HBM ESD Classification Level H1C
  - Device CDM ESD Classification Level C3B
- VIN 3.8V to 32V
- 3.5A Continuous Output Current
- 0.8V ± 1% Reference Voltage
- 22μA Ultralow Quiescent Current (Pulse Frequency Modulation)
- 450kHz Switching Frequency
- Pulse Width Modulation (PWM) Regardless of Output Load
  - AP63356Q
- Supports Pulse Frequency Modulation (PFM)
  - AP63357Q
  - Up to 80% Efficiency at 1mA Light Load
  - Up to 87% Efficiency at 5mA Light Load
- Proprietary Gate Driver Design for Best EMI Reduction
- Frequency Spread Spectrum (FSS) to Reduce EMI
- Power Good Indicator with 5MΩ Internal Pull-up
- Precision Enable Threshold to Adjust UVLO
- Protection Circuitry
  - Undervoltage Lockout (UVLO)
  - Output Overvoltage Protection (OVP)
  - Output Undervoltage Protection (UVP)
  - Cycle-by-Cycle Peak Current Limit
  - Thermal Shutdown
- Totally Lead-Free & Fully RoHS Compliant Halogen and Antimony Free. “Green” Device

APPLICATIONS

- 12V and 24V Distributed Power Bus Supplies
- Flat Screen TV Sets and Monitors
- Power Tools and Laser Printers
- White Goods and Small Home Appliances
- FPGA, DSP, and ASIC Supplies
- Home Audio
- Network Systems
- Set Top Boxes
- Gaming Consoles

FUNCTIONAL BLOCK

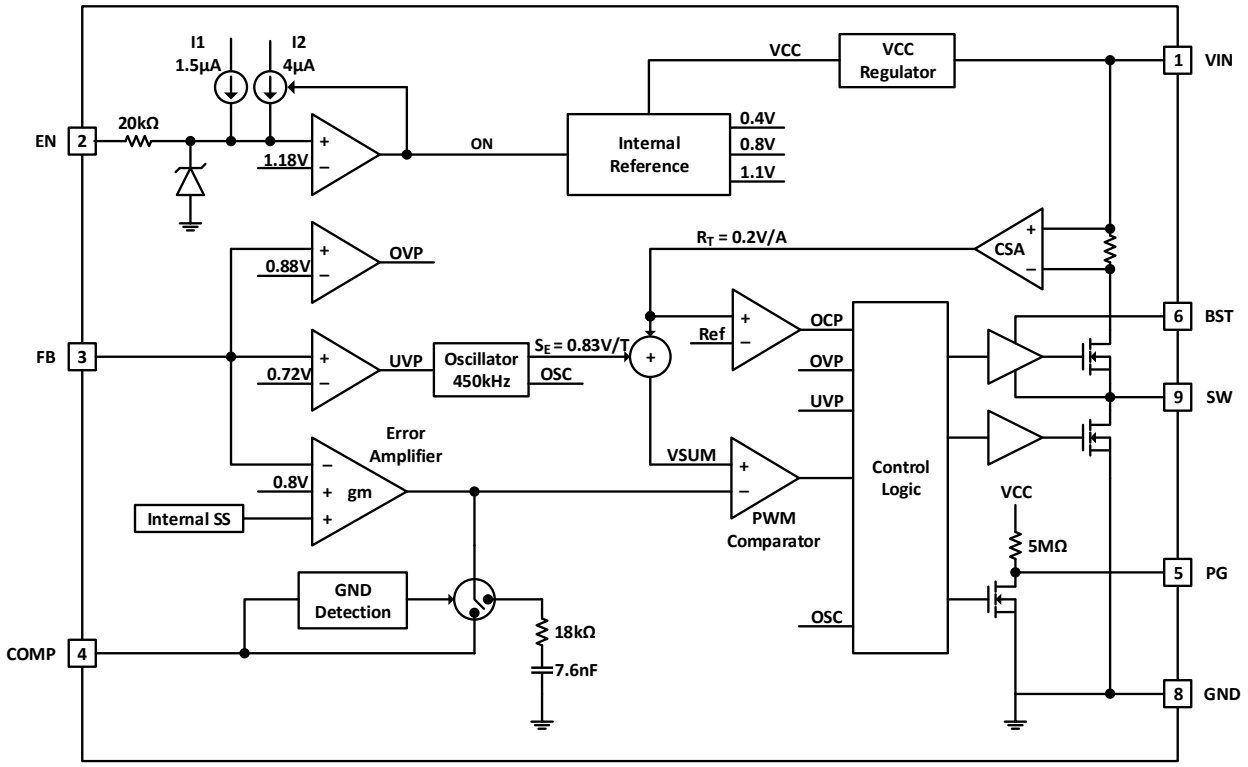


Figure 1. Functional Block Diagram

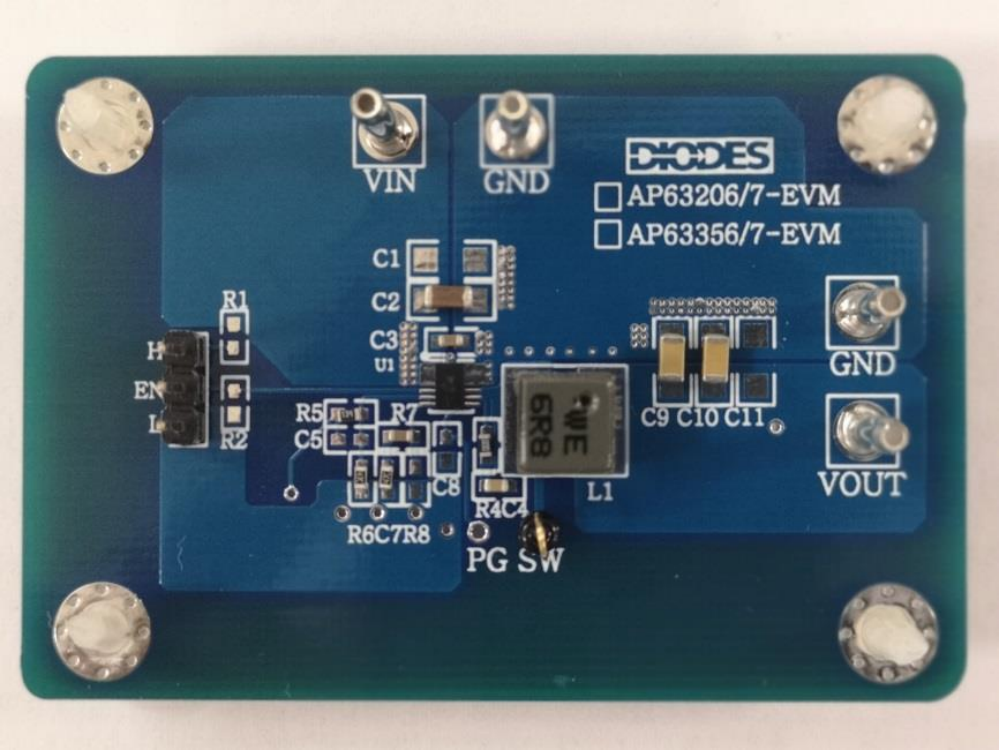
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VIN	Supply Pin Voltage	-0.3 to +35.0 (DC) -0.3 to +40.0 (400ms)	V
V_{EN}	Enable/UVLO Pin Voltage	-0.3 to +35.0	V
V_{FB}	Feedback Pin Voltage	-0.3 to +6.0	V
V_{COMP}	Compensation Pin Voltage	-0.3 to +6.0	V
V_{PG}	Power-Good Pin Voltage	-0.3 to +6.0	V
V_{BST}	Bootstrap Pin Voltage	V_{SW} - 0.3 to V_{SW} + 6.0	V
V_{SW}	Switch Pin Voltage	-1.0 to VIN + 0.3 (DC) -2.5 to VIN + 2.0 (20ns)	V
T_{ST}	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	+170	°C
T_L	Lead Temperature	+260	°C
ESD Susceptibility			
HBM	Human Body Mode	2000	V
CDM	Charge Device Model	1000	V

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
VIN	Supply Voltage	3.8	32	V
VOUT	Output Voltage	0.8	32	V
T_A	Operating Ambient Temperature Range	-40	+125	°C
T_J	Operating Junction Temperature Range	-40	+150	°C

EVALUATION BOARD



QUICK START GUIDE

The AP63356/7/Q-EVM has a simple layout and allows access to the appropriate signals through test points. To evaluate the performance of the AP63356/7/Q, follow the procedure below:

1. For evaluation board configured at V_{OUT}=12V, connect a power supply to the input terminals V_{IN} and GND. Set V_{IN} to 24V.
2. Connect the positive terminal of the electronic load to V_{OUT} and negative terminal to GND.
3. For Enable, place a jumper to “H” position to enable IC. Jump to “L” position to disable IC.
4. The evaluation board should now power up with a 12V output voltage.
5. Check for the proper output voltage of 12V (±1%) at the output terminals V_{OUT} and GND. Measurement can also be done with a multimeter with the positive and negative leads between V_{OUT} and GND.
6. Set the load to 2A through the electronic load. Check for the stable operation of the SW signal on the oscilloscope. Measure the switching frequency.

MEASUREMENT/PERFORMANCE GUIDELINES:

1) When measuring the output voltage ripple, maintain the shortest possible ground lengths on the oscilloscope probe. Long ground leads can erroneously inject high frequency noise into the measured ripple.

2) For efficiency measurements, connect an ammeter in series with the input supply to measure the input current. Connect an electronic load to the output for output current.

Setting the Output Voltage of AP63356/7

1) Setting the output voltage

The AP63356/7 features external programmable output voltage by using a resistor divider network R3 and R1 as shown in the typical application circuit. The output voltage is calculated as below,

$$V_{OUT} = 0.8 \times \left(\frac{R_5 + R_6}{R_6} \right)$$

First, select a value for R1 according to the value recommended in the table 1. Then, R3 is determined. The output voltage is given by Table 1 for reference. For accurate output voltage, 1% tolerance is required.

Table 1. Resistor selection for output voltage setting

Vo	R5	R6	C5(External/Internal Compensation)
1.0V	7.45K	30K	NC
3.3V	93.5KΩ	30 KΩ	33pF/33pF
5.0V	157 KΩ	30 KΩ	NC/47pF
12V	420 KΩ	30 KΩ	NC

EXTERNAL COMPONENT SELECTION:

1) Input & output Capacitors (Cin, Cout)
   (1) For lower output ripple, low ESR is required.
   (2) Low leakage current needed, X5R/X7R ceramic recommend, multiple capacitor parallel connection.
   (3) The Cin and Cout capacitances are greater than 10uF and 44uF respective. When set output voltage to 1.0V, 66uF Cout is recommended.

2) Bootstrap Voltage Regulator
   (1) An external 0.1uF ceramic capacitor is required as bootstrap capacitor between BST and SW pin to work as high side power MOSFET gate driver.

3) Compensation Capacitors and Resistors
   (1) For internal compensation: Connect Comp Pin to GND directly;
   (2) For external compensation: A resistor and a capacitor in series are connected from Comp Pin to GND, the value of resistor and capacitor is recommended refer to below table.

Output capacitor(uF)	Vo=3.3V		Vo=5.0V		Vo=1.0V/12V	
	R7(KΩ)	C7(nF)	R7(KΩ)	C7(nF)	R7(Ω)	C7(nF)
44	25	3.3	24	3.3	Internal compensation Recommended	
66	25	3.3	36	3.3	Internal compensation Recommended	

4) Inductor (L)
   (1) Low DCR for good efficiency
   (2) Inductance saturate current must higher than the output current
   (3) The recommended inductance is shown in the table 2 below.

Table 2. Recommended inductors

Output Voltage	1.0V	3.3 V	5.0 V	12 V
Co=44uF		4.7uH	6.8uH	
Co=66uF	2.2uH	6.8uH	6.8uH	10uH
Würth PART		744 393 460 47	744 393 460 68	
	744 393 440 22	744 393 460 68	744 393 460 68	744 393 461 00

EVALUATION BOARD SCHEMATIC

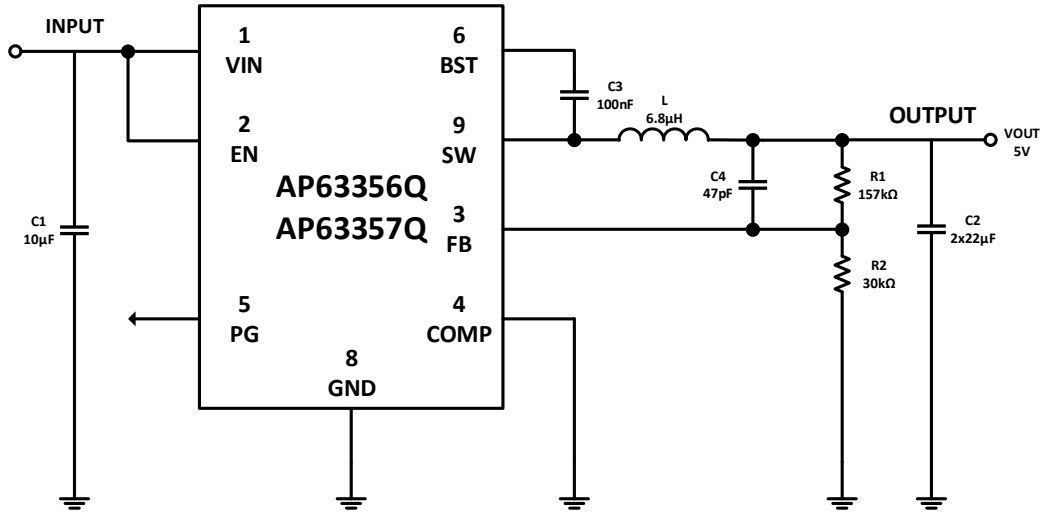


Figure 2. Typical Application Circuit

PCB TOP LAYOUT

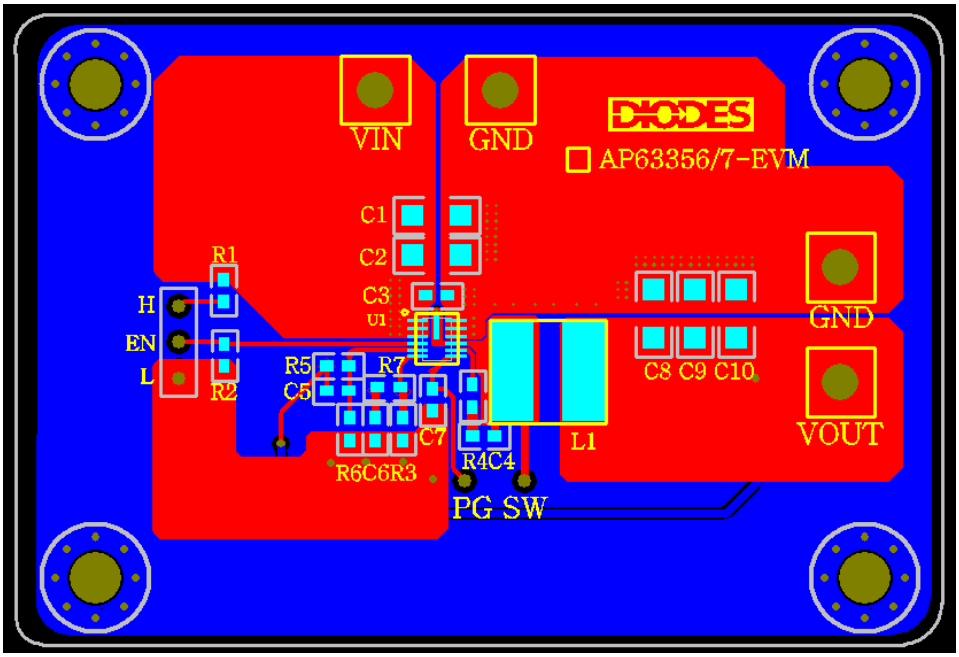


Figure 3. AP63356/7/Q-EVM – Top Layer

PCB BOTTOM LAYOUT

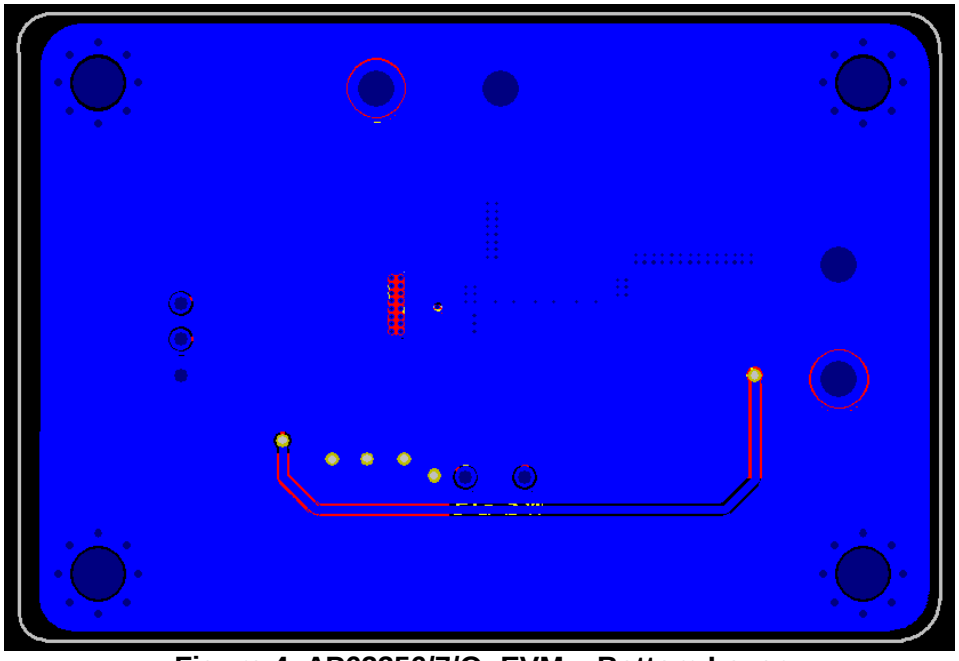


Figure 4. AP63356/7/Q -EVM – Bottom Layer

BILL OF MATERIALS for AP63356/7/Q-EVM (V_{OUT}=12V)

Item	Value	Type	Rating	Description
C2	10uF	X5R/X7R, Ceramic/1206	35V	Input CAP
C3	0.1uF	X5R/X7R, Ceramic/0603	50V	Input CAP
C4	0.1uF	X5R/X7R, Ceramic/0603	50V	Bootstrap CAP
C7	3.3nF	X5R/X7R, Ceramic/0603	50V	Comp CAP
C9 & C10	22uF	X5R/X7R, Ceramic/1206	25V	Output CAP
L1	6.8uH	6060	5.0A	Inductor
R1	100K	0603	1%	Enable RES
R4	0	0603	1%	Bootstrap RES
R5	157K	0603	1%	Voltage set RES*
R6	30K	0603	1%	
R7	36K	0603	1%	Comp RES
U1		AP63356/7		QFN

TYPICAL PERFORMANCE CHARACTERISTICS

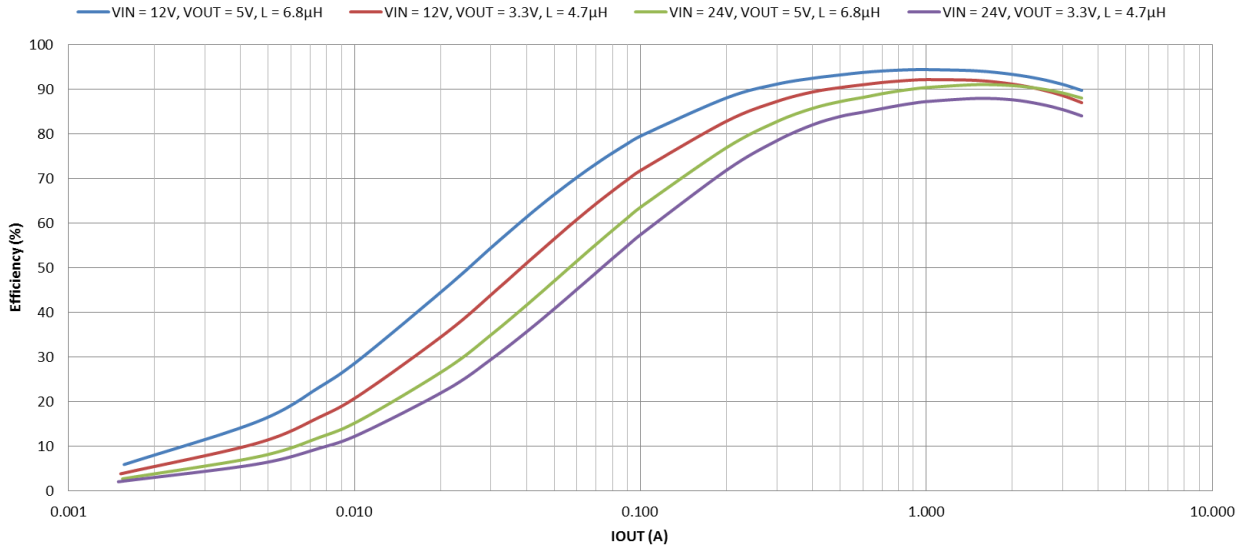


Figure 5. Efficiency vs. Output Current for AP63356Q

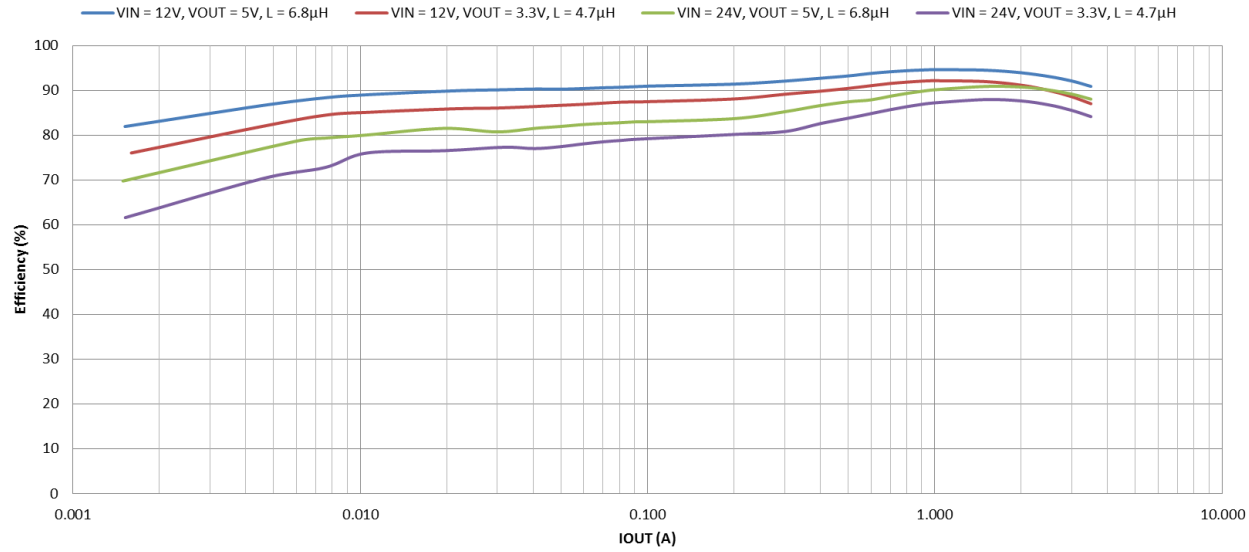


Figure 6. Efficiency vs. Output Current for AP63357Q

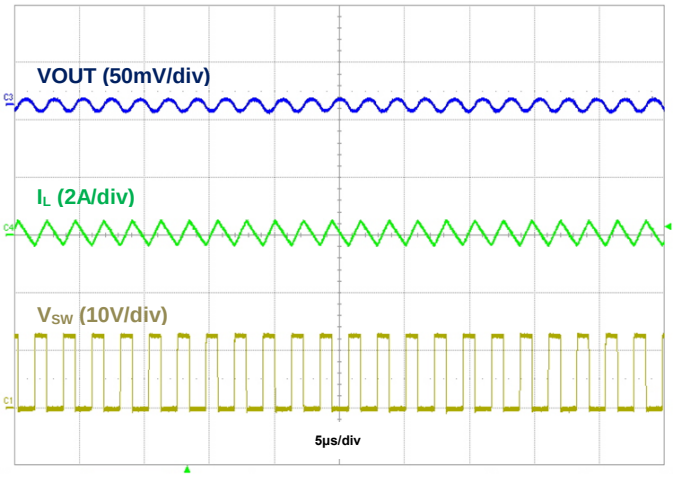


Figure 7. AP63356 Output Voltage Ripple, VIN = 12V, VOUT = 5V IOUT = 50mA

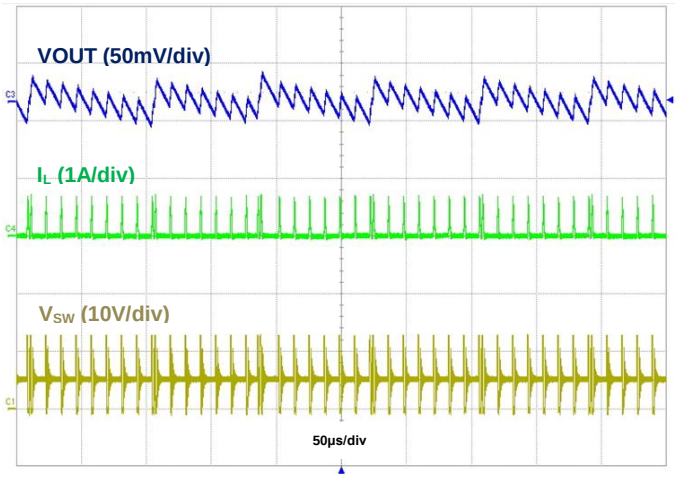


Figure 8. AP63357 Output Voltage Ripple, VIN = 12V, VOUT = 5V IOUT = 50mA

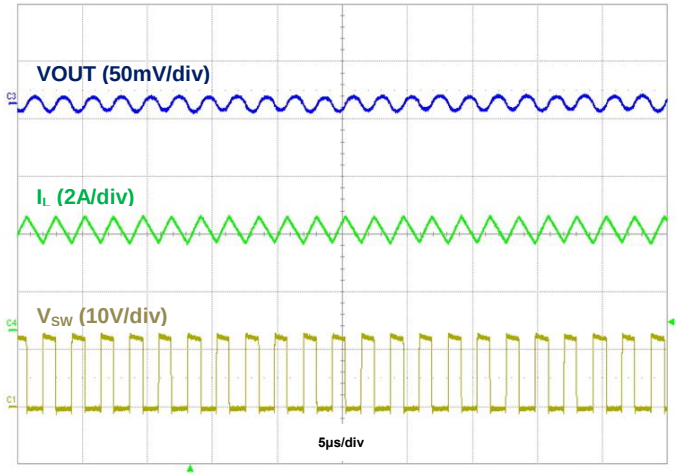


Figure 9. AP63356/7 Output Voltage Ripple, VIN = 12V, VOUT = 5V IOUT = 3.5A

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