Description

The AP63300Q is a 3A, synchronous buck converter with a wide input voltage range of 3.8V to 32V. The device fully integrates a 75mΩ high-side power MOSFET and a 40mΩ low-side power MOSFET to provide high-efficiency step-down DC-DC conversion.

The AP63300Q device is easily used by minimizing the external component count due to its adoption of peak current mode control along with its integrated loop compensation network.

Features

- VIN 3.8V to 32V
- 3A Continuous Output Current
- 0.8V ± 1% Reference Voltage
- 22µA Ultralow Quiescent Current (Pulse Frequency Modulation)
- 500kHz Switching Frequency
- Supports Pulse Frequency Modulation (PFM)
  - Up to 88% Efficiency at 5mA Light Load
- Proprietary Gate Driver Design for Best EMI Reduction
- Frequency Spread Spectrum (FSS) to Reduce EMI
- Low-Dropout (LDO) Mode
- Precision Enable Threshold to Adjust UVLO
- Protection Circuitry
  - Undervoltage Lockout (UVLO)
  - Output Overvoltage Protection (OVP)
  - Cycle-by-Cycle Peak Current Limit
  - Thermal Shutdown

The AP63300Q design is optimized for Electromagnetic Interference (EMI) reduction. The device has a proprietary gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off times, which reduces high-frequency radiated EMI noise caused by MOSFET switching. AP63300Q also features Frequency Spread Spectrum (FSS) with a switching frequency jitter of ±6%, which reduces EMI by not allowing emitted energy to stay in any one frequency for a significant period of time.

The device is available in a TSOT26 package.
AP63300QWU-EVM
3.8V TO 32V INPUT, 3A LOW IQ SYNCHRONOUS BUCK WITH ENCHANCED EMI REDUCTION

APPLICATIONS

- 5V, 12V, and 24V Distributed Power Bus Supplies
- FPGA, DSP, and ASIC Supplies
- Flat Screen TV Sets and Monitors
- White Goods and Small Home Appliances
- Home Audio
- Network Systems
- Consumer Electronics
- Cordless Power Tools
- Optical Communication and Networking Systems
- General Purpose Point of Load

FUNCTIONAL BLOCK

![Functional Block Diagram]

Figure 1. Functional Block Diagram
# ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>Supply Pin Voltage</td>
<td>-0.3 to +35.0 (DC)</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-0.3 to +40.0 (400ms)</td>
<td></td>
</tr>
<tr>
<td>VFB</td>
<td>Feedback Voltage</td>
<td>-0.3 to +6.0</td>
<td>V</td>
</tr>
<tr>
<td>VEN</td>
<td>Enable/UVLO Pin Voltage</td>
<td>-0.3 to +35.0</td>
<td>V</td>
</tr>
<tr>
<td>VSW</td>
<td>Switch Node Voltage</td>
<td>-0.3 to VIN + 0.3 (DC)</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-2.5 to VIN + 2.0 (20ns)</td>
<td>V</td>
</tr>
<tr>
<td>VBST</td>
<td>Bootstrap Pin Voltage</td>
<td>VSW - 0.3 to VSW + 6.0</td>
<td>V</td>
</tr>
<tr>
<td>TST</td>
<td>Storage Temperature</td>
<td>-65 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>TJ</td>
<td>Junction Temperature</td>
<td>+160</td>
<td>°C</td>
</tr>
<tr>
<td>TL</td>
<td>Lead Temperature</td>
<td>+260</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>ESD Susceptibility (Note 5)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>HBM</td>
<td>Human Body Mode</td>
<td>2000</td>
<td>V</td>
</tr>
<tr>
<td>CDM</td>
<td>Charged Device Model</td>
<td>1000</td>
<td>V</td>
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# RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>Supply Voltage</td>
<td>3.8</td>
<td>32</td>
<td>V</td>
</tr>
<tr>
<td>VOUT</td>
<td>Output Voltage</td>
<td>0.8</td>
<td>31</td>
<td>V</td>
</tr>
<tr>
<td>TA</td>
<td>Operating Ambient Temperature Range</td>
<td>-40</td>
<td>+125</td>
<td>°C</td>
</tr>
<tr>
<td>TJ</td>
<td>Operating Junction Temperature Range</td>
<td>-40</td>
<td>+150</td>
<td>°C</td>
</tr>
</tbody>
</table>
EVALUATION BOARD

Figure 2. Top Picture of AP63300QWU-EVM Board

QUICK START GUIDE

The AP63300QWU-EVM has a simple layout and allows access to the appropriate signals through test points. To evaluate the performance of the AP63300Q, follow the procedure below:

1. For evaluation board configured at V_{OUT}=5V, connect a power supply to the input terminals V_{IN} and GND. Set V_{IN} to 12V.

2. Connect the positive terminal of the electronic load to V_{OUT} and negative terminal to GND.

3. For Enable, place a jumper to “H” position to enable IC. Jump to “L” position to disable IC.

4. The evaluation board should now power up with a 5V output voltage.

5. Check for the proper output voltage of 5V (±1%) at the output terminals V_{OUT} and GND. Measurement can also be done with a multimeter with the positive and negative leads between V_{OUT} and GND.

6. Set the load to 3A through the electronic load. Check for the stable operation of the SW signal on the oscilloscope. Measure the switching frequency.
MEASUREMENT/PERFORMANCE GUIDELINES:

1) When measuring the output voltage ripple, maintain the shortest possible ground lengths on the oscilloscope probe. Long ground leads can erroneously inject high frequency noise into the measured ripple.

2) For efficiency measurements, connect an ammeter in series with the input supply to measure the input current. Connect an electronic load to the output for output current.

Setting the Output Voltage of AP63300Q

1) Setting the output voltage:
   The AP63300Q features external programmable output voltage by using a resistor divider network R3 and R1 as shown in the typical application circuit. The output voltage is calculated as below,

   \[
   V_{\text{OUT}} = 0.8 \times \frac{R_1 + R_3}{R_1} \]

   First, select a value for R1 according to the value recommended in the table 1. Then, R3 is determined. The output voltage is given by Table 1 for reference. For accurate output voltage, 1% tolerance is required.

2) Output feed-forward capacitor selection:
   The AP63300Q has the internal integrated loop compensation as shown in the function block diagram. The compensation network includes a 18k resistor and a 7.6nF capacitor. Usually, the type II compensation network has a phase margin between 60 and 90 degree. However, if the output capacitor has ultra-low ESR, the converter results in low phase margin. To increase the converter phase margin, a feed-forward cap C4 is used to boost the phase margin at the converter cross-over frequency \( f_c \). The feed-forward capacitor is given by Table 1 for reference. The feed-forward capacitor is calculated as below,

   \[
   C_{ff} = \frac{1}{2\pi \times f_c \times R_3} \]

Table 1. Resistor selection for output voltage setting

<table>
<thead>
<tr>
<th>Vo</th>
<th>R3</th>
<th>R1</th>
<th>C4</th>
<th>C6-C8</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.8V</td>
<td>77.5 KΩ</td>
<td>62 KΩ</td>
<td>100pF</td>
<td>22μFx2</td>
</tr>
<tr>
<td>2.5V</td>
<td>131 KΩ</td>
<td>62 KΩ</td>
<td>100pF</td>
<td>22μFx2</td>
</tr>
<tr>
<td>3.3V</td>
<td>182 KΩ</td>
<td>62 KΩ</td>
<td>100pF</td>
<td>22μFx2</td>
</tr>
<tr>
<td>5V</td>
<td>157 KΩ</td>
<td>30 KΩ</td>
<td>100 pF</td>
<td>22μFx2</td>
</tr>
<tr>
<td>12V</td>
<td>249 KΩ</td>
<td>18 KΩ</td>
<td>56 pF</td>
<td>22μFx4</td>
</tr>
</tbody>
</table>
EXTERNAL COMPONENT SELECTION:

1) Input & output Capacitors (Cin, Cout):
   (1) For lower output ripple, low ESR is required.
   (2) Low leakage current needed, multiple capacitor parallel connection.
   (3) The Cin and Cout capacitances are greater than 10µF and 44µF respective.

2) Bootstrap Voltage Regulator:
   An external 0.1µF ceramic capacitor is required as bootstrap capacitor between BST and SW pins to work as high-side power MOSFET gate driver.

3) Inductor (L):
   (1) Low DCR for good efficiency
   (2) Inductance saturate current must higher than the output current
   (3) The recommended inductance is shown in the table 2 below.

EVALUATION BOARD SCHEMATIC

![EVALUATION BOARD SCHEMATIC](image)

Figure 3. Typical Application Circuit
PCB TOP LAYOUT

![PCB Top Layout](image1.png)

Figure 4. AP63300QWU-EVM – Top Layer

PCB BOTTOM LAYOUT

![PCB Bottom Layout](image2.png)

Figure 5. AP63300QWU-EVM – Bottom Layer
### BILL OF MATERIALS for AP63300QWU-EVM

#### Table 2

<table>
<thead>
<tr>
<th>Item</th>
<th>Value</th>
<th>Type</th>
<th>Rating</th>
<th>Description</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C2</td>
<td>10µF</td>
<td>X7R, Ceramic/1206</td>
<td>35V</td>
<td>Input CAP</td>
<td>TDK CGA5L1X7R1V106K160AC</td>
</tr>
<tr>
<td>C3</td>
<td>0.1µF</td>
<td>X8R, Ceramic/0603</td>
<td>50V</td>
<td>Input CAP</td>
<td>TDK CGA3E3X8R1H104K080AB</td>
</tr>
<tr>
<td>C4</td>
<td>100pF</td>
<td>C0G, Ceramic/0603</td>
<td>50V</td>
<td>Feedback CAP</td>
<td>TDK CGA3E2C0G1H101J080AA</td>
</tr>
<tr>
<td>C5</td>
<td>0.1µF</td>
<td>X8R, Ceramic/0603</td>
<td>50V</td>
<td>Bootstrap CAP</td>
<td>TDK CGA3E3X8R1H104K080AB</td>
</tr>
<tr>
<td>C6 &amp; C7</td>
<td>22µF</td>
<td>X7R, Ceramic/1206</td>
<td>10V</td>
<td>Output CAP</td>
<td>TDK CGA5L1X7S1A226M160AC</td>
</tr>
<tr>
<td>L1</td>
<td>6.8µH</td>
<td>6060</td>
<td>6.5A</td>
<td>Inductor</td>
<td>Würth PART 744 393 690 68</td>
</tr>
<tr>
<td>R1</td>
<td>30K</td>
<td>0603</td>
<td>1%</td>
<td>Voltage set RES*</td>
<td></td>
</tr>
<tr>
<td>R3</td>
<td>162K</td>
<td>0603</td>
<td>1%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R4</td>
<td>0</td>
<td>0603</td>
<td>1%</td>
<td>Bootstrap RES</td>
<td></td>
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<tr>
<td>R5</td>
<td>100K</td>
<td>0603</td>
<td>1%</td>
<td>EN pull high RES</td>
<td></td>
</tr>
<tr>
<td>U1</td>
<td>AP63300Q</td>
<td>TSOT23-6</td>
<td></td>
<td>Diodes Incorporated BCD</td>
<td></td>
</tr>
</tbody>
</table>

*Note: The present value of R3/R1 are based on Vout=5.0V*
TYPICAL PERFORMANCE CHARACTERISTICS

Figure 6. AP63300Q Efficiency vs. Output Current

Figure 7. AP63300Q Vin=12V, Vout=5V Output Voltage Ripple, IOUT = 3A
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