

### **DESCRIPTION**

The AP63200 is a 2A, synchronous buck converter with a wide input voltage range of 3.8V to 32V and fully integrates a 125mΩ high-side power MOSFET and a 68mΩ low-side power MOSFET to provide high-efficiency step-down DC/DC conversion.

The AP63200 device is easily used by minimizing the external component count due to its adoption of peak current mode control along with its integrated compensation network.

The AP63200 has optimized designs for Electromagnetic Interference (EMI) reduction. The converter features Frequency Spread Spectrum (FSS) with a

switching frequency jitter of  $\pm 6\%$ , which reduces EMI by not allowing emitted energy to stay in any one frequency for a significant period of time. It also has a proprietary gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off times, which further reduces high-frequency radiated EMI noise caused by MOSFET switching.

The device is available in a low-profile, TSOT26 package.

### **FEATURES**

- VIN 3.8V to 32V
- 2A Continuous Output Current
- $0.8V \pm 1\%$  Reference Voltage
- 22μA Ultralow Quiescent Current (Pulse Frequency Modulation)
- 500kHz Switching Frequency
- Supports Pulse Frequency Modulation (PFM) and Pulse Width Modulation (PWM)
- Proprietary Gate Driver Design for Best EMI Reduction
- Frequency Spread Spectrum (FSS) to Reduce EMI
- Low-Dropout (LDO) Mode
- Precision Enable Threshold to Adjust UVLO
- Protection Circuitry
  - Undervoltage Lockout (UVLO)
  - Cycle-by-Cycle Peak Current Limit
  - Thermal Shutdown

### APPLICATIONS

- 12V and 24V Distributed Power Bus Supplies
- Flat Screen TV Sets and Monitors
- Power Tools and Laser Printers
- White Goods and Small Home Appliances
- FPGA, DSP, and ASIC Supplies
- Home Audio
- Network Systems
- Set Top Boxes
- Gaming Consoles
- Consumer Electronics

### FUNCTIONAL BLOCK

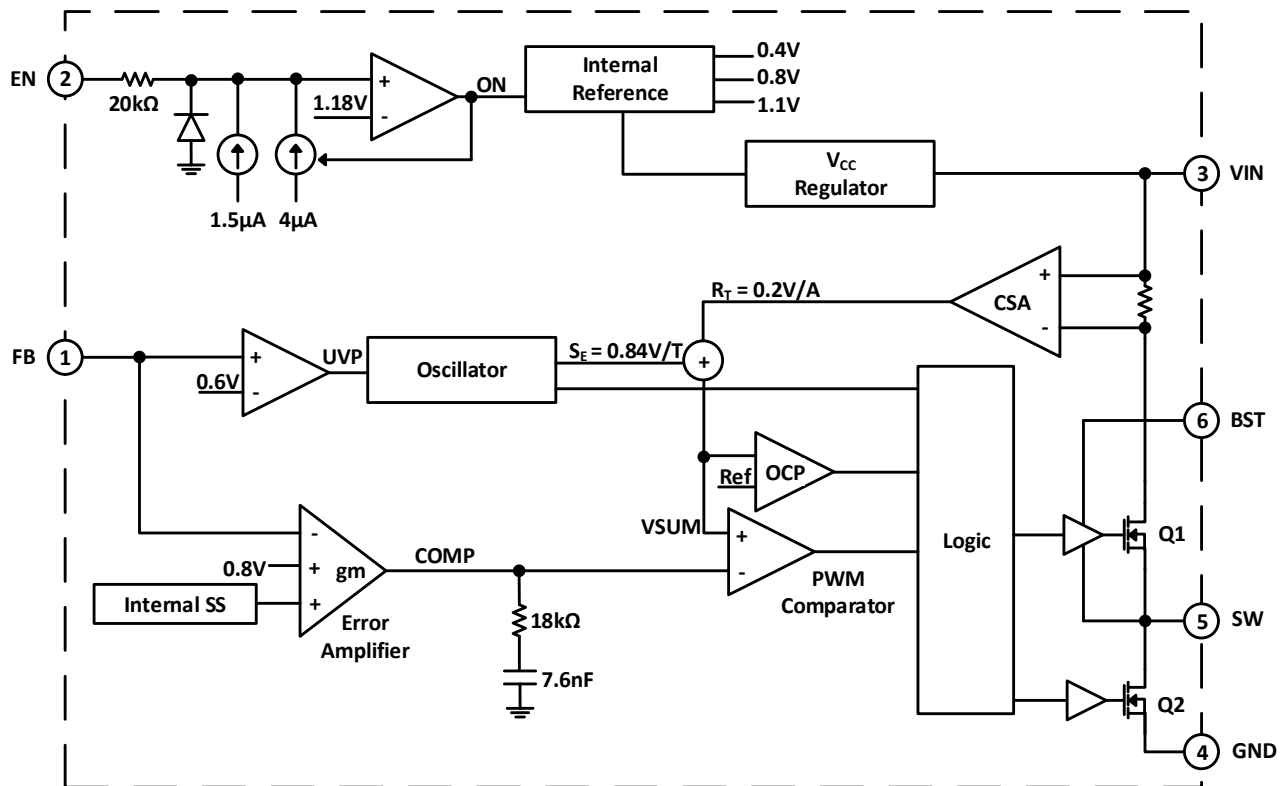


Figure 1. Functional Block Diagram

### ABSOLUTE MAXIMUM RATINGS

| Symbol                    | Parameter            | Rating                           | Unit |
|---------------------------|----------------------|----------------------------------|------|
| $V_{IN}$                  | Supply Voltage       | -0.3 to +35.0 (DC)               | V    |
|                           |                      | -0.3 to +40.0 (400ms)            |      |
| $V_{SW}$                  | Switch Node Voltage  | -1.0 to $V_{IN} + 0.3$ (DC)      | V    |
|                           |                      | -2.5 to $V_{IN} + 2.0$ (20ns)    |      |
| $V_{BST}$                 | Bootstrap Voltage    | $V_{SW} - 0.3$ to $V_{SW} + 6.0$ | V    |
| $V_{FB}$                  | Feedback Voltage     | -0.3 to +6.0                     | V    |
| $V_{EN}$                  | Enable/UVLO Voltage  | -0.3 to +35.0                    | V    |
| $T_{ST}$                  | Storage Temperature  | -65 to +150                      | °C   |
| $T_J$                     | Junction Temperature | +150                             | °C   |
| $T_L$                     | Lead Temperature     | +260                             | °C   |
| <b>ESD Susceptibility</b> |                      |                                  |      |
| HBM                       | Human Body Mode      | 2000                             | V    |
| CDM                       | Charge Device Model  | 1000                             | V    |

### RECOMMENDED OPERATING CONDITIONS

| Symbol   | Parameter                            | Min | Max  | Unit |
|----------|--------------------------------------|-----|------|------|
| $V_{IN}$ | Supply Voltage                       | 3.8 | 32   | V    |
| $T_A$    | Operating Ambient Temperature Range  | -40 | +85  | °C   |
| $T_J$    | Operating Junction Temperature Range | -40 | +125 | °C   |

**EVALUATION BOARD****Figure 2. AP63200WU-EVM****QUICK START GUIDE**

The AP63200WU-EVM has a simple layout and allows access to the appropriate signals through test points. To evaluate the performance of the AP63200WU, follow the procedure below:

1. For evaluation board configured at  $V_{OUT}=12V$ , connect a power supply to the input terminals  $V_{IN}$  and GND. Set  $V_{IN}$  to 24V.
2. Connect the positive terminal of the electronic load to  $V_{OUT}$  and negative terminal to GND.
3. For Enable, place a jumper to “H” position to enable IC. Jump to “L” position to disable IC.
4. The evaluation board should now power up with a 12V output voltage.
5. Check for the proper output voltage of 12V ( $\pm 1\%$ ) at the output terminals  $V_{OUT}$  and GND. Measurement can also be done with a multimeter with the positive and negative leads between  $V_{OUT}$  and GND.
6. Set the load to 2A through the electronic load. Check for the stable operation of the SW signal on the oscilloscope. Measure the switching frequency.

### MEASUREMENT/PERFORMANCE GUIDELINES:

- 1) When measuring the output voltage ripple, maintain the shortest possible ground lengths on the oscilloscope probe. Long ground leads can erroneously inject high frequency noise into the measured ripple.
- 2) For efficiency measurements, connect an ammeter in series with the input supply to measure the input current. Connect an electronic load to the output for output current.

### EXTERNAL COMPONENT SELECTION:

#### (1) Setting the output voltage:

The AP63200WU features external programmable output voltage by using a resistor divider network R3 and R1 as shown in the typical application circuit. The output voltage is calculated as below,

$$V_{OUT} = 0.8 \times \left( \frac{R_1 + R_3}{R_1} \right)$$

First, select a value for R1 according to the value recommended in the table 1. Then, R3 is determined. The output voltage is given by Table 1 for reference. For accurate output voltage, 1% tolerance is required.

#### (2) Output feed-forward capacitor selection:

The AP63200WU has the internal integrated loop compensation as shown in the function block diagram. The compensation network includes an 18k resistor and a 7.6nF capacitor. Usually, the type II compensation network has a phase margin between 60 and 90 degrees. However, if the output capacitor has ultra-low ESR, the converter results in low phase margin. To increase the converter phase margin, a feed-forward cap C4 is used to boost the phase margin at the converter cross-over frequency,  $f_c$ . The feed-forward capacitor is given by Table 1 for reference. The feed-forward capacitor is calculated as below,

$$C_4 = \frac{1}{2\pi \times f_c \times R_3}$$

| V <sub>OUT</sub> | R3      | R1    | C4     | C6-C8  |
|------------------|---------|-------|--------|--------|
| 1.8V             | 77.5 KΩ | 62 KΩ | 100pF  | 22uFx2 |
| 2.5V             | 131 KΩ  | 62 KΩ | 100pF  | 22uFx2 |
| 3.3V             | 182 KΩ  | 62 KΩ | 100 pF | 22uFx2 |
| 5V               | 157 KΩ  | 30 KΩ | 100 pF | 22uFx2 |
| 12V              | 249 KΩ  | 18 KΩ | 56 pF  | 22uFx4 |

**Table 1. Resistor selection for common output voltages**

### (3) External Component Selection

#### a) Input & output Capacitors ( $C_{IN}$ , $C_{OUT}$ )

- (1) For lower output ripple, low ESR is required.
- (2) For low leakage current, X5R/X7R ceramic is recommend in multiple capacitor parallel connections.
- (3) The  $C_{IN}$  capacitances are greater than 10 $\mu$ F.
- (4) 44 $\mu$ F ceramic output capacitors are recommended to work for most applications, due to a capacitor's de-rating under DC bias, The 88 $\mu$ F is recommend for high output voltage condition. The output capacitor selection is shown in table1.

#### b) Bootstrap Capacitor

An external 0.1 $\mu$ F ceramic capacitor is required as bootstrap capacitor between BST and SW pin to work as high side power MOSFET gate driver.

#### c) Inductor (L)

- (1) Low DCR for good efficiency
- (2) Inductance saturate current must higher than the output current.
- (3) The recommended inductance values are shown in table 2.

Table 2 shows a list of recommended inductors for common output voltages.

| $V_{OUT}$  | 1.8V           | 2.5V           | 3.3V           | 5.0V           | 12V           |
|------------|----------------|----------------|----------------|----------------|---------------|
| Inductor   | 3.3 $\mu$ H    | 3.3 $\mu$ H    | 6.8 $\mu$ H    | 10 $\mu$ H     | 15 $\mu$ H    |
| Würth Part | 744 393 440 33 | 744 393 440 33 | 744 393 460 68 | 744 393 461 00 | 744 770 915 0 |

Table 2. Recommended Inductor Selection

### EVALUATION BOARD SCHEMATIC

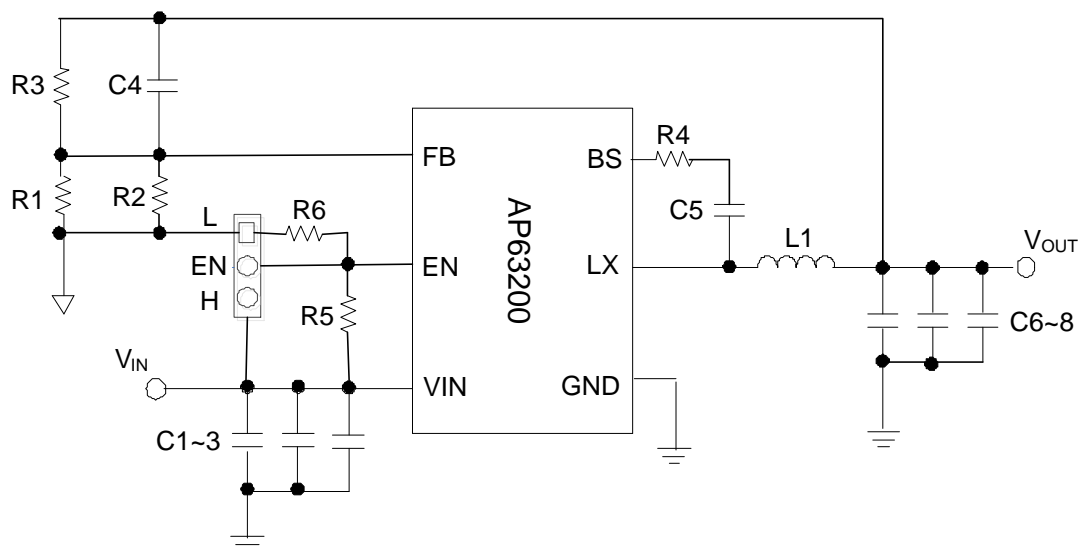


Figure 3. AP63200WU-EVM Schematic

**PCB TOP LAYOUT**

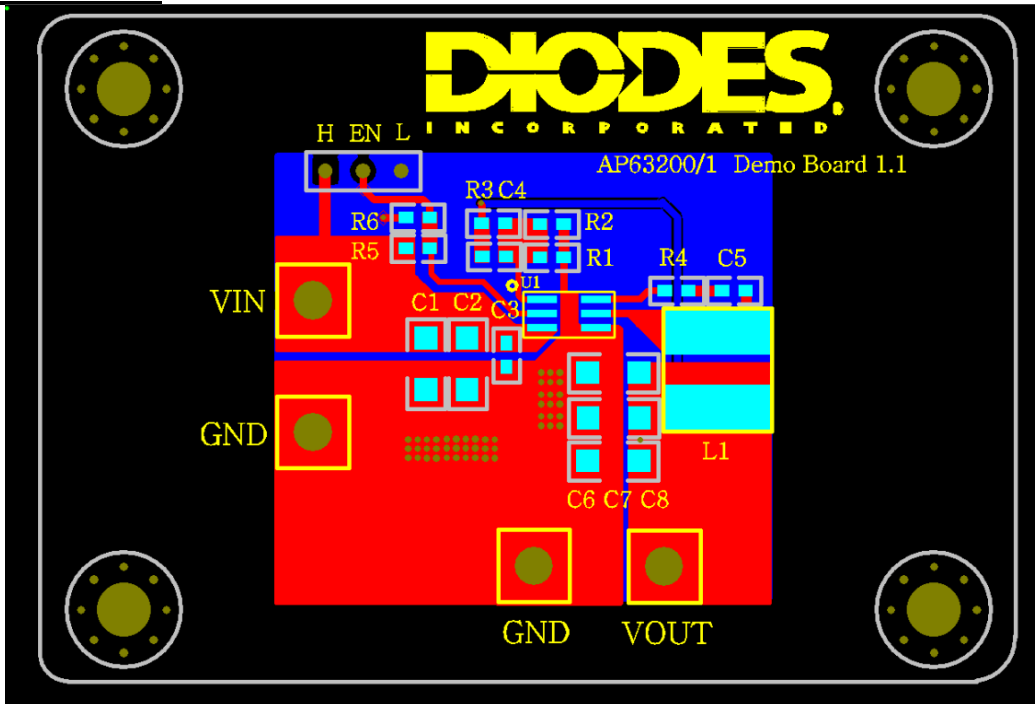


Figure 4. AP63200WU-EVM – Top Layer

**PCB BOTTOM LAYOUT**

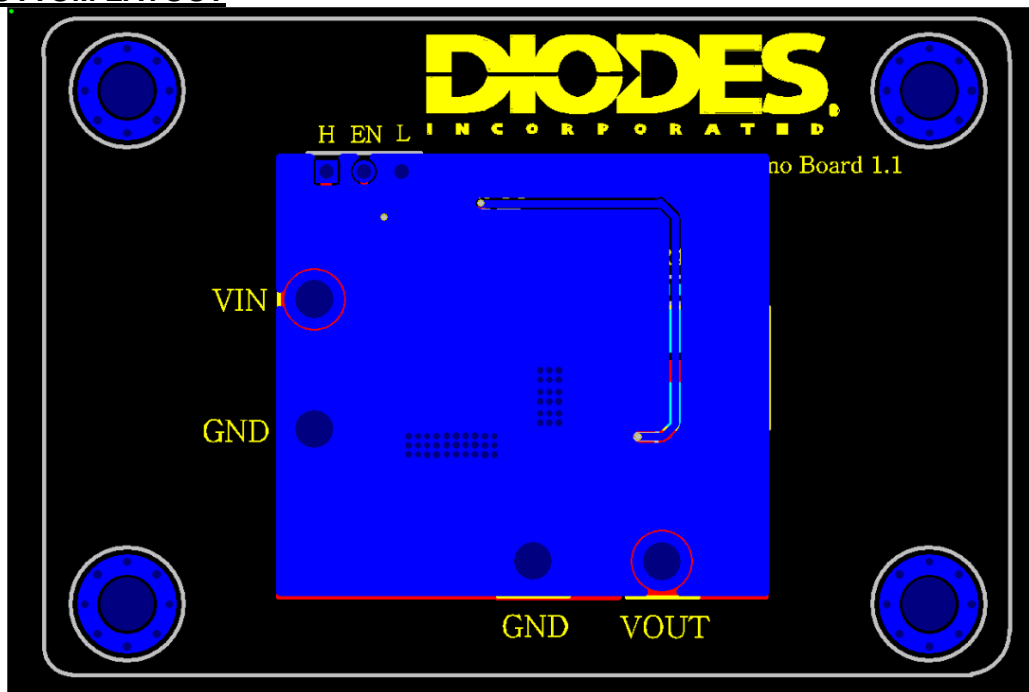


Figure 5. AP63200WU-EVM – Bottom Layer

### BILL OF MATERIALS for AP63200WU-EVM (V<sub>OUT</sub>=12V)

| Item       | Value   | Type                     | Rating | Description   | Manufacturer                         |
|------------|---------|--------------------------|--------|---------------|--------------------------------------|
| C2         | 10uF    | X5R/X7R,<br>Ceramic/1206 | 35V    | Input CAP     |                                      |
| C3         | 0.1uF   | X5R/X7R,<br>Ceramic/0603 | 50V    | Input CAP     | Würth Electronics<br>885 012 206 095 |
| C4         | 56pF    | 0603                     | 100V   | Feedback CAP  |                                      |
| C5         | 0.1uF   | X5R/X7R,<br>Ceramic/0603 | 50V    | Bootstrap CAP | Würth Electronics<br>885 012 206 095 |
| C6, C7, C8 | 22uF x4 | X5R/X7R,<br>Ceramic/1206 | 25V    | Output CAP*   |                                      |
| L1         | 15uH    | SMD                      | 6.5A   | Inductor*     | Würth Electronics<br>7447709150      |
| R1         | 18KΩ    | 0603                     | 1%     | Voltage RES*  |                                      |
| R3         | 249KΩ   | 0603                     | 1%     |               |                                      |
| R4         | 0       | 0603                     | 1%     | Bootstrap RES |                                      |
| U1         |         | AP63200WU                |        | TSOT26        | Diodes Inc                           |

\*Note: The present values of R3/R1, C6, C7, C8, L1 are based on V<sub>OUT</sub>=12V



**TYPICAL PERFORMANCE CHARACTERISTICS**

Figure 6. Efficiency for VIN=12V, VOUT=1.8V / 3.3V / 5.0V

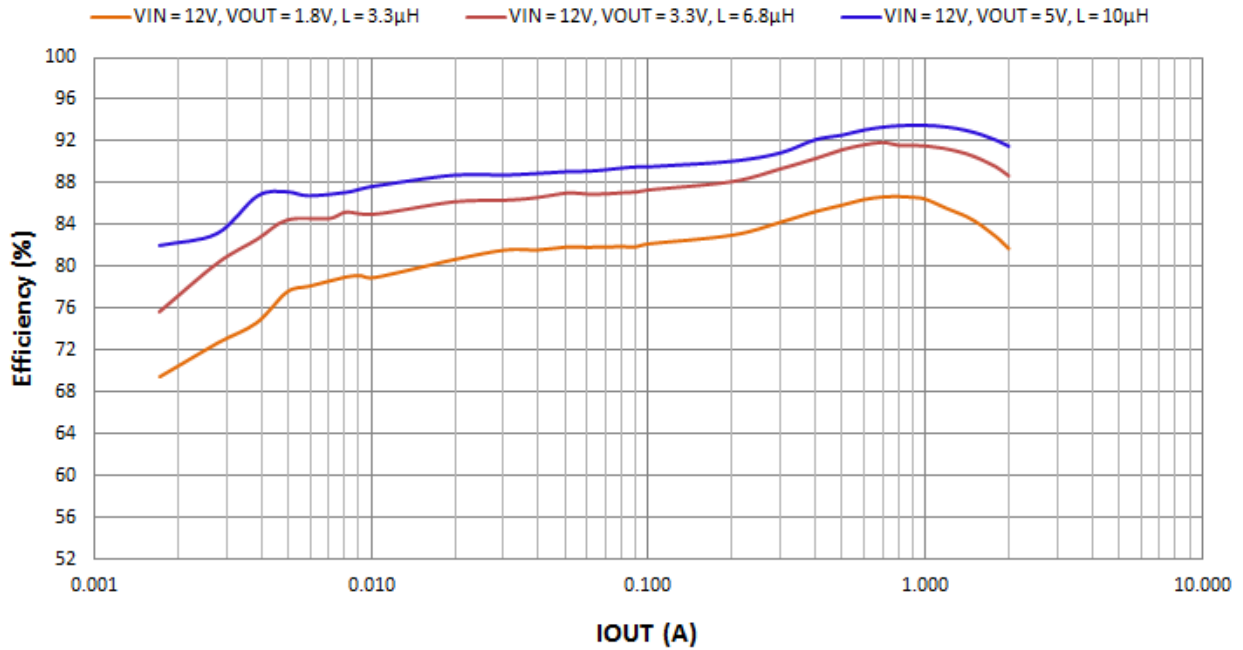


Figure 7. Efficiency for VIN=24V, VOUT=12V

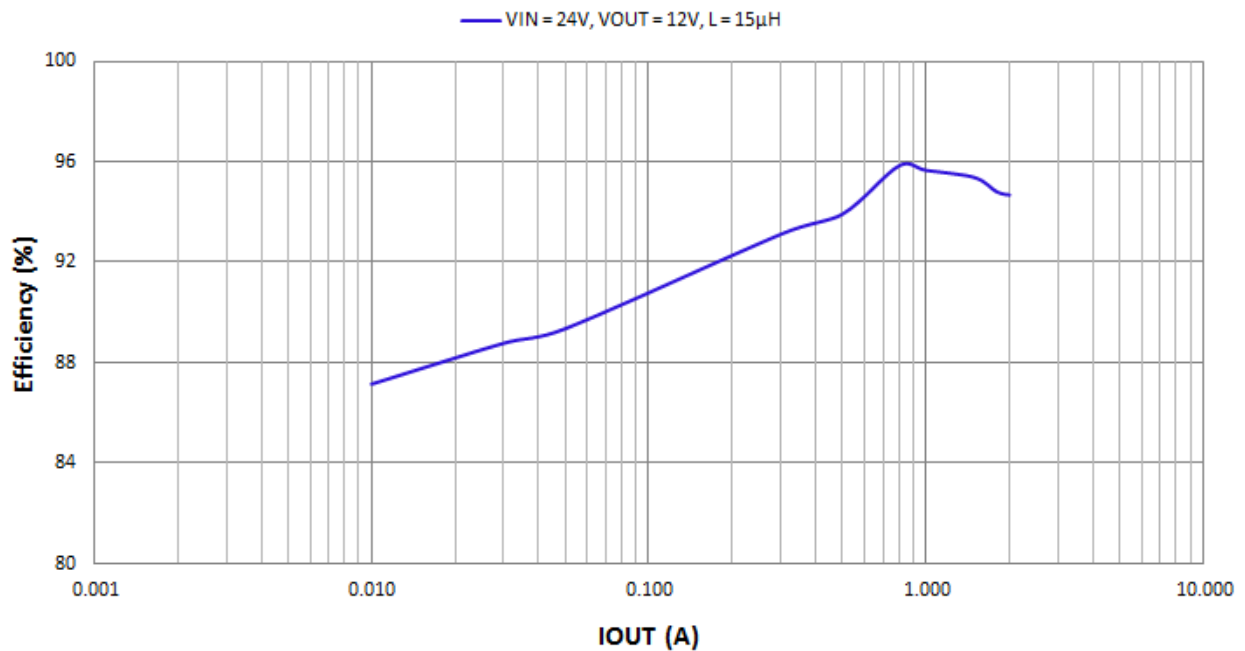


Figure 8. Output Ripple for  $V_{IN}=12V$ ,  $V_{OUT}=5.0V$ ,  $I_{OUT}=2A$

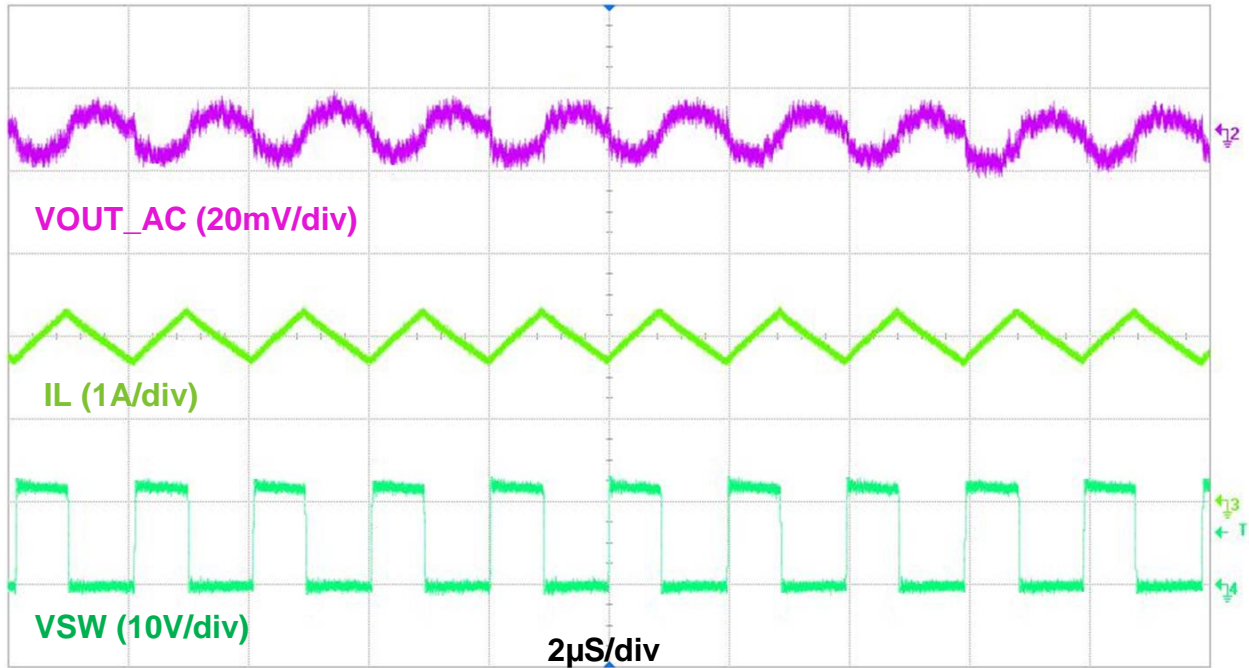
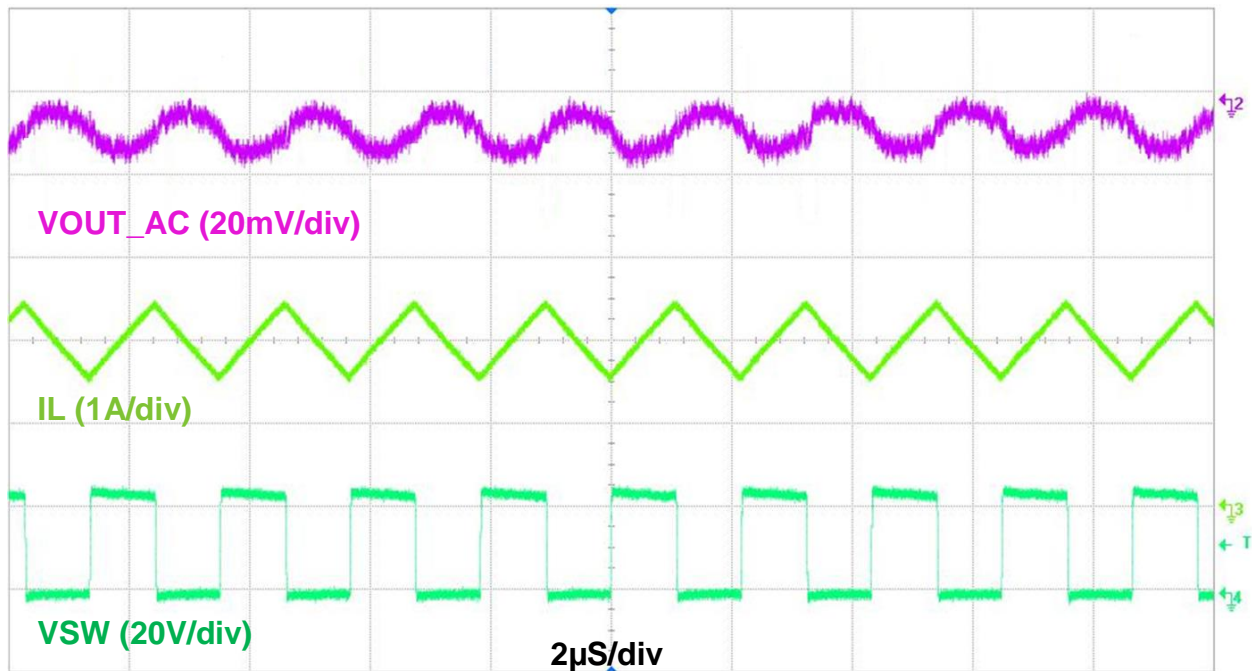


Figure 9. Output Ripple for  $V_{IN}=24V$ ,  $V_{OUT}=12V$ ,  $I_{OUT}=2A$



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