

Process Introduction

4um / 25V Bipolar Process Technology

Process features

- Single isolation
- Deep N+ collector plug
- NPN transistor
- Lateral PNP transistor
- Vertical (substrate) PNP transistor
- Zener diode
- Implant Resistor (optional)
- MOS Capacitor (optional)
- Double metal (optional)
- Low cost
- Applications: analog, power linear

Key Design Rules

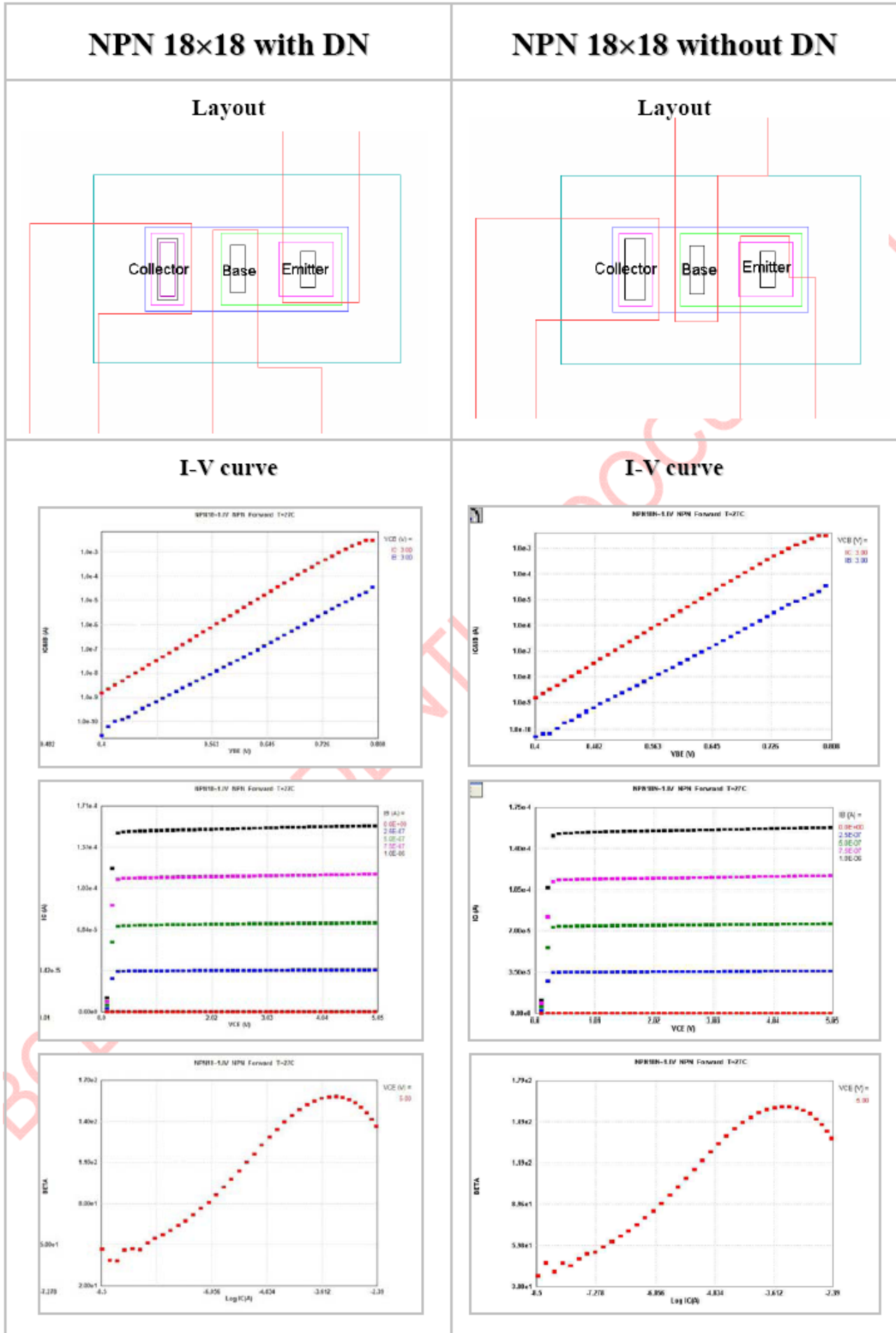
7 Masks	Min. Width/Space(um)
Diffusion(Iso)	6
Diffusion(others)	5
Contact	4
Metal	6/6

Electrical Specification

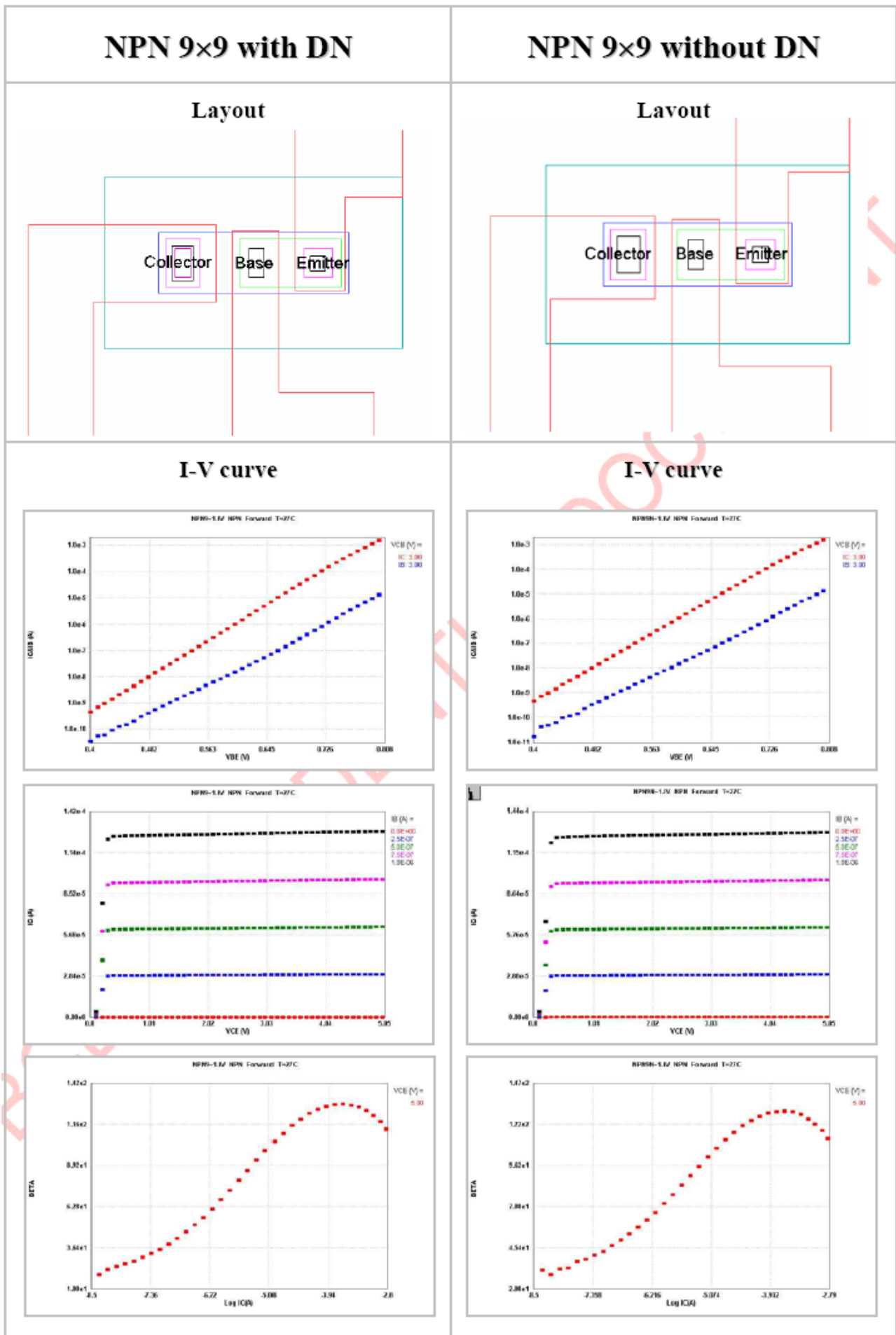
Device	Parameter	Specification			
		Min	Typ	Max	Unit
NPN transistor (18x18 um ² emitter)	Hfe (Ic=1mA)	80	160	300	-
	BVceo(Ic=10uA)	26	-	-	V
	BVebo(Ic=10uA)	7.0	7.6	8.5	V
Lateral PNP Transistor (Wb=12um)	Hfe (Ic=100uA)	30	100	160	-
	BVceo(Ic=10uA)	26	-	-	V
Vertical (substrate) PNP	Hfe (Ic=100uA)	100	250	450	-
	BVceo(Ic=10uA)	30	-	-	V
Sheet Resistance	PBASE-R	200	225	250	Ω/□
	Implant-R	1.80	2.05	2.3	kΩ/□
Capacitance (SiO2)	C(100x100um ²)	3	4	5	pF

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Device characteristic curve



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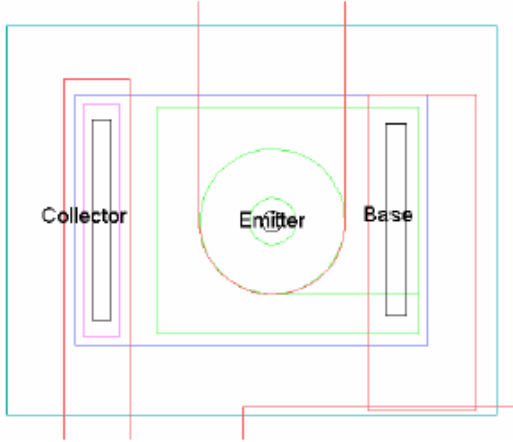


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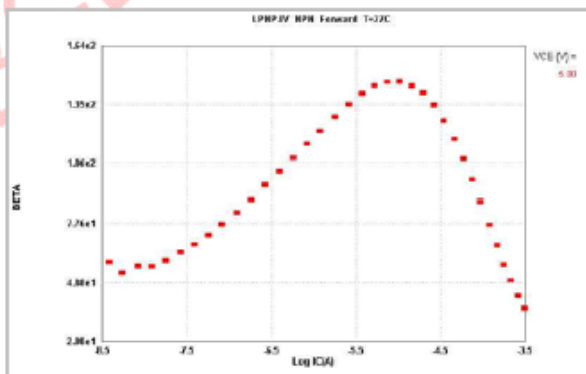
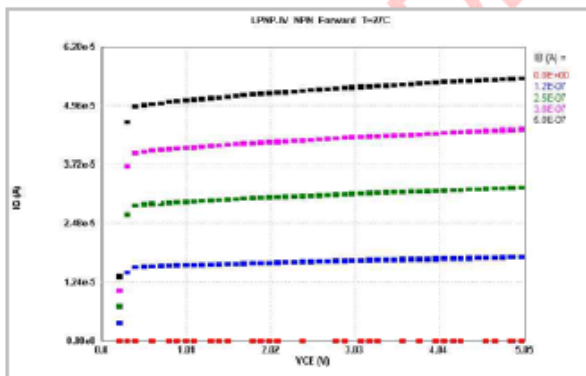
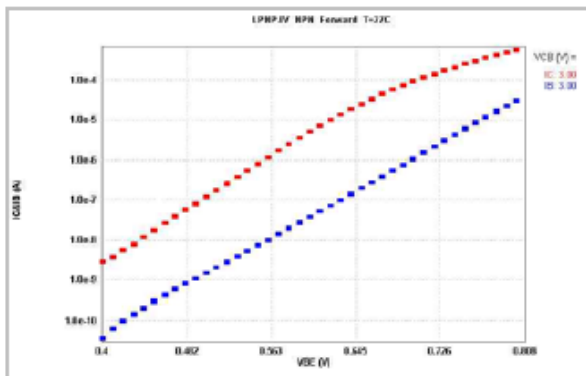
PBAS LPNP

$\phi=11.0\text{ }\mu\text{m}$, $W_b=12.0\text{ }\mu\text{m}$

Layout



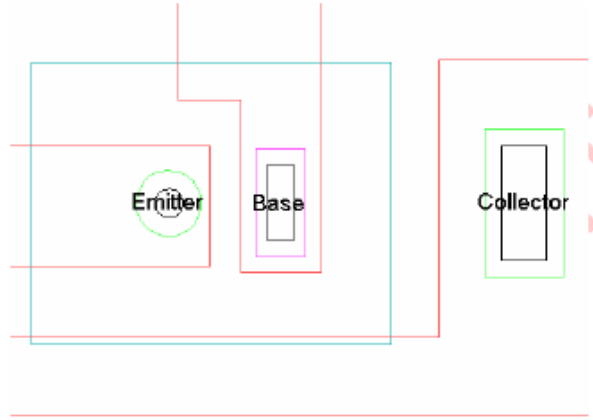
I-V curve



Substrate VPNP

$\phi=11.0\text{ }\mu\text{m}$

Layout



I-V curve

