PART OBSOLETE - USE PI3WVR648



A Product Line of Diodes Incorporated

PI3WVR2646

2:1 MIPI 4-Data Lane Switch

Features

- SPDT (10x) Switch Type and Signal Type Support D-PHY and C-PHY
- Data Rate: D-PHY (2.5Gbps) 4-Data Lane and C-PHY (2.5Gsps) 3-Data Lane
- Supports 2:1 clock differential signal
- -3 dB Bandwidth: 4.1 GHz Typical
- Low Crosstalk: -30 dB@1.25 GHz
- Input Signals 0 to 1.3V
- RON: 6Ω Typical LP & HS MIPI
- ΔR_{ON} : 0.1 Ω Typical LP & HS MIPI
- R_{ON_FLAT} : 0.3 Ω Typical LP & HS MIPI
- I_{CCZ}: 0.5uA Typical
- I_{CC}: 32µA Max
- C_{ON}: 1.5pF Typical
- Skew of Opposite Transitions of the Same Output: 6ps Typical
- V_{DD} Operating Range: 1.5V to 3.6V
- ESD Tolerance: 2kV HBM
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please <u>contact us</u> or your local Diodes representative. <u>https://www.diodes.com/quality/product-definitions/</u>
- Packaging (Pb-free & Green):
 - ^o 36-Ball, WLCSP (GH) 2.10x2.10

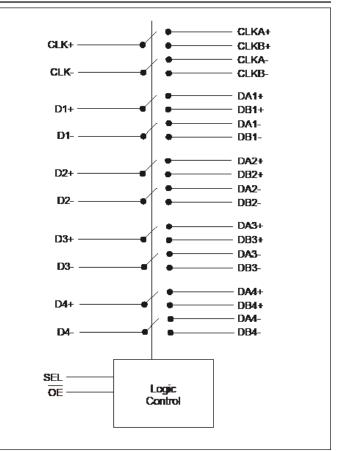
Application(s)

- Cellular Phones, Smart Phones
- Tablets
- Laptops
- Displays

Description

The DIODES PI3WVR2646 is a four-data-lane MIPI-D-PHY switch. This 10 channel single-pole, double-throw (SPDT) switch is optimized for switching between two high-speed (HS) or low-power (LP) MIPI signal. The PI3WVR2646 is designed for the MIPI specification and allows connection to a CSI or DSI module.

Block Diagram



Notes:

See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm

antimony compounds.

^{1.} No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.

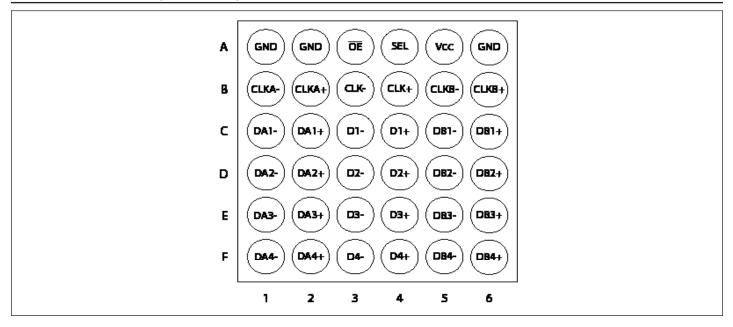




Truth Table

| SEL | ŌĒ | Function |
|------|------|--|
| LOW | LOW | CLK+ = CLKA+, CLK- = CLKA-, Dn(+/-) = DAn(+/-) |
| HIGH | LOW | CLK+ = CLKB+, CLK- = CLKB-, Dn(+/-) = DBn(+/-) |
| Х | HIGH | Clock and Data Ports High Impedance |

Pin Configuration(Top View)



Pin Description

| Pin# | Pin Name | Туре | Description |
|------|----------|--------|---|
| A1 | GND | Ground | Ground |
| A2 | GND | Ground | Ground |
| A3 | ŌĒ | Ι | Output enable. if \overline{OE} is low, IC is enabled. if \overline{OE} is high, IC is power down and all I/Os are Hi-Z |
| A4 | SEL | Ι | Switch logic control |
| A5 | VCC | Power | 1.5V to 3.6V power supply |
| A6 | GND | Ground | Ground |
| B1 | CLKA- | I/O | Clock negative differential signal for port A |
| B2 | CLKA+ | I/O | Clock positive differential signal for port A |
| B3 | CLK- | I/O | Clock negative differential signal for COM port |
| B4 | CLK+ | I/O | Clock positive differential signal for COM port |
| B5 | CLKB- | I/O | Clock negative differential signal for port B |
| B6 | CLKB+ | I/O | Clock positive differential signal for port B |
| C1 | DA1- | I/O | Negative differential signal 1 for port A |
| C2 | DA1+ | I/O | Positive differential signal 1 for port A |





| Pin# | Pin Name | Туре | Description |
|------|----------|------|---|
| C3 | D1- | I/O | Negative differential signal 1 for COM port |
| C4 | D1+ | I/O | Positive differential signal 1 for COM port |
| C5 | DB1- | I/O | Negative differential signal 1 for port B |
| C6 | DB1+ | I/O | Positive differential signal 1 for port B |
| D1 | DA2- | I/O | Negative differential signal 2 for port A |
| D2 | DA2+ | I/O | Positive differential signal 2 for port A |
| D3 | D2- | I/O | Negative differential signal 2 for COM port |
| D4 | D2+ | I/O | Positive differential signal 2 for COM port |
| D5 | DB2- | I/O | Negative differential signal 2 for port B |
| D6 | DB2+ | I/O | Positive differential signal 2 for port B |
| E1 | DA3- | I/O | Negative differential signal 3 for port A |
| E2 | DA3+ | I/O | Positive differential signal 3 for port A |
| E3 | D3- | I/O | Negative differential signal 3 for COM port |
| E4 | D3+ | I/O | Positive differential signal 3 for COM port |
| E5 | DB3- | I/O | Negative differential signal 3 for port B |
| E6 | DB3+ | I/O | Positive differential signal 3 for port B |
| F1 | DA4- | I/O | Negative differential signal 4 for port A |
| F2 | DA4+ | I/O | Positive differential signal 4 for port A |
| F3 | D4- | I/O | Negative differential signal 4 for COM port |
| F4 | D4+ | I/O | Positive differential signal 4 for COM port |
| F5 | DB4- | I/O | Negative differential signal 4 for port B |
| F6 | DB4+ | I/O | Positive differential signal 4 for port B |





Absolute Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

| <u> </u> | - |
|--|--------------------------|
| V _{CC} , Supply Voltage | 0.5V to 4.5V |
| V_{CNTRL} , DC Input Voltage (\overline{OE} , SEL) ⁽¹⁾ | -0.5V to V _{CC} |
| V _{SW} , DC Switch I/O Voltage ^(1,2) | 0.3V to 2.5V |
| I _{IK} , DC Input Diodes Current | |
| I _{OUT} , DC Output Current | 25mA |
| T _{STG} , Storage Temperature | 65°C to +150°C |
| Tj, Junction Temperature | 125°C |
| ESD: | |
| Human Body Model, JEDEC: JESD22-A114, All Pir | ns 2.0kV |
| Charged Device Model, JEDEC: JESD22-C101 | 1.0kV |
| 1 | |

Note:

Stresses greater than those listed under MAXIMUM RAT-INGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Note:

1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

2. V_{SW} refers to analog data switch paths.

Recommended Operating Conditions

The Recommended operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications.

| Symbol | Description | Test Conditions | Min. | Max. | Units |
|--------------------|--|------------------------|------|-----------------|-------|
| V _{CC} | Supply Voltage | | 1.5 | 3.6 | V |
| V _{CNTRL} | Control Input Voltage (SEL, \overline{OE}) ⁽¹⁾ | | 0 | V _{CC} | V |
| V. | witch 1/0 Waltons (CLV, D. CLVA, CLVB, DA, DB) | - HS Mode | 0 | 0.5 | V |
| V _{SW} | Switch I/O Voltage (CLK-, D-, CLKA-, CLKB-, DA-, DB-) | - LP Mode | 0 | 1.3 | V |
| T _A | Operating Temperature | | -40 | +85 | °C |

Note:

1. The control inputs must be held HIGH or LOW; they must not float.

DC and Transient Characteristics

All typical values are at $T_A = 25^{\circ}C$ unless otherwise specified.

| Symbol | Description | Test Conditions | | $T_{\rm A} = -40^{\circ} {\rm C}$ to $+85^{\circ} {\rm C}$ | | | Units |
|--|--|----------------------------------|-------------|--|------|------|-------|
| Symbol | Description | Test Conditions | $V_{CC}(V)$ | Min. | Тур. | Max. | Units |
| V _{IK} | Clamp Diode Voltage (OE, SEL) | $I_{IN} = -18mA$ | 1.5 | -1.2 | | -0.6 | V |
| V _{IH} | Input Voltage High | SEL, \overline{OE} | 1.5 to 3.3 | 1.0 | | | V |
| V _{IL} | Input Voltage Low | SEL, \overline{OE} | 1.5 to 3.3 | | | 0.5 | V |
| I _{IN} | Control Input Leakage (\overline{OE} , SEL) | $V_{CNTRL} = 0$ to V_{CC} | 3.3 | -0.5 | | 0.5 | μΑ |
| I _{NO(OFF)} I _{NC(OFF)} | Off Leakage Current of Port | $V_{SW} = 0.0 \le DATA \le 1.3V$ | 3.3 | -0.5 | | 0.5 | μΑ |
| I _{A(ON)} | On Leakage Current of Common Ports | $V_{SW} = 0.0 \le DATA \le 1.3V$ | 3.3 | -0.5 | | 0.5 | μΑ |





DC and Transient Characteristics Cont.

| 6 1 1 | Description | Test Carditions | | $T_{\rm A} = -40^{\circ} {\rm C} \text{ to } +85^{\circ} {\rm C}$ | | | TT •4 |
|-------------------------|---|--|-------------|---|------|------|-------|
| Symbol | Description | Test Conditions | $V_{CC}(V)$ | Min. | Тур. | Max. | Units |
| I _{OFF} | Power-Off Leakage Current (All I/O Ports) | V _{SW} = 0.0 or 1.3V | 0 | -0.5 | | 0.5 | μΑ |
| I _{OZ} | Off-State Leakage | $\frac{V_{SW} = 0.0 \le DATA \le 1.3V,}{OE} = High$ | 3.6 | -0.5 | | 0.5 | μΑ |
| | | $I_{ON} = -8mA$, $\overline{OE} = 0V$, | 1.5 | | | | |
| R _{ON_MIPI_HS} | Switch On Resistance for HS MIPI | SEL = V_{CC} or 0V, All I/O | 2.5 | | 6 | | Ω |
| | | Switches = 0.2V | 3.3 | | | | |
| | | $I_{ON} = -8mA$, $\overline{OE} = 0V$, | 1.5 | | | | |
| R _{ON_MIPI_LP} | Switch On Resistance for LP MIPI | SEL = V_{CC} or 0V, All I/O | 2.5 | | 6 | | Ω |
| | | Switches = 1.2V | 3.3 | | | | |
| | On Resistance Matching Between | $I_{ON} = -8mA$, $\overline{OE} = 0V$, | 1.5 | | | | |
| $\Delta R_{ON_MIPI_HS}$ | HS MIPI Channels ⁽¹⁾ | SEL = V_{CC} or 0V, All I/O Switches = 0.2V | 2.5 | | 0.1 | | Ω |
| | | Switches = 0.2 v | 3.3 | | | | |
| | On Resistance Matching Between | $I_{ON} = -8mA$, $\overline{OE} = 0V$, | 1.5 | | | | |
| $\Delta R_{ON_MIPI_LP}$ | LP MIPI Channels ⁽¹⁾ | SEL = V _{CC} or 0V, All I/O Switches = 1.2V | 2.5 | | 0.1 | | Ω |
| | | | 3.3 | | | | |
| R _{ON_FLAT_} | | $I_{ON} = -8mA, \overline{OE} = 0V,$ | 1.5 | | | | 0 |
| MIPI_HS | On Resistance Flatness for HS MIPI | SEL = V_{CC} or 0V, All I/O Switches = 0 to 0.5V | 2.5 | | 0.3 | | Ω |
| | | | 3.3 | | | | |
| R _{ON_FLAT_} | On Resistance Flatness for LP MIPI | $I_{ON} = -8mA$, $\overline{OE} = 0V$, SEL = V _{CC} or 0V, All I/O | 1.5 | | 0.3 | | Ω |
| MIPI_LP | | SEL = v_{CC} of $0v$, All $1/O$ Switches = 0 to 1.3V | 2.5 | | 0.5 | | 77 |
| I _{CC} | Quiescent Supply Current | $\frac{V_{SEL} = 0 \text{ or } V_{CC}, I_{OUT} = 0,}{OE = 0V}$ | 3.6 | | 15 | 32 | μΑ |
| I _{CCZ} | Quiescent Supply Current (High Impedance) | $\frac{V_{SEL} = 0 \text{ or } V_{CC}, I_{OUT} = 0,}{OE} = High$ | 3.6 | | 0.5 | 1.0 | μΑ |
| I _{CCT} | Increase in $I_{\rm CC}$ Current Per Control Voltage and $V_{\rm CC}$ | $V_{SEL} = 0 \text{ or } V_{CC}, \overline{OE} = 1.5V$ | 3.6 | | 1 | | μΑ |





AC Electrical Characteristics

All typical values are for $V_{CC} = 3.3V$ and $T_A = 25^{\circ}C$ unless otherwise specified.

| 6 1 1 | Description | Test Conditions | | $T_{\rm A} = -40^{\circ} {\rm C}$ to $+85^{\circ} {\rm C}$ | | | TT •4 |
|-------------------|--|---|-------------|--|------|------|-------|
| Symbol | Description | Test Conditions | $V_{CC}(V)$ | Min. | Тур. | Max. | Units |
| t _{INIT} | Initialization Time V_{CC} to $Output^{(1)}$ | $R_{L} = 50\Omega, C_{L} = 0pF, V_{SW}$ $= 0.6V$ | 1.5 to 3.6 | | 60 | | μs |
| t _{EN} | Enable Time \overline{OE} to Output | $\begin{aligned} R_L &= 50\Omega, \ C_L = 0 p F, \ V_{SW} \\ &= 0.6 V \end{aligned}$ | 1.5 to 3.6 | | 60 | 150 | μs |
| t _{DIS} | Disable Time \overline{OE} to Output | $\begin{aligned} R_L &= 50\Omega, \ C_L = 0 p F, \ V_{SW} \\ &= 0.6V \end{aligned}$ | 1.5 to 3.6 | | 35 | 250 | ns |
| t _{ON} | Turn-On Time SEL to Output | $\begin{aligned} R_L &= 50\Omega, \ C_L = 0 p F, \ V_{SW} \\ &= 0.6V \end{aligned}$ | 1.5 to 3.6 | | 350 | 1500 | ns |
| t _{OFF} | Turn-Off Time SEL to Output | $\begin{aligned} R_L &= 50\Omega, \ C_L = 0 p F, \ V_{SW} \\ &= 0.6 V \end{aligned}$ | 1.5 to 3.6 | | 125 | 800 | ns |
| t _{BBM} | Break-Before-Make Time | $\begin{split} R_L &= 50\Omega, \ C_L = 0 p F, \ V_{SW} \\ &= 0.6 V \end{split}$ | 1.5 to 3.6 | | | 1000 | ns |
| t _{PD} | Propagation Delay ⁽¹⁾ | $C_L = 0 p F, R_L = 50 \Omega$ | 1.5 to 3.6 | | | 0.25 | ns |
| O _{IRR} | Differential Off Isolation for MIPI ⁽¹⁾ | $\frac{R_L}{OE} = 50\Omega, \ f = 1250MHz, \\ \overline{OE} = HIGH, \ V_{SW} = 0.5V$ | 1.5 to 3.6 | | -26 | | dB |
| X _{TALK} | Differential Crosstalk for MIPI ⁽¹⁾ | $\label{eq:RL} \begin{split} R_L &= 50\Omega, \ f = 1250 MHz, \\ SEL &= HIGH, \ V_{SW} = 0.5 V \end{split}$ | 1.5 to 3.6 | | | -30 | dB |
| I _{LOSS} | Differential Insertion Loss ⁽¹⁾ | $\begin{split} R_L &= 50\Omega, \ C_L = 0 p F, \\ f &= 1250 M Hz, \ V_{SW} = 0.5 V \end{split}$ | 1.5 to 3.6 | | -0.8 | | |
| BW | Differential -3db Bandwidth ⁽¹⁾ | $\begin{split} R_L &= 50\Omega, \ C_L = 0 p F, \ V_{SW} \\ &= 0.5 V \end{split}$ | 1.5 to 3.6 | 3 | 4.1 | | GHz |

Note:

1. Guaranteed by characterization.





High-Speed-Related AC Electrical Characteristics

| Symbol | Description | Test Conditions | V _{CC} (V) | $T_{\rm A} = -40^{\rm o}{\rm C}$ to $+85^{\rm o}{\rm C}$ | | | Unita |
|--------------------|--|--|------------------------|--|------|------|-------|
| Symbol | Description | | | Min. | Тур. | Max. | Units |
| | D-PHY HS Mode Skew of Opposite Transitions of the Same Output ⁽¹⁾ | $\begin{array}{c} R_L = 50\Omega, \ C_L = 0 p F, \ V_{SW} = \\ 0.3V \end{array}$ | 1.5 to 3.6 | | 4 | | |
| t _{SK(P)} | C-PHY HS Mode Skew of 3 channels in same lane | $\begin{array}{c} R_L=50\Omega,\ C_L=0pF,\ V_{SW}=\\ 0.5V \end{array}$ | 1.5 to 3.6 | | 4 | | ps |
| | D-PHY HS Mode Skew of all group A or group B channels ⁽¹⁾ | $\begin{array}{c} R_L=50\Omega,\ C_L=0pF,\ V_{SW}=\\ 0.3V \end{array}$ | 1.5 to 3.6 | | 8 | | |

Note:

1. Guaranteed by characterization.

Capacitance

| Symbol | Description | Test Conditions | $T_{\rm A} = -40^{\circ}{\rm C}$ to $+85^{\circ}{\rm C}$ | | | |
|------------------|--|--|--|------|------|-------|
| Symbol | Description | Test Conditions | Min. | Тур. | Max. | Units |
| C _{IN} | Control Pin Input Capacitance ⁽¹⁾ | $V_{CC} = 0V, f = 1MHz$ | | 2.1 | | pF |
| C _{ON} | On Capacitance ⁽¹⁾ | $V_{CC} = 3.3V, \overline{OE} = 0V, f = 1250MHz$ (In HS common value) | | 1.5 | | pF |
| C _{OFF} | Off Capacitance ⁽¹⁾ | V_{CC} or $\overline{OE} = 3.3V$, f = 1250MHz (Both sides in HS common value) | | 0.9 | | pF |

Note:

1. Guaranteed by characterization.

Part Markina

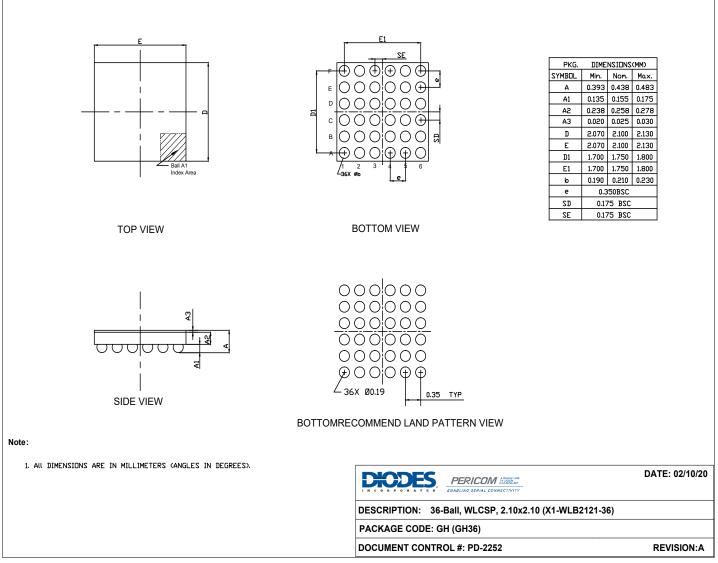
| PI3WVR 2646GHE ZYYWWXX | |
|---|--|
| Z: Die Rev YY: Date Code (Year) WW: Date Code (Workweek) 1st X: Assembly Site Code 2nd X: Fab Site Code | |





Packaging Mechanical

36-WLCSP (GH)



20-1127

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

For latest package info.

| Ordering Code | Package Code | Package Description |
|----------------|--------------|---|
| PI3WVR2646GHEX | GH | 36-Ball, 2.10x2.10, (WLCSP) X1-WLB2121-36 |

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.

2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free. 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm

antimony compounds.

4. E = Pb-free and Green

5. X suffix = Tape/Reel





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