

ESD PROTECTION DEVICE

STAND-OFF VOLTAGE - 3.3 V
POWER DISSIPATION - 40 W

GENERAL DESCRIPTION

The L04U3V3NA-4 is ultra-low capacitance TVS arrays designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from overvoltage caused by ESD (electrostatic discharge), CDE (Cable Discharge Events), and EFT (electrical fast transients).

FEATURES

- Protects for I/O lines.
- Max. peak pulse power : Ppp = 40W at tp = 8/20 us.
- Ultra-low capacitance: 0.45pF typical (I/O to Gnd)..
- IEC 61000-4-2 (ESD), > ±30KV (air) ; > ±16KV (contact)
- Qualified to ACE-Q101 Rev_C

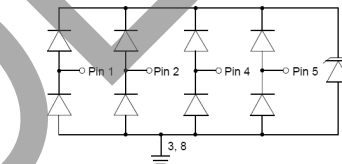
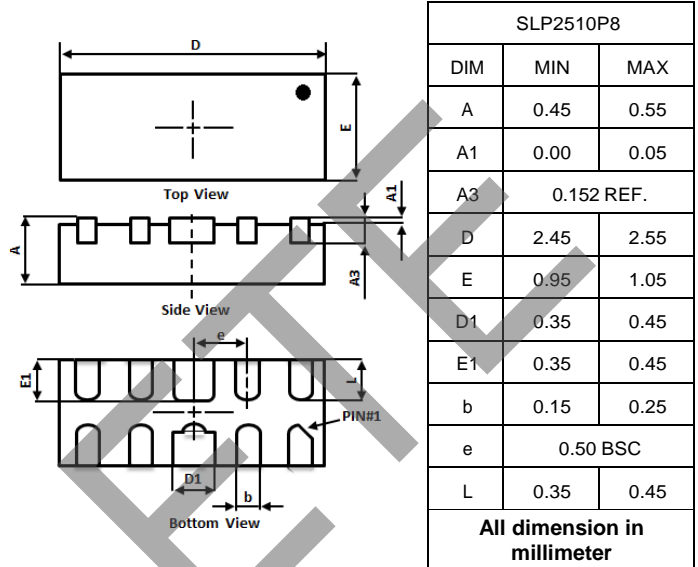
APPLICATION

- High definition multi-media interface(HDMI) 1.3& 1.4 and 2.0 version.
- Digital visual interface (DVI).
- Display Port interface.
- SATA and ESATA interface.
- USB 3.0
- Ethernet port: 10/100/1000 Mb/s
- Desktop and Notebooks PCs.

MECHANICAL DATA

- Case material: “Green” molding compound UL flammability classification 94V-0 (No Br, Sb, Cl)
- Terminals: Lead Free Plating
- Component in accordance to RoHs 2011/65/EU

SLP2510P8



PIN ASSIGNMENT	
1,2,4,5	Input lines
6,7,9,10	NC
3,8	Ground

MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Ratings at 25°C ambient temperature unless otherwise specified.

PARAMETER	SYMBOL	VALUE	UNIT
Peak pulse power (tp = 8/20 us)	P _{PK}	40	W
Peak pulse current (tp = 8/20 us)	I _{PP}	4	A
Operating junction temperature range	T _J	-55 to +125	°C
Storage temperature range	T _{STG}	-55 to +150	°C
Soldering temperature, t max=10s	T _L	260	°C

ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Reverse stand-off voltage	V _{RWM}	Any pin to ground	--	----	3.3	V
Forward voltage	V _F	I _F = 15 mA	--	--	1.1	V
Reverse leakage current	I _{RM}	V _{DRM} = 3.3 V, Any I/O pin to ground	--	--	1.0	uA
Breakdown voltage	V _{BR}	I _R = 1 mA	4.0	--	--	V
Clamping voltage	V _C	I _{PP} = 1A, tp = 8/20 uS,	--	--	6.5	V
		I _{PP} = 4A, tp = 8/20 uS,	--	--	10	
Junction Capacitance	C _J	V _R = 1.65V, f =1MHz, Any I/O pin to ground	--	0.45	0.65	pF

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FIG.1- 8/20us pulse waveform according to IEC 61000-4-5

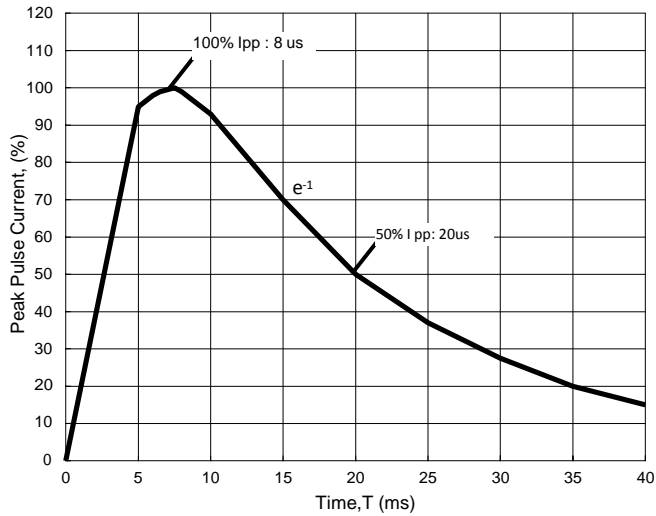


FIG.2- ESD pulse waveform according to IEC 61000-4-2

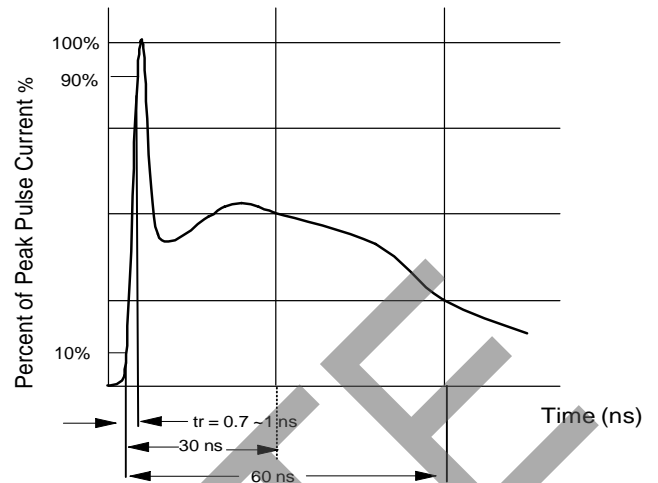


FIG.3- power dissipation versus pulse time

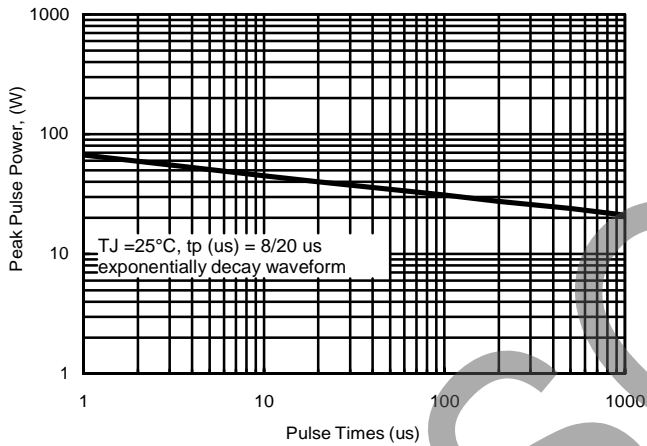


FIG.4- peak pulse power versus T_J

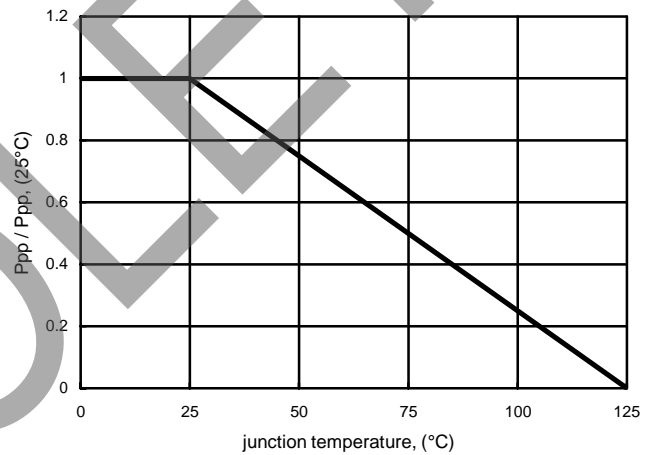


FIG.5- typical junction capacitance

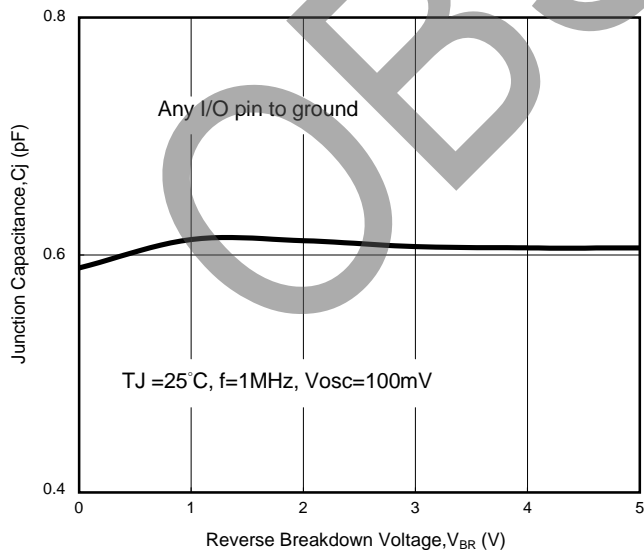
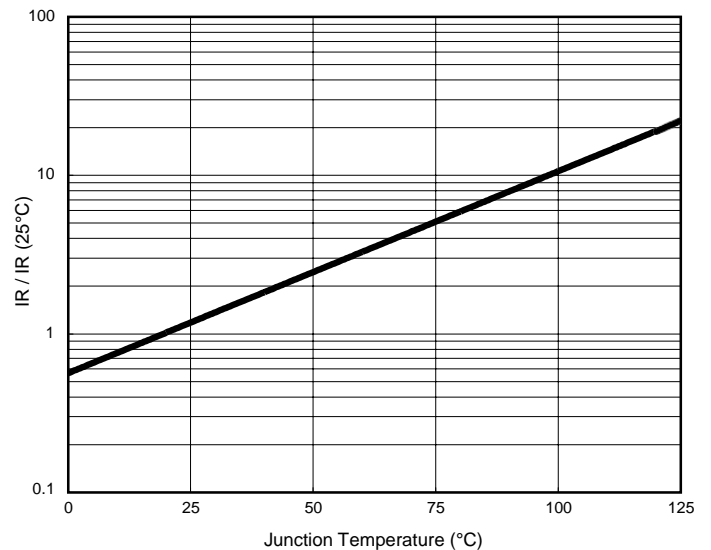


FIG.6- reverse leakage current versus T_J



RATING AND CHARACTERISTIC CURVES L04U3V3NA-4

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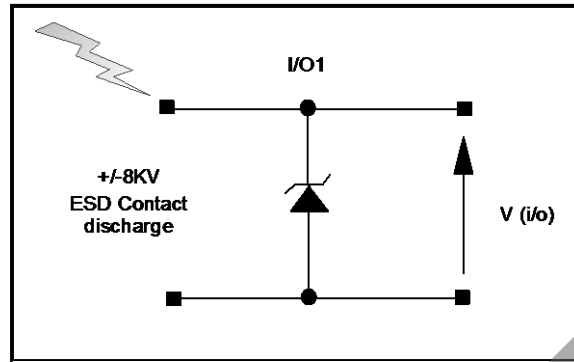


FIG.7- ESD Test Configuration

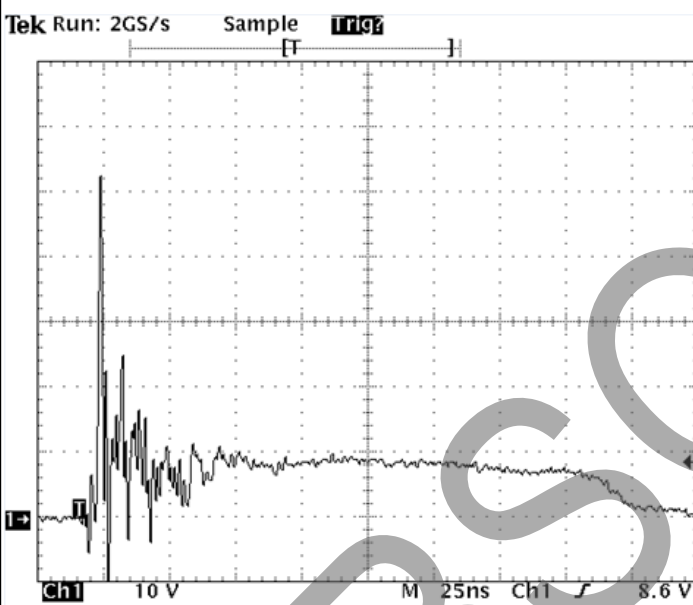


FIG.8- Clamped +8 kV ESD voltage waveform

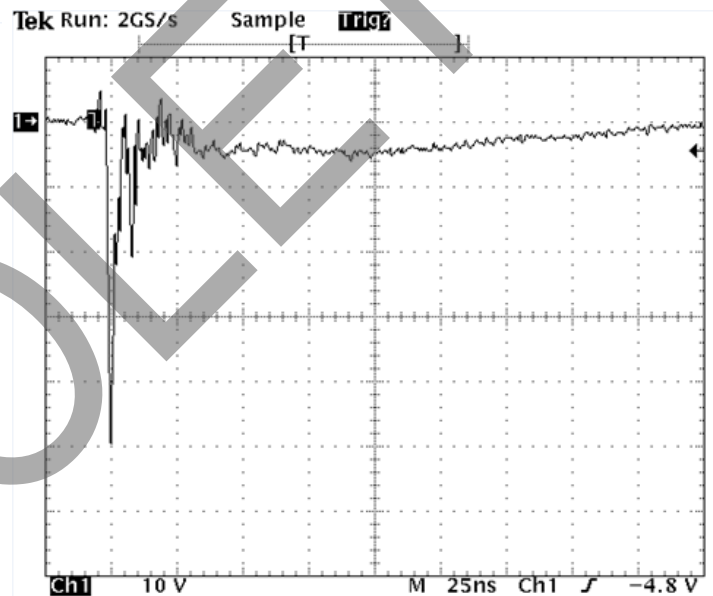


FIG.9- Clamped -8 kV ESD voltage waveform

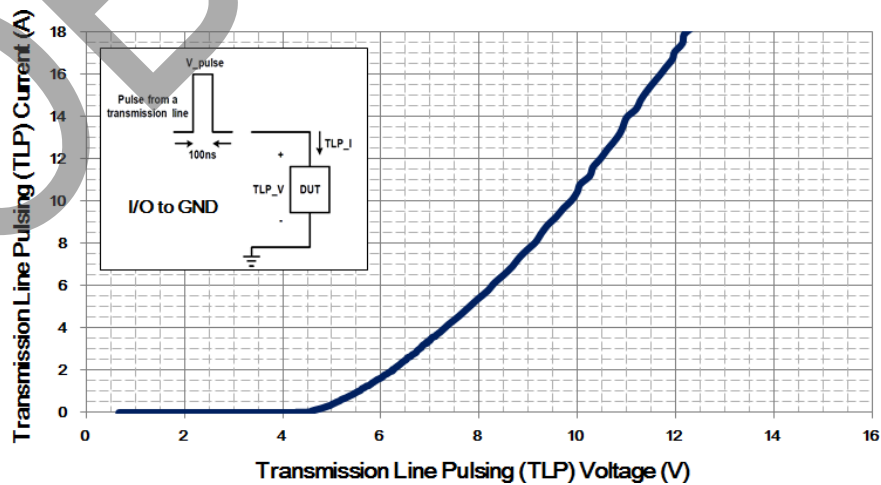
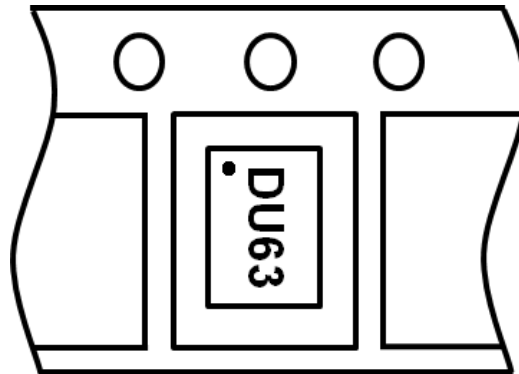


FIG.10- Transmission Line Pulsing (TLP) Measurement

RATING AND CHARACTERISTIC CURVES L04U3V3NA-4

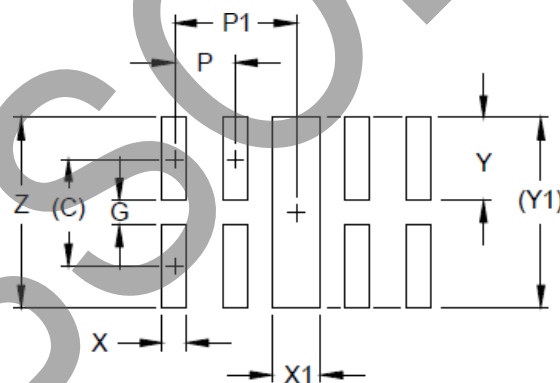
Marking & Orientation



Packaging Information

DEVICE	Q'TY/REEL (PCS)	REEL DIA. (INCH)	Q'TY/BOX (PCS)	Q'TY/CARTON (PCS)
L04U3V3NA-4	3000	7	45000	90K/180K

SLP2510P8 Soldering Pad Layout



Dim.	Millimeters	Inches
C	(0.0875)	(0.034)
G	0.20	0.008
P	0.50	0.020
P1	1.00	0.039
X	0.20	0.008
X1	0.40	0.016
Y	0.68	0.027
Y1	(1.550)	(0.061)
Z	1.55	0.061

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