

## Product Summary

V <sub>DSS</sub>	R <sub>DS(on)</sub>	Q <sub>g</sub>	Q <sub>gd</sub>	I <sub>D</sub>
-12V	12mΩ	4.9nC	1.1nC	-7.6A

Typ. @ V<sub>GS</sub> = -4.5V, T<sub>A</sub> = +25°C

## Description

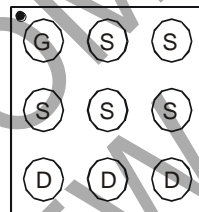
This 1<sup>st</sup> generation Lateral MOSFET (LD-MOS) is engineered to minimize on-state losses and switch ultra-fast, making it ideal for high efficiency power transfer. Using Chip-Scale Package (CSP) to increase power density by combining low thermal impedance with minimal R<sub>DS(on)</sub> per footprint area.

## Applications

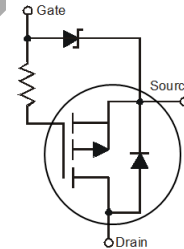
- DC-DC converters
- Battery managements
- Load switches



ESD PROTECTED TO 3kV



Top-View  
Pin Configuration



Equivalent Circuit

## Features

- LD-MOS technology with the lowest Figure of Merit:  
R<sub>DS(on)</sub> = 12mΩ to Minimize On-State Losses  
Q<sub>g</sub> = 4.9nC for Ultra-Fast Switching
- V<sub>gs(th)</sub> = -0.8V typ. for a Low Turn-On Potential
- CSP with Footprint 1.5mm × 1.5mm
- Height = 0.62mm for Low Profile
- ESD = 3kV HBM Protection of Gate
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e.: parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please refer to the related automotive grade (Q-suffix) part. A listing can be found at <https://www.diodes.com/products/automotive/automotive-products/>.**
- **This part is qualified to JEDEC standards (as references in AEC-Q) for High Reliability.**  
<https://www.diodes.com/quality/product-definitions/>

## Mechanical Data

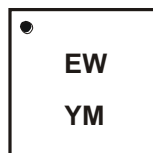
- Package: U-WLB1515-9
- Terminal Connections: See Diagram Below

## Ordering Information (Note 4)

Part Number	Package	Packing	
		Qty.	Carrier
DMP1018UCB9-7	U-WLB1515-9	3,000	Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
  2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

## Marking Information



EW = Product Type Marking Code  
YM = Date Code Marking  
Y or Y = Year (ex: J = 2022)  
M or M = Month (ex: 1 = January)

### Date Code Key

Year	2012	...	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
Code	Z	...	J	K	L	M	N	O	P	R	S	T

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V <sub>DSS</sub>	-12	V
Gate-Source Voltage			V <sub>GSS</sub>	-6	V
Continuous Drain Current (Note 5) V <sub>GS</sub> = -4.5V	Steady State	T <sub>A</sub> = +25°C	I <sub>D</sub>	-7.6	A
		T <sub>A</sub> = +70°C		-6.0	
Continuous Drain Current (Note 6) V <sub>GS</sub> = -4.5V	Steady State	T <sub>A</sub> = +25°C	I <sub>D</sub>	-5.5	A
		T <sub>A</sub> = +70°C		-4.3	
Pulsed Drain Current (Pulse duration 10μs, duty cycle ≤1%)			I <sub>DM</sub>	-60	A

**Thermal Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P <sub>D</sub>	1.0	W
Total Power Dissipation (Note 6)	P <sub>D</sub>	1.8	W
Thermal Resistance, Junction to Ambient (Note 5)	R <sub>θJA</sub>	126.8	°C/W
Thermal Resistance, Junction to Ambient (Note 6)	R <sub>θJA</sub>	69	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-12	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA
Zero Gate Voltage Drain Current @T <sub>C</sub> = +25°C	I <sub>DSS</sub>	—	—	-1	μA	V <sub>DS</sub> = -9.6V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	-100	nA	V <sub>GS</sub> = -6.0V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	-0.4	-0.8	-1.3	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	—	12	18	mΩ	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -2A
			15	22		V <sub>GS</sub> = -2.5V, I <sub>D</sub> = -2A
Forward Transfer Admittance	Y <sub>fs</sub>	—	5.5	—	S	V <sub>DS</sub> = -6V, I <sub>D</sub> = -2A
Diode Forward Voltage (Note 6)	V <sub>SD</sub>	—	-0.7	-1	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = -2A
Reverse Recovery Charge	Q <sub>rr</sub>	—	30.2	—	nC	V <sub>dd</sub> = -5V, I <sub>F</sub> = -2A,
Reverse Recovery Time	t <sub>rr</sub>	—	71.4	—	ns	di/dt = 200A/μs
<b>DYNAMIC CHARACTERISTICS (Note 8)</b>						
Input Capacitance	C <sub>iss</sub>	—	457	—	pF	V <sub>DS</sub> = -6V, V <sub>GS</sub> = 0V, f = 1.0MHz
Output Capacitance	C <sub>oss</sub>	—	272	—	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>	—	120	—	pF	
Series Gate Resistance	R <sub>G</sub>	—	21.23	—	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1.0MHz
Total Gate Charge (-4.5V)	Q <sub>g</sub>	—	4.9	—	nC	V <sub>GS</sub> = -4.5V, V <sub>DS</sub> = -6V, I <sub>D</sub> = -2A
Gate-Source Charge	Q <sub>gs</sub>	—	0.6	—	nC	
Gate-Drain Charge	Q <sub>gd</sub>	—	1.1	—	nC	
Turn-On Delay Time	t <sub>D(on)</sub>	—	4.45	—	ns	V <sub>DD</sub> = -6V, V <sub>GS</sub> = -4.5V, I <sub>DS</sub> = -2A, R <sub>G</sub> = 2Ω
Turn-On Rise Time	t <sub>r</sub>	—	12	—	ns	
Turn-Off Delay Time	t <sub>D(off)</sub>	—	100	—	ns	
Turn-Off Fall Time	t <sub>f</sub>	—	93	—	ns	

- Notes:
- Device mounted on FR-4 PCB with minimum recommended pad layout.
  - Device mounted on FR4 material with 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm thick) Cu.
  - Short duration pulse test used to minimize self-heating effect.
  - Guaranteed by design. Not subject to production testing.

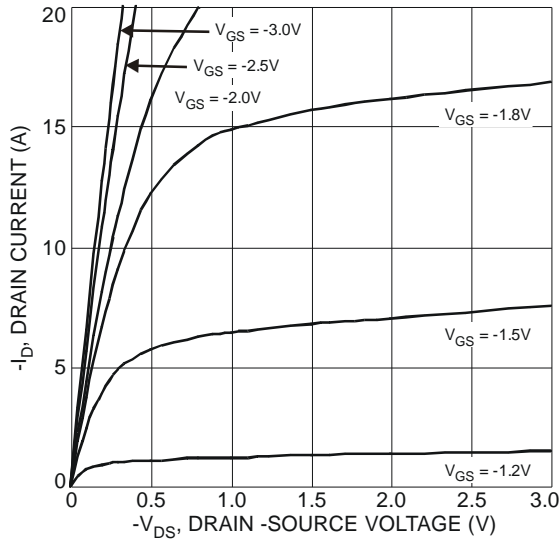


Figure 1 Typical Output Characteristics

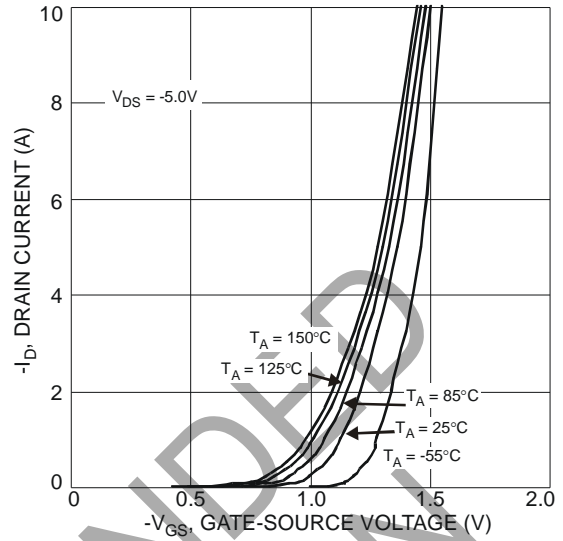


Figure 2 Typical Transfer Characteristics

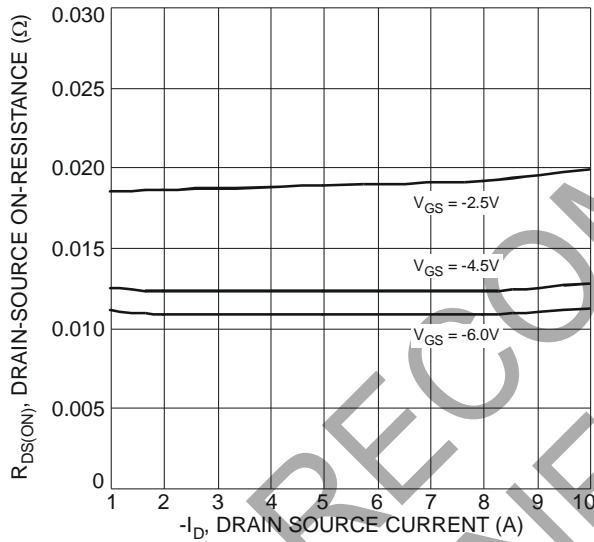


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

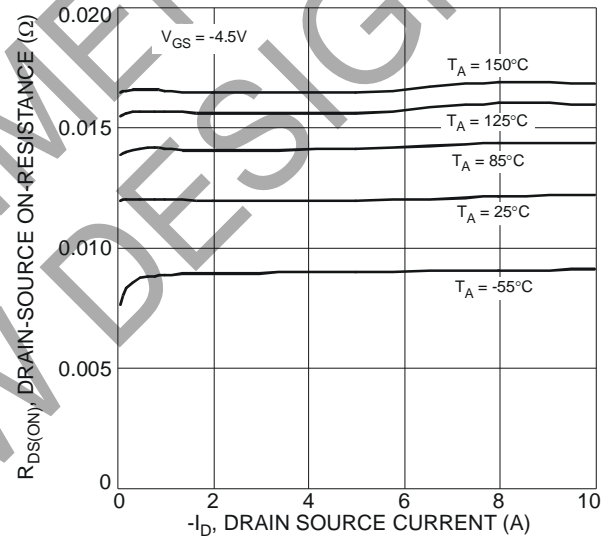


Figure 4 Typical On-Resistance vs. Drain Current and Temperature

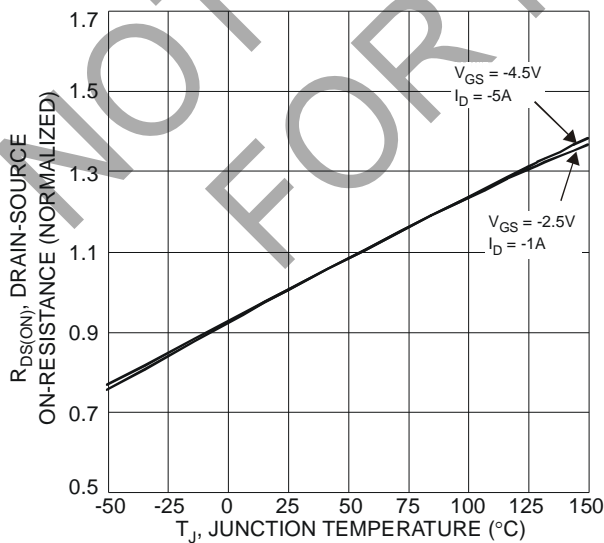


Figure 5 On-Resistance Variation with Temperature

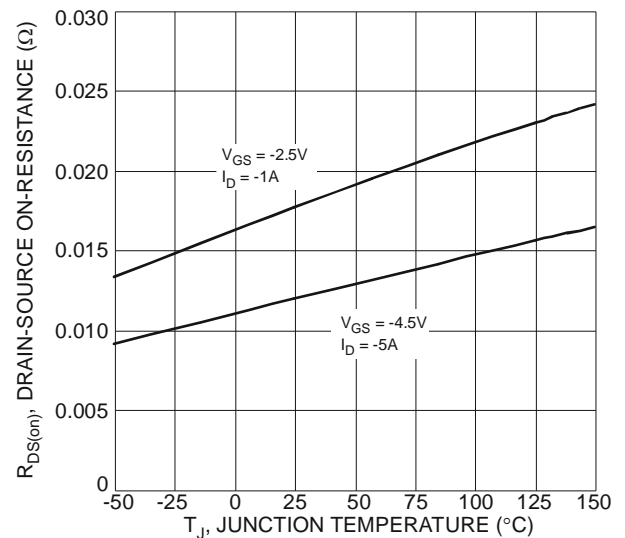


Figure 6 On-Resistance Variation with Temperature

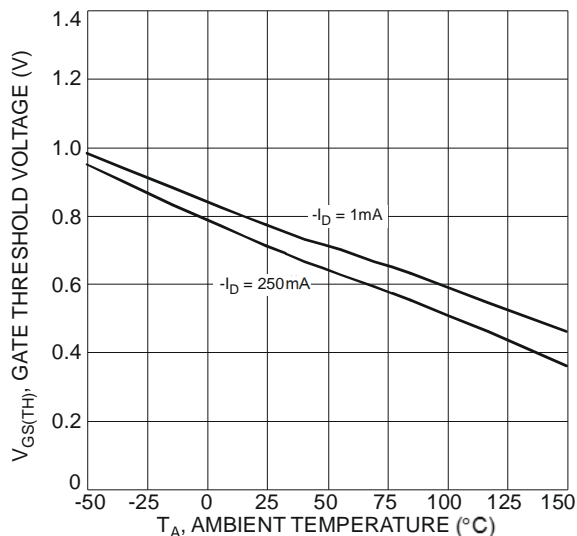


Figure 7 Gate Threshold Variation vs. Ambient Temperature

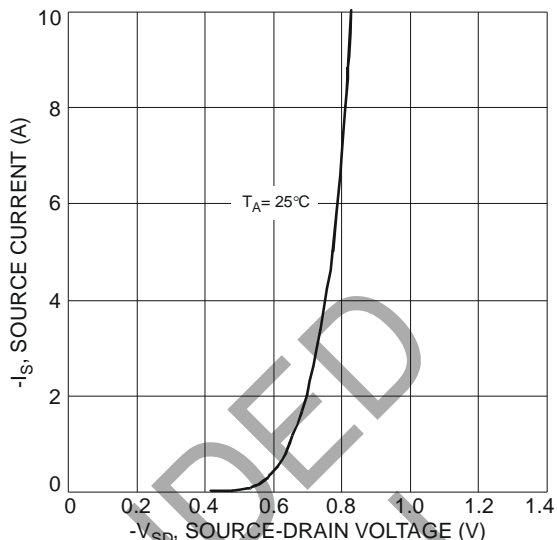


Figure 8 Diode Forward Voltage vs. Current

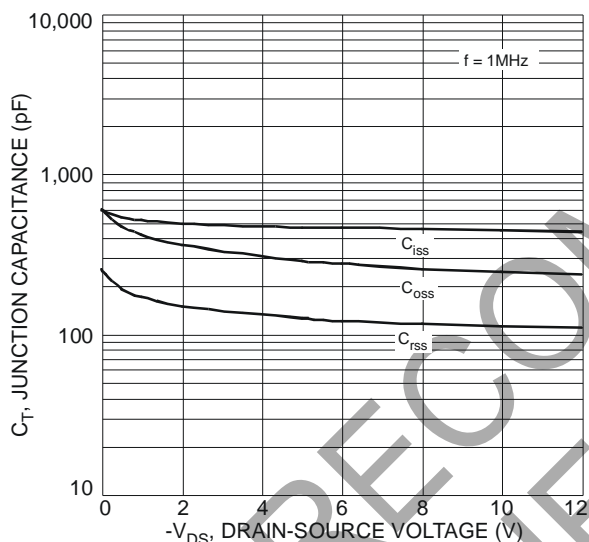


Figure 9 Typical Junction Capacitance

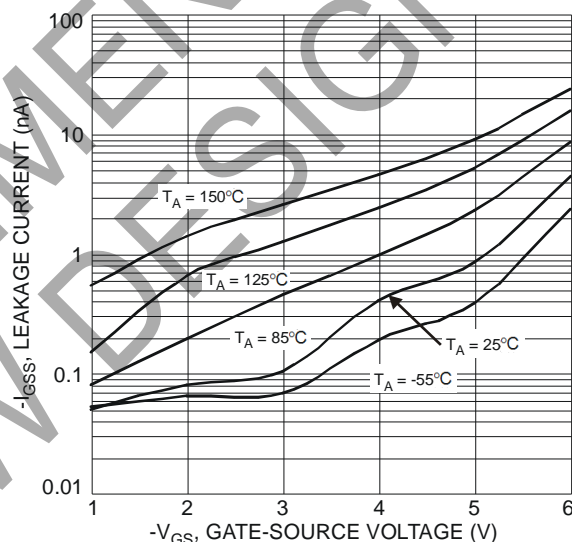


Figure 10 Typical Gate-Source Leakage Current vs. Voltage

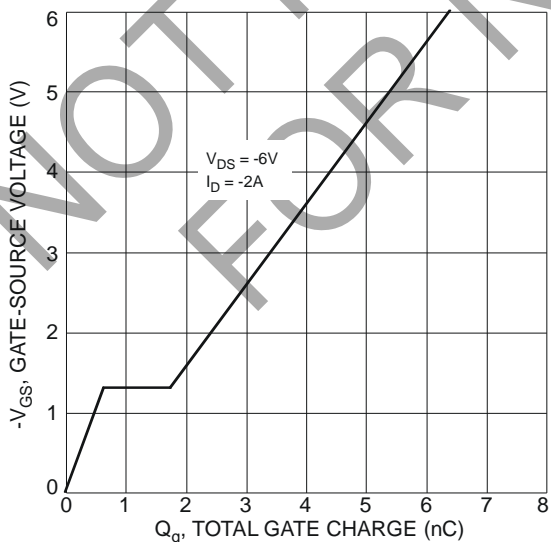


Figure 11 Gate-Charge Characteristics

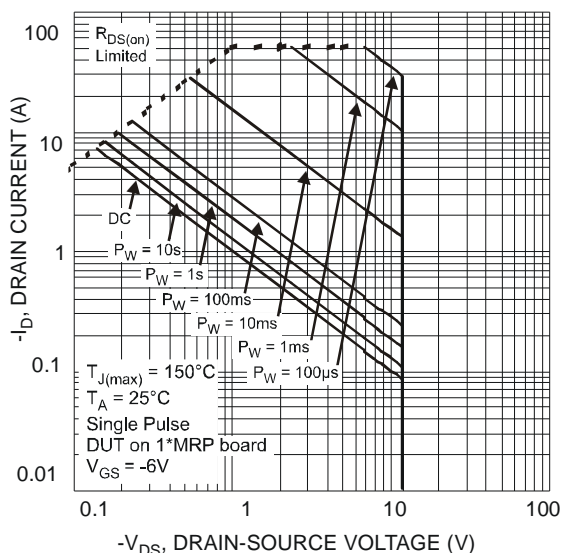


Figure 12 SOA, Safe Operation Area

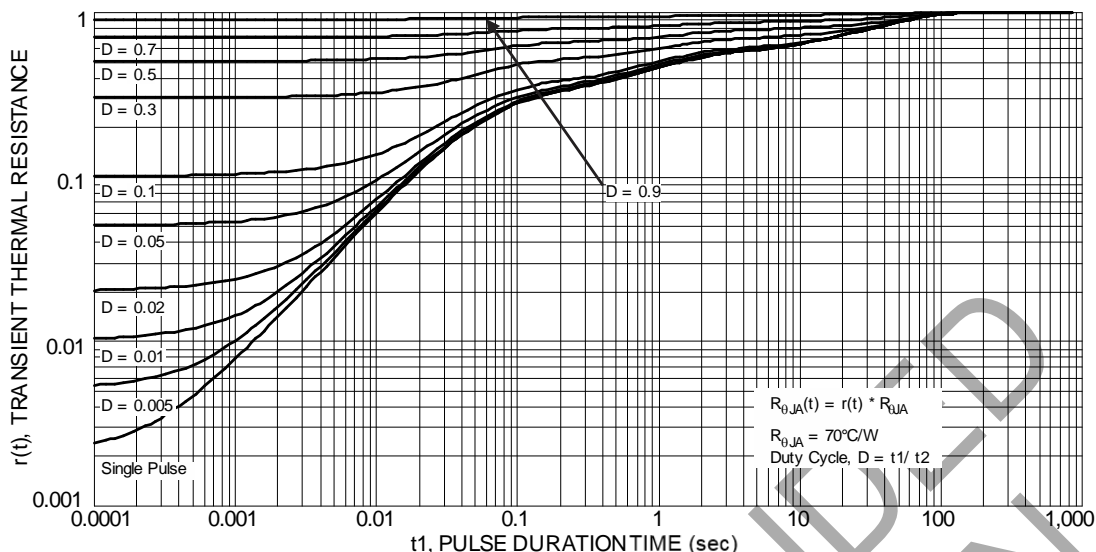
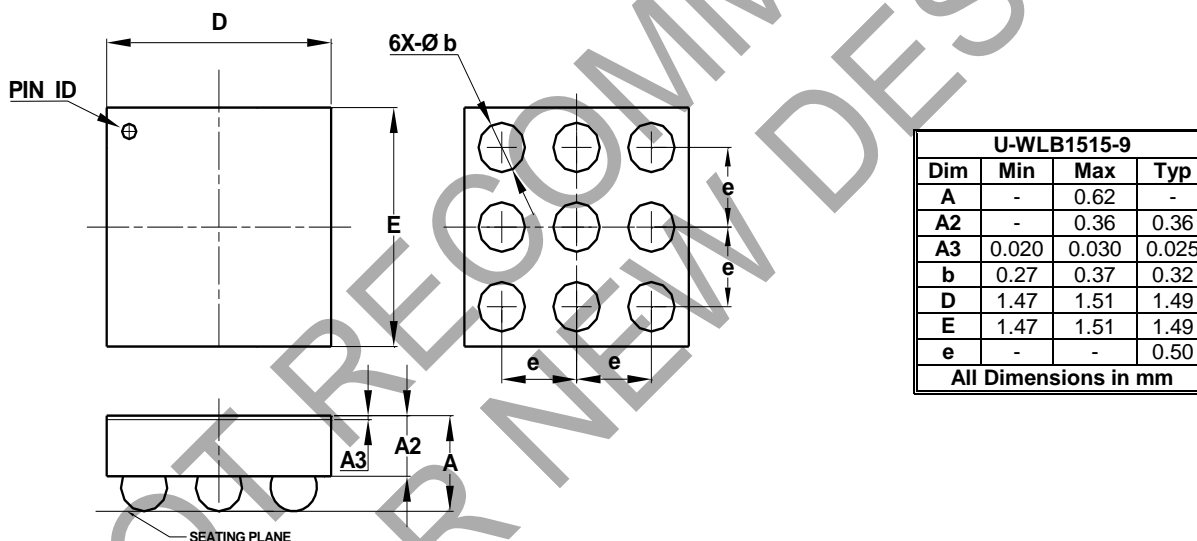


Figure 13 Transient Thermal Resistance

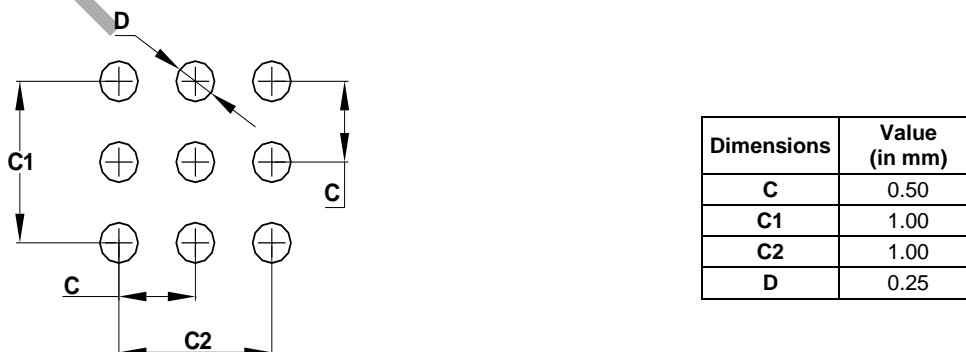
### Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.



### Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.



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