

HIGH FREQUENCY HIGH-SIDE AND LOW-SIDE GATE DRIVER IN V-QFN3030-8

Description

The DGD0590 is a high-frequency high-side and low-side gate driver capable of driving N-channel MOSFETs in a half-bridge configuration. The floating high-side driver is rated up to 50V and provides a 5V gate drive to the MOSFETs.

The DGD0590 logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with MCUs. A UVLO protects ICs and MOSFETs with loss of supply.

Fast and well-matched propagation delays allow a higher switching frequency, enabling a smaller, more compact power switching design, using smaller associated components. The DGD0590 is offered in the V-QFN3030-8 package and operates over an extended -40°C to +125°C temperature range.

Applications

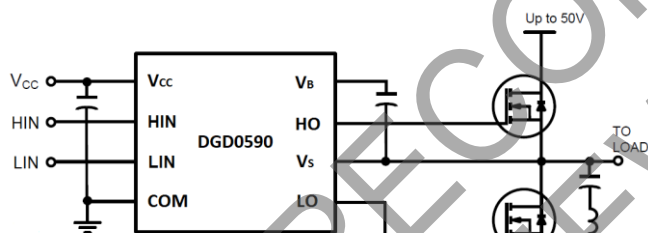
- Wireless Power Charger
- Motor Drive
- Logic Level MOSFET Gate Driver

Features

- 50V Floating High-Side Driver
- Low V_{CC} Operating Voltage: 4.5V to 5.5V
- Drives Two N-Channel Logic Level MOSFETs in a Half-Bridge Configuration
- High-Side 1.0A Source / 1.0A Sink and Low-Side 1.0A Source / 3.0A Sink Output Current Capability
- Internal Bootstrap Diode Included
- 3.4V UVLO with 0.4V Hysteresis
- Fast Rise and Fall Times (27ns/17ns) with 3nF Load
- Propagation Delay Typical of 16ns for High-Side and 12ns for Low-Side
- Extended Temperature Range: -40°C to +125°C
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony free. "Green" Device (Note 3)**

Mechanical Data

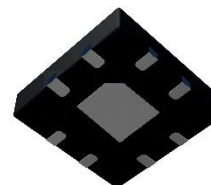
- Case: V-QFN3030-8 (Type TH)
- Case Material: Molded Plastic. "Green" Molding Compound
- UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 3 per J-STD-020
- Terminals: Finish—Matte Tin Finish; Solderable per MIL-STD-202, Method 208 (E3)
- Weight: 0.017 grams (Approximate)



Typical Configuration



Top View



Bottom View

V-QFN3030-8

Ordering Information (Note 4)

Product	Marking	Reel Size (inches)	Tape Width (mm)	Quantity per Reel
DGD0590FU-7	DGD0590	7	8	3000

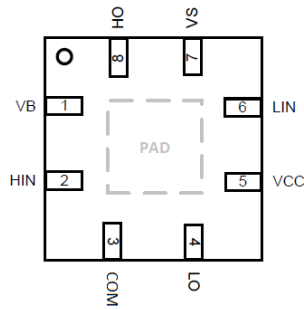
- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information



DGD0590 = Product Type Marking Code
 YY = Year (ex: 19 = 2019)
 WW = Week (01 to 53)

Pin Diagrams

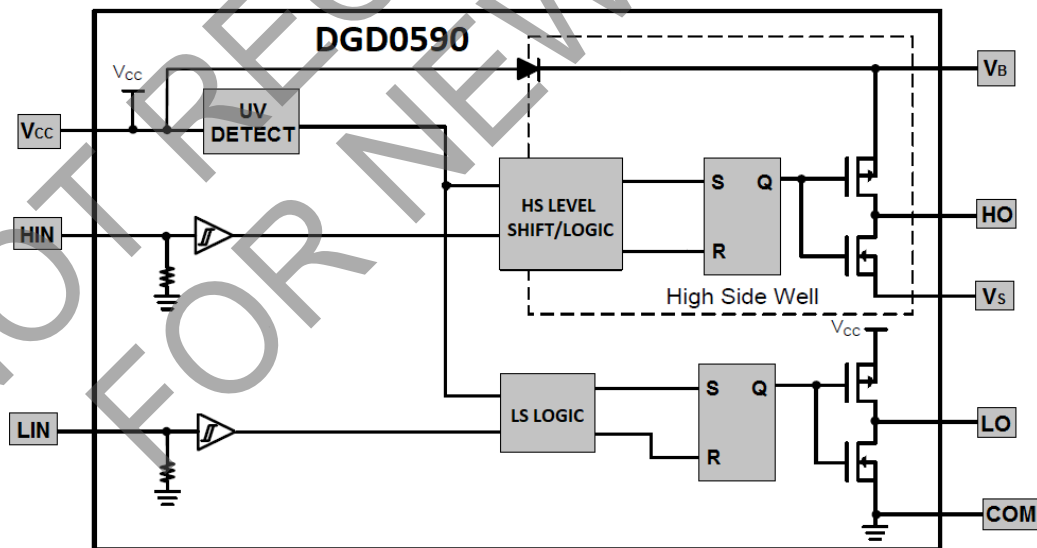


Top View: V-QFN3030-8

Pin Descriptions

Pin Number	Pin Name	Function
1	VB	High-Side Floating Supply
2	HIN	Logic Input for High-Side Gate Driver, in Phase with HO, Pull Down Resistor at Input
3	COM	Low-Side and Logic Return
4	LO	Low-Side Gate Driver Output
5	VCC	Low-Side and Logic Supply
6	LIN	Logic Input for Low-Side Gate Driver, in Phase with LO, Pull Down Resistor at Input
7	VS	High-Side Floating Supply Return
8	HO	High-Side Gate Driver Output
PAD	Substrate	Connect to COM on PCB

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
High-Side Floating Positive Supply Voltage	V _B	0.3 to +60	V
High-Side Floating Negative Supply Voltage	V _S	V _B -6 to V _B +0.3	V
High-Side Floating Output Voltage	V _{HO}	V _S -0.3 to V _B +0.3	V
Offset Supply Voltage Transient	dV _S / dt	50	V/ns
Logic and Low-Side Fixed Supply Voltage	V _{CC}	-0.3 to +6	V
Low-Side Output Voltage	V _{LO}	-0.3 to V _{CC} +0.3	V
Logic Input Voltage (HIN and LIN)	V _{IN}	-0.3 to +6	V

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Ambient (Note 5)	R _{eJA}	120	°C/W
Thermal Resistance, Junction to Case (Note 5)	R _{eJC}	132	°C/W
Operating Temperature	T _J	+150	°C
Lead Temperature (Soldering, 10s)	T _L	+300	
Storage Temperature Range	T _{STG}	-55 to +150	

Note: 5. When mounted on a standard JEDEC 2-layer FR-4 board.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
High-Side Floating Supply	V _B	V _S + 4.5	V _S + 5.5	V
High-Side Floating Supply Offset Voltage	V _S	0	50 (Note 6)	V
High-Side Floating Output Voltage	V _{HO}	V _S	V _B	V
Logic and Low Side Fixed Supply Voltage	V _{CC}	4.5	5.5	V
Low-Side Output Voltage	V _{LO}	0	V _{CC}	V
Logic Input Voltage (HIN and LIN)	V _{IN}	0	5	V
Ambient Temperature	T _A	-40	+125	°C

Note: 6. Provided V_B doesn't exceed absolute maximum rating of 60V.

DC Electrical Characteristics ($V_{CC} = 5V$, $@T_A = +25^\circ C$, unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Logic "1" Input Voltage, HIN	V_{HIH}	—	3.5	3.8	V	—
Logic "0" Input Voltage, HIN	V_{HIL}	1.0	1.3	—	V	—
Logic "1" Input Voltage, LIN	V_{LIH}	—	2.8	3.3	V	—
Logic "0" Input Voltage, LIN	V_{LIL}	1.0	1.2	—	V	—
Logic Input Bias Current	I_{IN+}	—	31	60	μA	$V_{IN} = V_{CC}$
V_{CC} Quiescent Supply Current	I_{CCQ}	—	22	50	μA	—
V_{CC} Operating Supply Current	I_{CCO}	—	300	—	μA	HO and LO Open, $f_s = 250kHz$
High-Side Source Impedance	R_{HSO}	—	1.8	2.6	Ω	Source = 100mA
High-Side Sink Impedance	R_{HSI}	—	1.5	2.1	Ω	Sink = 100mA
Low-Side Source Impedance	R_{LSO}	—	1.8	2.6	Ω	Source = 100mA
Low-Side Sink Impedance	R_{LSI}	—	0.4	1.0	Ω	Sink = 100mA
V_{CC} Supply Undervoltage Positive Going Threshold	V_{CCUV+}	2.85	3.4	3.85	V	—
V_{CC} Supply Undervoltage Hysteresis	V_{CCU_HYST}	—	0.4	—	V	—
Bootstrap Diode Forward Voltage	V_{BFD}	—	650	800	mV	$I = 100\mu A$
Bootstrap Diode Reverse Leakage	I_{BDL}	—	0.1	0.4	μA	$V_B = V_S = 55.5V$, $V_{CC} = 0V$

AC Electrical Characteristics ($V_{CC} = 5V$, $C_L = 3nF$, $@T_A = +25^\circ C$, unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Turn-on Rise Time	t_r	—	27	—	ns	—
Turn-off Fall Time, High-Side	t_f	—	29	—	ns	—
Turn-off Fall Time, Low-Side		—	17	—	ns	—
Turn-on Propagation Delay, High-Side	t_{ONH}	—	16	—	ns	—
Turn-off Propagation Delay, High-Side	t_{OFFH}	—	17	—	ns	—
Turn-on Propagation Delay, Low-Side	t_{ONL}	—	12	—	ns	—
Turn-off Propagation Delay, Low-Side	t_{OFFL}	—	17	—	ns	—

Timing Waveforms

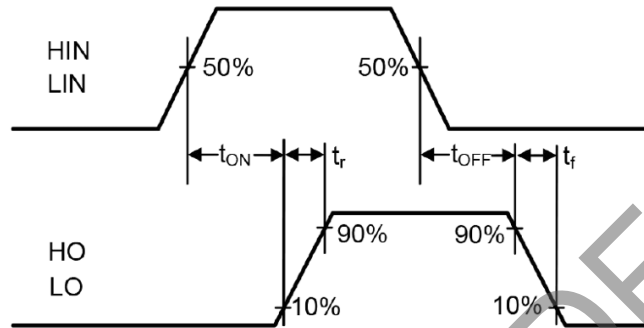


Figure 1. Switching Time Waveform Definitions

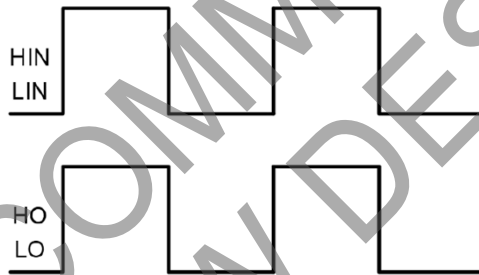


Figure 2. Input / Output Timing Diagram

NOT RECOMMENDED FOR NEW DESIGN

Typical Performance Characteristics ($V_{CC} = 5V$, $@T_A = +25^\circ C$, unless otherwise specified.)

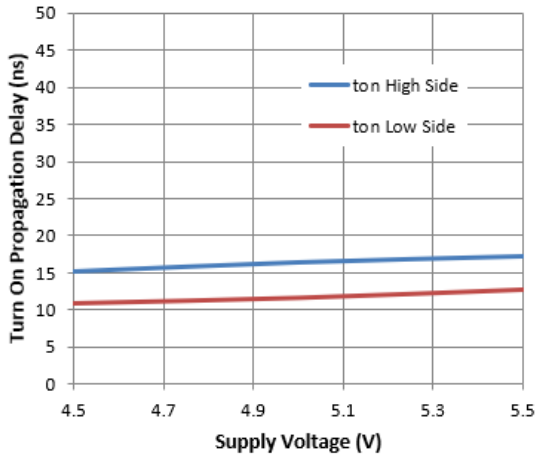


Figure 3. Turn-on Propagation Delay vs. Supply Voltage

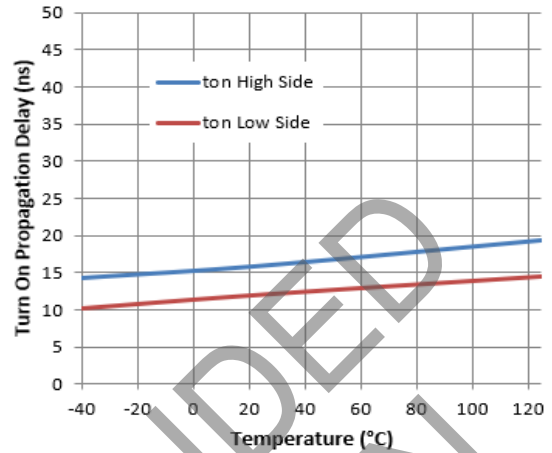


Figure 4. Turn-on Propagation Delay vs. Temperature

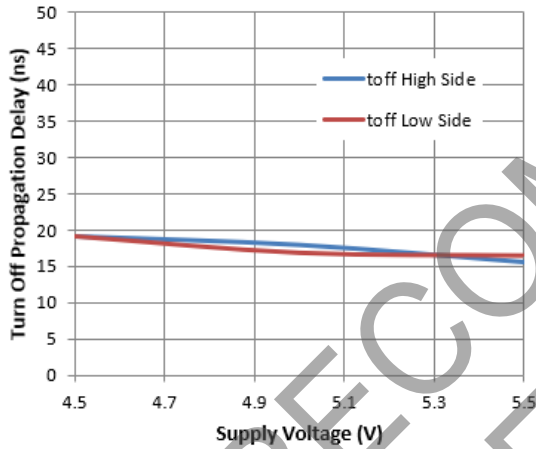


Figure 5. Turn-off Propagation Delay vs. Supply Voltage

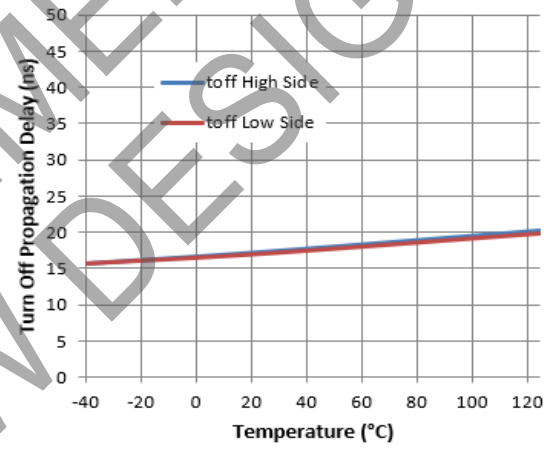


Figure 6. Turn-off Propagation Delay vs. Temperature

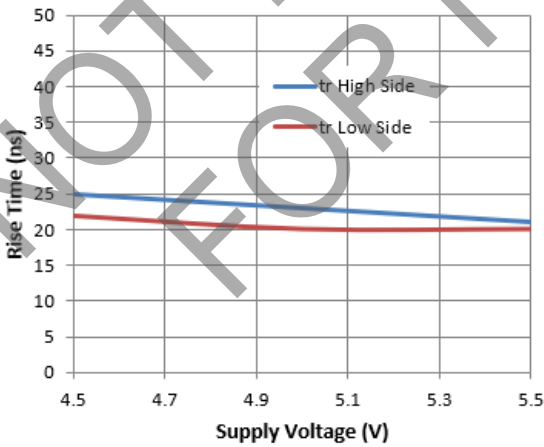


Figure 7. Rise Time vs. Supply Voltage

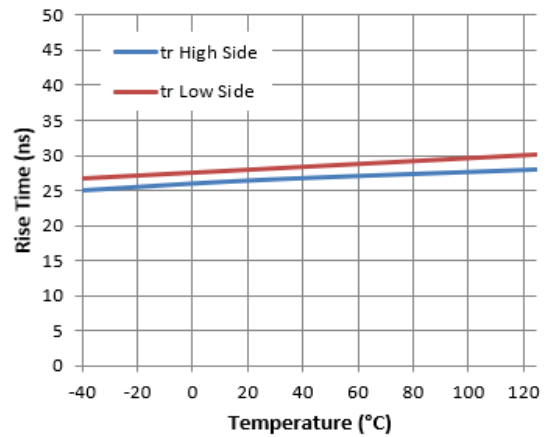


Figure 8. Rise Time vs. Temperature

Typical Performance Characteristics (continued)

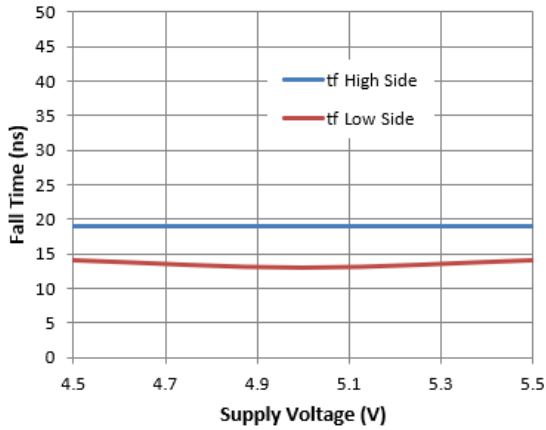


Figure 9. Fall Time vs. Supply Voltage

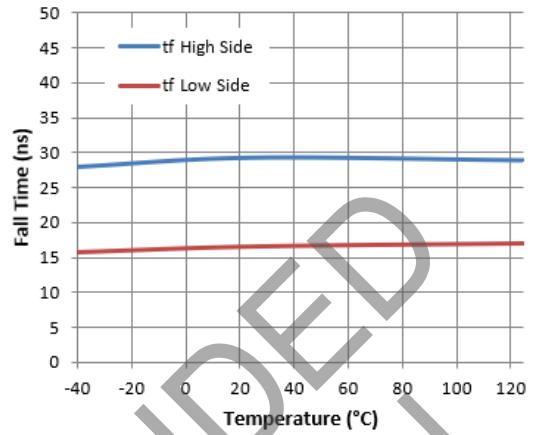


Figure 10. Fall Time vs. Temperature

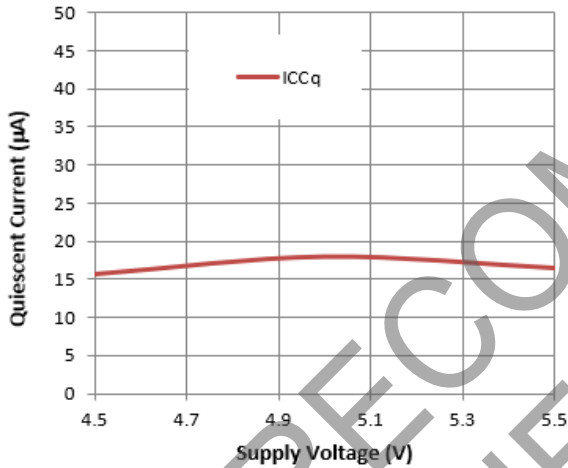


Figure 11. Quiescent Current vs. Supply Voltage

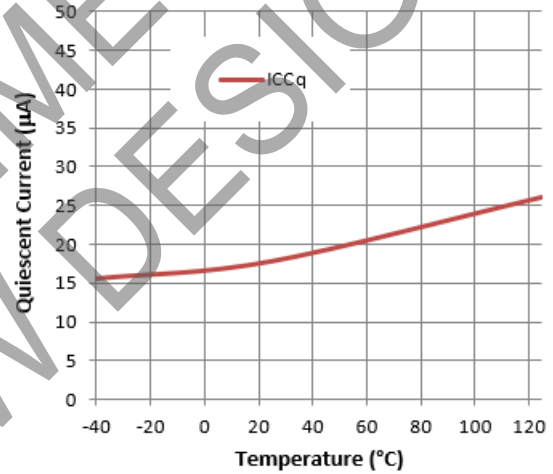


Figure 12. Quiescent Current vs. Temperature

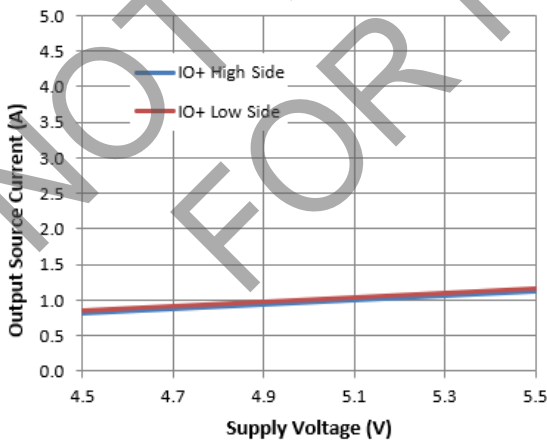


Figure 13. Output Source Current vs. Supply Voltage

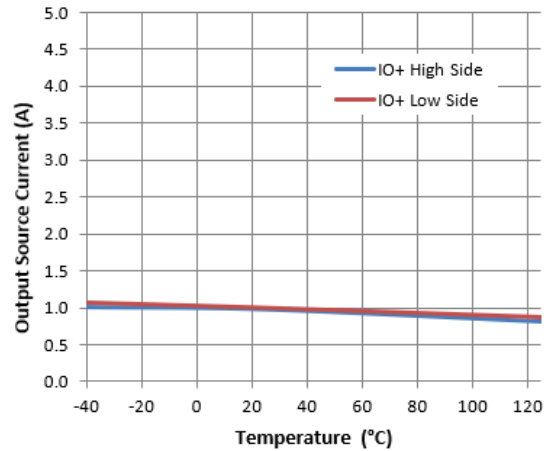


Figure 14. Output Source Current vs. Temperature

Typical Performance Characteristics (continued)

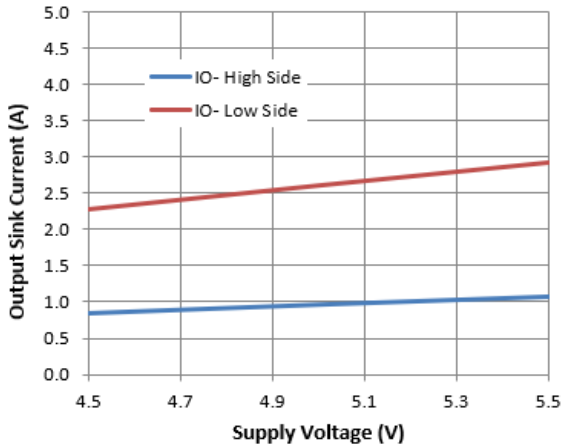


Figure 15. Output Sink Current vs. Supply Voltage

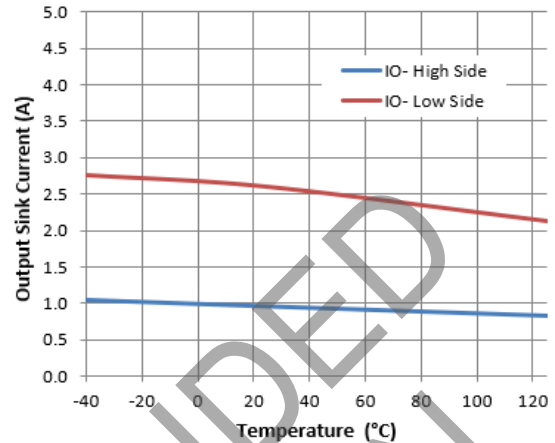


Figure 16. Output Sink Current vs. Temperature

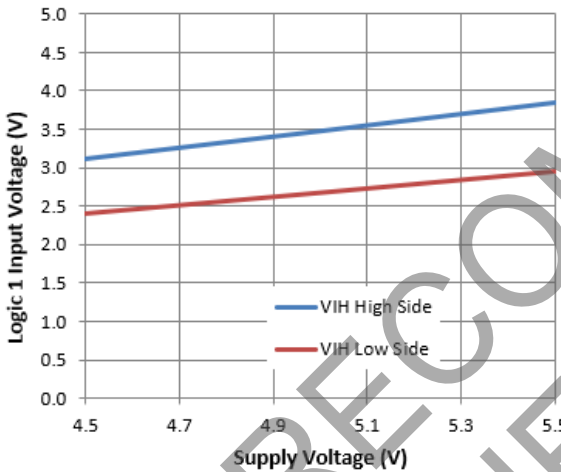


Figure 17. Logic 1 Input Voltage vs. Supply Voltage

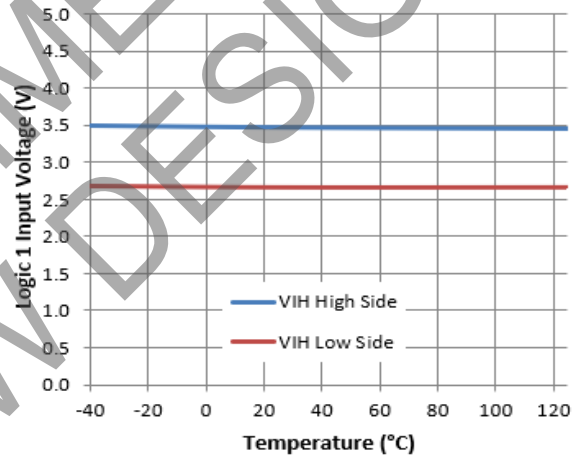


Figure 18. Logic 1 Input Voltage vs. Temperature

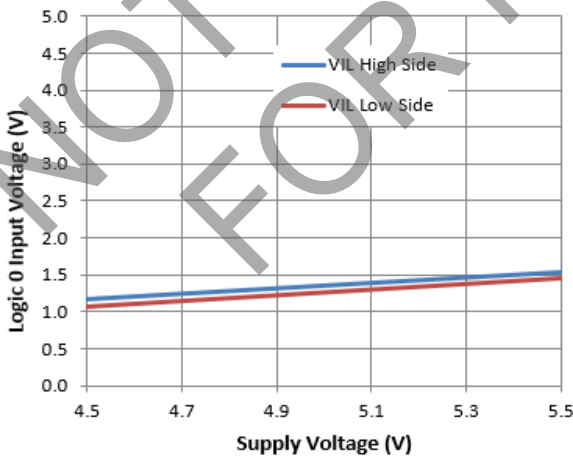


Figure 19. Logic 0 Input Voltage vs. Supply Voltage

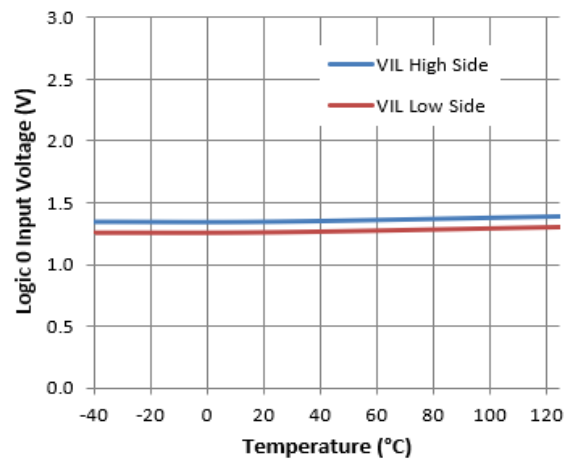


Figure 20. Logic 0 Input Voltage vs. Temperature

Typical Performance Characteristics (continued)

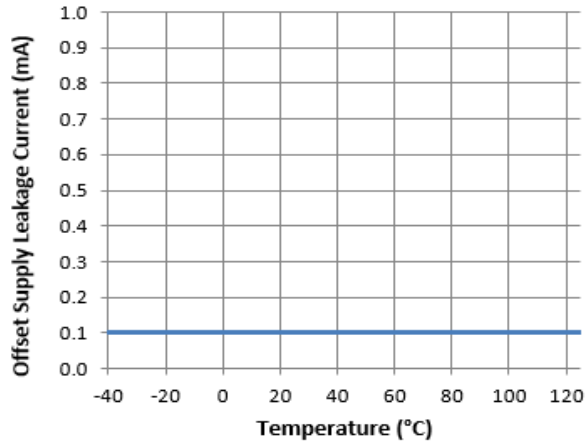


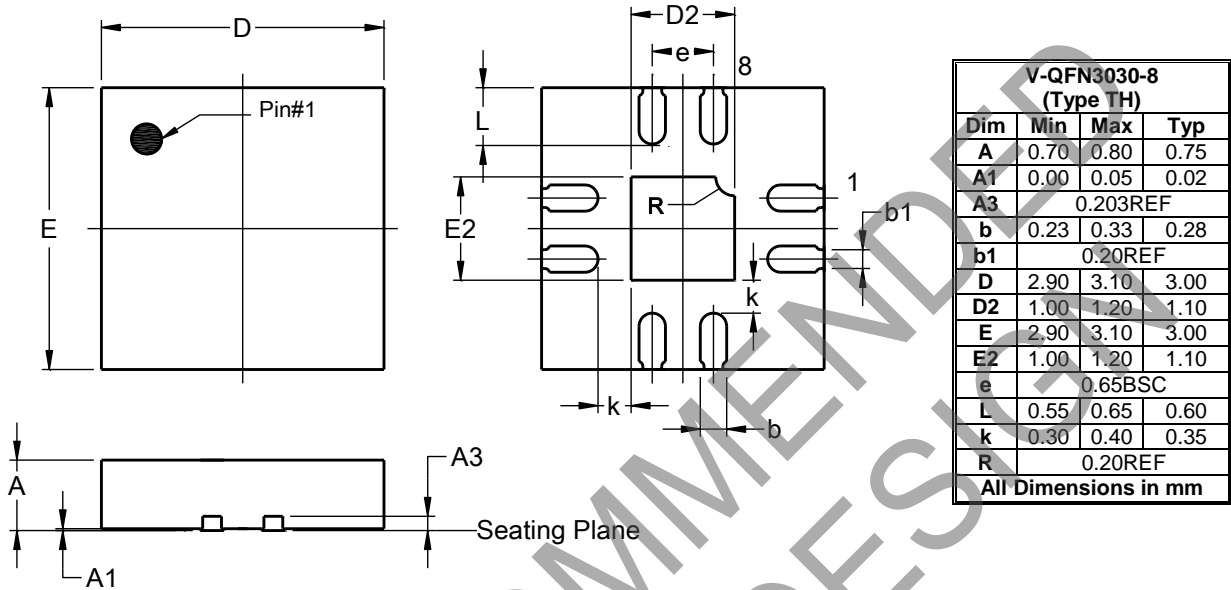
Figure 21. Offset Supply Leakage Current vs. Temperature

NOT RECOMMENDED
FOR NEW DESIGN

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

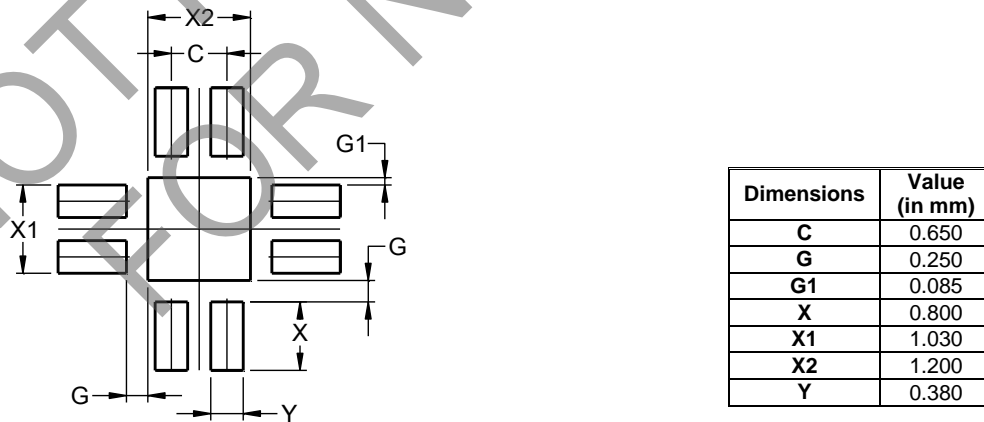
V-QFN3030-8 (Type TH)



Suggested Pad Layout

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V-QFN3030-8 (Type TH)



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