General Description

The AUR9707 is a high efficiency step-down DC-DC voltage converter. The chip operation is optimized using constant frequency, peak-current mode architecture with built-in synchronous power MOSFET switches and internal compensators to reduce external part counts. It is automatically switching between the normal PWM mode and LDO mode to offer improved system power efficiency covering a wide range of loading conditions.

The oscillator and timing capacitors are all built-in providing an internal switching frequency of 1.5MHz that allows the use of small surface mount inductors and capacitors for portable product implementations. Additional features included Soft Start (SS), Under Voltage Lock Out (UVLO), Input Over Voltage Protection (IOVP) and Thermal Shutdown Detection (TSD) are integrated to provide reliable product applications.

The device is available in adjustable output voltage versions ranging from 1V to 3.3V, and is able to deliver up to 1A.

The AUR9707 is available in WDFN-3×3-12 package.

Features

- Dual Channel High Efficiency Buck Power Converter
- Low Quiescent Current
- Output Current: 1A
- Adjustable Output Voltage from 1V to 3.3V
- Wide Operating Voltage Range: 2.5V to 5.5V
- Built-in Power Switches for Synchronous Rectification with High Efficiency
- Feedback Voltage: 600mV
- 1.5MHz Constant Frequency Operation
- Automatic PWM/LDO Mode Switching Control
- Thermal Shutdown Protection
- Low Drop-out Operation at 100% Duty Cycle
- No Schottky Diode Required
- Internal Input Over Voltage Protection

Applications

- Mobile Phone, Digital Camera and MP3 Player
- Headset, Radio and Other Hand-held Instrument
- Post DC-DC Voltage Regulation
- PDA and Notebook Computer

![WDFN-3x3-12](image_url)

Figure 1. Package Type of AUR9707
Pin Configuration

D Package
(WDFN-3×3-12)

Exposed Pad

Figure 2. Pin Configuration of AUR9707 (Top View)

Pin Description

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VIN2</td>
<td>Power supply input of channel 2</td>
</tr>
<tr>
<td>2</td>
<td>LX2</td>
<td>Connection from power MOSFET of channel 2 to inductor</td>
</tr>
<tr>
<td>3, 9</td>
<td>GND</td>
<td>This pin is the GND reference for the NMOSFET power stage. It must be connected to the system ground</td>
</tr>
<tr>
<td>4</td>
<td>FB1</td>
<td>Feedback voltage of channel 1</td>
</tr>
<tr>
<td>5, 11</td>
<td>NC1, NC2</td>
<td>No internal connection (floating or connecting to GND)</td>
</tr>
<tr>
<td>6</td>
<td>EN1</td>
<td>Enable signal input of channel 1, active high</td>
</tr>
<tr>
<td>7</td>
<td>VIN1</td>
<td>Power supply input of channel 1</td>
</tr>
<tr>
<td>8</td>
<td>LX1</td>
<td>Connection from power MOSFET of channel 1 to inductor</td>
</tr>
<tr>
<td>10</td>
<td>FB2</td>
<td>Feedback voltage of channel 2</td>
</tr>
<tr>
<td>12</td>
<td>EN2</td>
<td>Enable signal input of channel 2, active high</td>
</tr>
</tbody>
</table>
Functional Block Diagram

Figure 3. Functional Block Diagram of AUR9707

Ordering Information

<table>
<thead>
<tr>
<th>Package</th>
<th>Temperature Range</th>
<th>Part Number</th>
<th>Marking ID</th>
<th>Packing Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>WDFN-3x3-12</td>
<td>-40 to 80°C</td>
<td>AUR9707AGD</td>
<td>9707A</td>
<td>Tape &amp; Reel</td>
</tr>
</tbody>
</table>

BCD Semiconductor's Pb-free products, as designated with “G” in the part number, are RoHS compliant and green.
## Absolute Maximum Ratings (Note 1)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Input Voltage</td>
<td>$V_{IN}$</td>
<td>0 to 6.5</td>
<td>V</td>
</tr>
<tr>
<td>Enable Input Voltage</td>
<td>$V_{EN}$</td>
<td>-0.3 to $V_{IN}+0.3$</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>$V_{OUT}$</td>
<td>-0.3 to $V_{IN}+0.3$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IN1}-V_{IN2}$ Voltage (Note 2)</td>
<td>$V_{DF}$</td>
<td>0.3 to 0.3</td>
<td>V</td>
</tr>
<tr>
<td>Power Dissipation (On PCB, $T_A=30^\circ$C)</td>
<td>$P_D$</td>
<td>2.31</td>
<td>W</td>
</tr>
<tr>
<td>Thermal Resistance (Junction to Ambient, Simulation)</td>
<td>$\theta_{JA}$</td>
<td>41</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal Resistance (Junction to Case, Simulation)</td>
<td>$\theta_{JC}$</td>
<td>4.2</td>
<td>°C/W</td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td>$T_J$</td>
<td>160</td>
<td>°C</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>$T_0$</td>
<td>-40 to 85</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>$T_S$</td>
<td>-55 to 150</td>
<td>°C</td>
</tr>
<tr>
<td>ESD (Human Body Model)</td>
<td>$V_{HBM}$</td>
<td>2000</td>
<td>V</td>
</tr>
<tr>
<td>ESD (Machine Model)</td>
<td>$V_{MM}$</td>
<td>200</td>
<td>V</td>
</tr>
</tbody>
</table>

Note 1: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

Note 2: $|V_{IN1}-V_{IN2}|$ voltage difference can not exceed 0.3V, otherwise, the chip will be damaged.

## Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Input Voltage</td>
<td>$V_{IN}$</td>
<td>2.5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Junction Temperature Range</td>
<td>$T_J$</td>
<td>-20</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Ambient Temperature Range</td>
<td>$T_A$</td>
<td>-40</td>
<td>80</td>
<td>°C</td>
</tr>
</tbody>
</table>
## Electrical Characteristics

$V_{IN}=3.6\,V$, $V_{OUT}=2.5\,V$, $V_{REF}=0.6\,V$, $L=2.2\,\mu F$, $C_{IN}=4.7\,\mu F$, $C_{OUT}=10\,\mu F$, $T_{A}=25^\circ C$, $I_{MAX}=1\,A$.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage Range</td>
<td>$V_{IN}$</td>
<td></td>
<td>2.5</td>
<td></td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Shutdown Current</td>
<td>$I_{OFF}$</td>
<td>$V_{EN}=0$</td>
<td></td>
<td>0.1</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>Regulated Feedback Voltage</td>
<td>$V_{FB}$</td>
<td>For Adjustable Output Voltage</td>
<td>0.585</td>
<td>0.6</td>
<td>0.615</td>
<td>V</td>
</tr>
<tr>
<td>Regulated Output Voltage Accuracy</td>
<td>$\Delta V_{OUT}/V_{OUT}$</td>
<td>$V_{IN}=2.5,V$ to $5.5,V$; $I_{OUT}=0$ to $1A$</td>
<td>-3</td>
<td></td>
<td>3</td>
<td>%</td>
</tr>
<tr>
<td>Peak Inductor Current</td>
<td>$I_{PK}$</td>
<td>$V_{IN}=3,V$, $V_{FB}=0.5,V$</td>
<td></td>
<td>1.5</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>Oscillator Frequency</td>
<td>$f_{OSC}$</td>
<td>$V_{IN}=3.6,V$</td>
<td>1.2</td>
<td>1.5</td>
<td>1.8</td>
<td>MHz</td>
</tr>
<tr>
<td>PMOSFET $R_{ON}$</td>
<td>$R_{ON(P)}$</td>
<td>$V_{IN}=3.6,V$, $I_{OUT}=200mA$</td>
<td></td>
<td>0.28</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NMOSFET $R_{ON}$</td>
<td>$R_{ON(N)}$</td>
<td>$V_{IN}=2.5,V$, $I_{OUT}=200mA$</td>
<td></td>
<td>0.38</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input DC Bias Current</td>
<td>$I_{S}$</td>
<td>$V_{IN}=3.6,V$, $I_{OUT}=200mA$</td>
<td></td>
<td>0.25</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LX Leakage Current</td>
<td>$I_{LX}$</td>
<td>$V_{IN}=5,V$, $V_{EN}=0,V$, $V_{LX}=0,V$ or $5,V$</td>
<td>0.01</td>
<td></td>
<td>0.1</td>
<td>µA</td>
</tr>
<tr>
<td>Feedback Current</td>
<td>$I_{FB}$</td>
<td></td>
<td></td>
<td>30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Over Voltage Protection</td>
<td>$V_{LOVP}$</td>
<td></td>
<td></td>
<td>6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN Leakage Current</td>
<td>$I_{EN}$</td>
<td></td>
<td></td>
<td>0.01</td>
<td></td>
<td>0.1</td>
</tr>
<tr>
<td>EN High-level Input Voltage</td>
<td>$V_{EN_H}$</td>
<td>$V_{IN}=2.5,V$ to $5.5,V$</td>
<td></td>
<td>1.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN Low-Level Input Voltage</td>
<td>$V_{EN_L}$</td>
<td>$V_{IN}=2.5,V$ to $5.5,V$</td>
<td></td>
<td></td>
<td></td>
<td>0.6</td>
</tr>
<tr>
<td>Under Voltage Lock Out</td>
<td></td>
<td></td>
<td></td>
<td>1.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hysteresis</td>
<td></td>
<td></td>
<td></td>
<td>0.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Shutdown</td>
<td>$T_{SD}$</td>
<td></td>
<td></td>
<td>150</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Typical Performance Characteristics

Figure 4. Efficiency vs. Output Current

Figure 5. Efficiency vs. Load Current

Figure 6. Efficiency vs. Load Current

Figure 7. LDO Mode Efficiency vs. Load Current
Typical Performance Characteristics (Continued)

Figure 8. Output Voltage vs. Output Current

Figure 9. UVLO Threshold vs. Temperature

Figure 10. Output Voltage vs. Output Current

Figure 11. Frequency vs. Temperature
Typical Performance Characteristics (Continued)

**Figure 12. Output Current Limit vs. Input Voltage**

**Figure 13. Output Voltage vs. Temperature**

**Figure 14. Frequency vs. Input Voltage**

**Figure 15. Output Current Limit vs. Temperature**
Typical Performance Characteristics (Continued)

Figure 16. Temperature vs. Load Current

Figure 17. Waveform of $V_{\text{IN}}=4.5\text{V}$, $V_{\text{OUT}}=1.5\text{V}$, $L=2.2\mu\text{H}$

Figure 18. Soft Start
Application Information

The basic AUR9707 application circuit is shown in Figure 23, external components selection is determined by the load current and is critical with the selection of inductor and capacitor values.

1. Inductor Selection
For most applications, the value of inductor is chosen based on the required ripple current with the range of 2.2μH to 4.7μH.

\[ \Delta I_L = \frac{1}{f \times \Delta L_{(MAX)}(MAX)} \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \]

The largest ripple current occurs at the highest input voltage. Having a small ripple current reduces the ESR loss in the output capacitor and improves the efficiency. The highest efficiency is realized at low operating frequency with small ripple current. However, larger value inductors will be required. A reasonable starting point for ripple current setting is \( \Delta I_L = 40\% I_{L\text{MAX}} \). For a maximum ripple current stays below a specified value, the inductor should be chosen according to the following equation:

\[ L = \left[ \frac{V_{OUT}}{f \times \Delta I_L(MAX)} \right] \left[1 - \frac{V_{OUT}}{V_{IN}(MAX)}\right] \]

The DC current rating of the inductor should be at least equal to the maximum output current plus half the highest ripple current to prevent inductor core saturation. For better efficiency, a lower DC-resistance inductor should be selected.

2. Capacitor Selection
The input capacitance, \( C_{IN} \), is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

\[ I_{RMS} = I_{OMAX} \times \left(\frac{V_{OUT} - V_{IN}}{V_{IN}}\right)^{\frac{1}{2}} \]

It indicates a maximum value at \( V_{IN} = 2V_{OUT} \), where \( I_{RMS} = I_{OMAX}/2 \). This simple worse-case condition is commonly used for design because even significant deviations do not much relieve. The selection of \( C_{OUT} \) is determined by the Effective Series Resistance (ESR) that is required to minimize output voltage ripple and load step transients, as well as the amount of bulk capacitor that is necessary to ensure that the control loop is stable. Loop stability can also be checked by examining the load step transient response as described in the following section. The output ripple, \( \Delta V_{OUT} \), is determined by:

\[ \Delta V_{OUT} \leq \Delta I_L \left[ ESR + \frac{1}{8 \times f \times C_{OUT}} \right] \]

The output ripple is the highest at the minimum input voltage since \( \Delta I_L \) increases with input voltage.

3. Load Transient
A switching regulator typically takes several cycles to respond to the load current step. When a load step occurs, \( V_{OUT} \) immediately shifts by an amount equal to \( \Delta I_{LOAD} \times ESR \), where ESR is the effective series resistance of output capacitor. \( \Delta I_{LOAD} \) also begins to charge or discharge \( C_{OUT} \) generating a feedback error signal used by the regulator to return \( V_{OUT} \) to its steady-state value. During the recovery time, \( V_{OUT} \) can be monitored for overshoot or ringing that would indicate a stability problem.

4. Output Voltage Setting
The output voltage of AUR9707 can be adjusted by a resistive divider according to the following formula:

\[ V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) = 0.6V \times \left(1 + \frac{R_1}{R_2}\right) \]

The resistive divider senses the fraction of the output voltage as shown in Figure 19.
Application Information (Continued)

5. Efficiency Considerations

The efficiency of switching regulator is equal to the output power divided by the input power times 100%. It is usually useful to analyze the individual losses to determine what is limiting efficiency and which change could produce the largest improvement. Efficiency can be expressed as:

\[ \text{Efficiency} = 100\% - L1 - L2 - \ldots \]

Where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the regulator produce losses, two major sources usually account for most of the power losses: \( V_{IN} \) quiescent current and \( IR \) losses. The \( V_{IN} \) quiescent current loss dominates the efficiency loss at very light load currents and the \( IR \) loss dominates the efficiency loss at medium to heavy load currents.

5.1 The \( V_{IN} \) quiescent current loss comprises two parts: the DC bias current as given in the electrical characteristics and the internal MOSFET switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each cycle the gate is switched from high to low, then to high again, and the packet of charge, \( dQ \), moves from \( V_{IN} \) to ground. The resulting \( dQ/dt \) is the current out of \( V_{IN} \) that is typically larger than the internal DC bias current. In continuous mode,

\[ I_{GATE} = f \times (Q_P + Q_N) \]

Where \( Q_P \) and \( Q_N \) are the gate charge of power PMOSFET and NMOSFET switches. Both the DC bias current and gate charge losses are proportional to the \( V_{IN} \) and this effect will be more serious at higher input voltages.

5.2 \( IR \) losses are calculated from internal switch resistance, \( R_{SW} \) and external inductor resistance \( R_L \). In continuous mode, the average output current flowing through the inductor is chopped between power PMOSFET switch and NMOSFET switch. Then, the series resistance looking into the LX pin is a function of both PMOSFET \( R_{DS(ON)} \) and NMOSFET \( R_{DS(ON)} \) resistance and the duty cycle (D):

\[ R_{SW} = R_{DS(ON)} \times D + R_{DS(ON)} \times (1 - D) \]

Therefore, to obtain the \( IR \) losses, simply add \( R_{SW} \) to \( R_L \) and multiply the result by the square of the average output current.

Other losses including \( C_IN \) and \( C_OUT \) ESR dissipative losses and inductor core losses generally account for less than 2% of total additional loss.

6. Thermal Characteristics

In most applications, the part does not dissipate much heat due to its high efficiency. However, in some conditions when the part is operating in high ambient temperature with high \( R_{DS(ON)} \) resistance and high duty cycles, such as in LDO mode, the heat dissipated may exceed the maximum junction temperature. To avoid the part from exceeding maximum junction temperature, the user should do some thermal analysis. The maximum power dissipation depends on the layout of PCB, the thermal resistance of IC package, the rate of surrounding airflow and the temperature difference between junction and ambient.

7. PCB Layout Considerations

When laying out the printed circuit board, the following checklist should be used to optimize the performance of AUR9707.

1) The power traces, including the GND trace, the LX trace and the VIN trace should be kept direct, short and wide.
2) Put the input capacitor as close as possible to the VIN and GND pins.
3) The FB pin should be connected directly to the feedback resistor divider.
4) Keep the switching node, LX, away from the sensitive FB pin and the node should be kept small area.
5) The following is an example of 2-layer PCB layout as shown in Figure 21 and Figure 22 for reference.
Application Information (Continued)

Figure 20. The Evaluation Board Schematic

Figure 21. Top Layer Layout

Figure 22. Bottom Layer Layout
Typical Application

Note 3: $V_{OUT1} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)$; $V_{OUT2} = V_{REF} \times \left(1 + \frac{R_3}{R_4}\right)$

When R2 or R4=300kΩ to 60 kΩ, the Ic1 or Ic4=2μA to 10μA, and R1×C1 or R3×C2 should be in the range between $3\times10^{-6}$ and $6\times10^{-6}$ for component selection.

Figure 23. Typical Application Circuit of AUR9707

<table>
<thead>
<tr>
<th>V_{OUT1} or V_{OUT2}(V)</th>
<th>R1 or R3(kΩ)</th>
<th>R2 or R4(kΩ)</th>
<th>C1 or C2(pF)</th>
<th>L1 or L2(µH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3</td>
<td>240</td>
<td>53</td>
<td>20</td>
<td>2.2</td>
</tr>
<tr>
<td>2.5</td>
<td>240</td>
<td>75</td>
<td>20</td>
<td>2.2</td>
</tr>
<tr>
<td>1.8</td>
<td>240</td>
<td>120</td>
<td>20</td>
<td>2.2</td>
</tr>
<tr>
<td>1.5</td>
<td>240</td>
<td>160</td>
<td>20</td>
<td>2.2</td>
</tr>
<tr>
<td>1.2</td>
<td>240</td>
<td>240</td>
<td>20</td>
<td>2.2</td>
</tr>
<tr>
<td>1.0</td>
<td>240</td>
<td>300</td>
<td>20</td>
<td>2.2</td>
</tr>
</tbody>
</table>

Table 1. Component Guide
Mechanical Dimensions

WDFN-3×3-12

Unit: mm (inch)

TOP VIEW
2.900(0.114)
3.100(0.122)

BOTTOM VIEW
2.250(0.089)
2.500(0.098)

SIDE VIEW
0.203(0.008)
0.000(0.000)
0.050(0.002)

N7
N6
N5
N4
N3
N1
N2

0.150(0.006)
0.250(0.010)
0.350(0.014)
0.450(0.018)

0.700(0.028)
0.800(0.031)
1.350(0.053)
1.800(0.071)

0.250(0.010)
0.450(0.018)

0.800(0.031)

0.240(0.0094)

Recommend Footprint

Pin 1 Dot by Marking

Unit:

mm (inch)
BCD Semiconductor Manufacturing Limited

http://www.bcdsemi.com

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