PI7C9X440SL
PCI EXPRESS TO USB 2.0 HOST CONTROLLER
DATASHEET
REVISION 3
January 2018
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<td>08h</td>
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<tr>
<td>CACHE LINE REGISTER</td>
<td>0Ch</td>
</tr>
<tr>
<td>MASTER LATENCY TIMER REGISTER</td>
<td>0Ch</td>
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<tr>
<td>HEADER TYPE REGISTER</td>
<td>0Ch</td>
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<tr>
<td>BASE ADDRESS REGISTER 0</td>
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<tr>
<td>BASE ADDRESS REGISTER 0</td>
<td>10h (Func 2 Only)</td>
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<td>SUBSYSTEM VENDOR REGISTER</td>
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<td>CAPABILITIES POINTER REGISTER</td>
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<td>INTERRUPT LINE REGISTER</td>
<td>3Ch</td>
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<td>INTERRUPT PIN REGISTER</td>
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<td>SERIAL BUS RELEASE NUMBER REGISTER</td>
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<td>FRAME LENGTH ADJUSTMENT REGISTER</td>
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<td>80h</td>
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<tr>
<td>NEXT ITEM POINTER REGISTER</td>
<td>80h</td>
</tr>
<tr>
<td>POWER MANAGEMENT CAPABILITIES REGISTER</td>
<td>80h</td>
</tr>
<tr>
<td>POWER MANAGEMENT DATA REGISTER</td>
<td>84h</td>
</tr>
<tr>
<td>PPB SUPPORT EXTENSIONS</td>
<td>84h</td>
</tr>
<tr>
<td>PM DATA REGISTER</td>
<td>84h</td>
</tr>
<tr>
<td>MESSAGE SIGNALED INTERRUPT (MSI) Capability ID Register</td>
<td>8Ch</td>
</tr>
<tr>
<td>MESSAGE SIGNALED INTERRUPT (MSI) NEXT ITEM POINTER</td>
<td>8Ch</td>
</tr>
<tr>
<td>MESSAGE CONTROL REGISTER</td>
<td>9Ch</td>
</tr>
<tr>
<td>MESSAGE ADDRESS REGISTER</td>
<td>90h</td>
</tr>
<tr>
<td>MESSAGE DATA REGISTER</td>
<td>94h</td>
</tr>
<tr>
<td>USB PHYSICAL LAYER CONTROL REGISTER (USB PORT 1)</td>
<td>A0h</td>
</tr>
<tr>
<td>USB PHYSICAL LAYER CONTROL REGISTER (USB PORT 2)</td>
<td>A4h</td>
</tr>
<tr>
<td>USB PHYSICAL LAYER CONTROL REGISTER (USB PORT 3)</td>
<td>A8h</td>
</tr>
<tr>
<td>USB PHYSICAL LAYER CONTROL REGISTER (USB PORT 4)</td>
<td>ACh</td>
</tr>
<tr>
<td>PCI EXPRESS CAPABILITY ID REGISTER</td>
<td>E0h</td>
</tr>
<tr>
<td>NEXT ITEM POINTER REGISTER</td>
<td>E0h</td>
</tr>
<tr>
<td>PCI EXPRESS CAPABILITIES REGISTER</td>
<td>E0h</td>
</tr>
<tr>
<td>DEVICE CAPABILITIES REGISTER</td>
<td>E4h</td>
</tr>
<tr>
<td>DEVICE CONTROL REGISTER</td>
<td>E8h</td>
</tr>
<tr>
<td>DEVICE STATUS REGISTER</td>
<td>E8h</td>
</tr>
<tr>
<td>LINK CAPABILITIES REGISTER</td>
<td>ECh</td>
</tr>
<tr>
<td>LINK CONTROL REGISTER</td>
<td>F0h</td>
</tr>
<tr>
<td>LINK STATUS REGISTER</td>
<td>F0h</td>
</tr>
</tbody>
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1 Features

**General Features**
- PCI Express to four USB 2.0 host controller ports
- Strapped pins configurable with optional EEPROM or SMBus
- SMBus interface support
- Low Power Dissipation at 432 mW typical in L0 normal mode
- Industrial Temperature Range -40°C to 85°C
- 128-pin LQFP 14mm x 14mm package

**Industrial Compliance**
- Compliant with PCI Express Base Specification Revision 1.1
- Compliant with PCI Express CEM Specification Revision 1.1
- Compliant with PCI-to-PCI Bridge Architecture Specification Revision 1.2
- Compliant with Advanced Configuration Power Interface (ACPI) Specification
- Compliant with Universal Serial Bus Specification Revision 2.0 (data rate 1.5/12/480 Mbps)
- Compliant with Open Host Controller Interface Specification for USB Rev 1.0a
- Compliant with Enhanced Host Controller Interface Specification for USB Rev 1.0
- Compliant with System Management (SM) Bus, Version 1.0

**PCI Express Interface**
- One x1 PCIe 1.1 port
- Advanced Power Saving
  - Link Power Management
  - Supports L0, L0s, L1, L2, L2/L3Ready and L3 link power state
  - Active state power management for L0s and L1 state
  - PME# support in L2 state
  - Device State Power Management
  - Supports D0, D3Hot and D3Cold device power state
  - 3.3V Aux Power support in D3Cold power state
- Supports up to 256-byte maximum payload size
- Programmable driver current and de-emphasis level at the PCIe port
- Reliability, Availability and Serviceability

**USB Host Controller**
- USB Root Hub with 4 downstream facing ports shared by OHCI and EHCI host controllers
- All USB downstream facing ports are able to handle high-speed (480 Mbps), full-speed (12 Mbps) and low-speed (1.5 Mbps) transactions
- PCI Express to USB bridging through PCI Express multi-functional core of PI7C9X440SL
- Two OHCI host controllers for full-speed and low-speed and one EHCI host controller for high-speed
- Programmable PHY parameters for each USB port
- Operational registers of the USB Host Controller are directly mapped to PCI memory space
2 GENERAL DESCRIPTION

The PI7C9X440SL PCI Express-to-USB 2.0 Host Controller complies with PCI Express Base Specification Revision 1.1, Open Host Controller Interface Specification Revision 1.0a, and Enhanced Host Controller Interface Specification Revision 1.0. The high-performance architecture of the PI7C9X440SL is capable of bridging from one PCIe x1 upstream port to four USB 2.0 ports. The device allows simultaneous access to multiple USB devices from system host processor, and therefore expands the connectivity domain of the system. The USB ports of the device can support all the available speeds including High-Speed (HS), Full-Speed (FS) and Low-Speed (LS). The PCIe-to-USB2.0 bridge function of the device is implemented by two types of host controllers, the Enhanced Host Controller Interface (EHCI) and Open Host Controller Interface (OHCI). There are one EHCI controller and two OHCI controllers residing in PI7C9X440SL. The EHCI controller handles High-Speed USB transaction while the OHCI controllers handle Full-Speed or Low-Speed USB transaction.

From the perspective of system model, the device contains two cascaded virtual PCI-to-PCI bridges, where the upstream-port bridge sits upon the downstream-port bridge over a virtual PCI Bus, and three USB controllers are attached to the downstream PCI Express port. During enumeration, the internal PCIe upstream and downstream ports are given unique bus numbers, device number and function number that are logically formed as a destination ID. The USB host controllers are viewed as a multi-functional device by the bootstrapping procedures. The EHCI controller is assigned function #2 and the two OHCI controllers are assigned function #0 and #1, and all the controllers are assigned the same device number. The memory-map and IO address ranges are exclusively allocated to each port and USB host controller. After the software enumeration is completed, the transaction packets are routed to the dedicated PCIe port or USB host controller based on the embedded contents of address or destination ID.

For the PCIe-to-USB bridging function, the four USB ports are first served in a host-centric manner by EHCI or OHCI host controllers, which then interface with the PCIe port to transfer packets to/from the upstream port through switch fabric. At High-Speed mode, all the USB ports are handled by ECHI controller with function #2. At Full-Speed and Low-Speed modes, USB port #1 and port #2 are handled by OHCI controller with function #0 and USB port #3 and port #4 are handled by OHCI controller with function #1. The Root Hub resides between the USB ports and host controllers and handles connection sessions from the host controller cores to USB ports.
Figure 2-1 PI7C9X440SL Topology
3 PIN DEFINITION

3.1 SIGNAL TYPES

<table>
<thead>
<tr>
<th>TYPE OF SIGNAL</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>Input</td>
</tr>
<tr>
<td>O</td>
<td>Output</td>
</tr>
<tr>
<td>P</td>
<td>Power</td>
</tr>
</tbody>
</table>

“_L” in signal name indicates Active LOW signal

3.2 PCI EXPRESS INTERFACE SIGNALS

<table>
<thead>
<tr>
<th>NAME</th>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>REFCLKP</td>
<td>51, 52</td>
<td>I</td>
<td>Reference Clock Input Pairs: Connect to external 100MHz differential clock. The input clock signals must be delivered to the clock buffer cell through an AC-coupled interface so that only the AC information of the clock is received, converted, and buffered. It is recommended that a 0.1uF be used in the AC-coupling.</td>
</tr>
<tr>
<td>REFCLKN</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PERP</td>
<td>37</td>
<td>I</td>
<td>PCI Express Data Serial Input Pair: Differential data receive signals.</td>
</tr>
<tr>
<td>PERN</td>
<td>38</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>PETP</td>
<td>41</td>
<td>O</td>
<td>PCI Express Data Serial Output Pairs: Differential data transmit signals.</td>
</tr>
<tr>
<td>PETN</td>
<td>42</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>PERST_L</td>
<td>104</td>
<td>I</td>
<td>System Reset (Active LOW): When PERST_L is asserted, the internal states of whole chip except sticky logics are initialized.</td>
</tr>
<tr>
<td>REXT</td>
<td>57</td>
<td>I</td>
<td>External Reference Resistor: Connect an external resistor (1.43K Ohm +/- 1%) to REXT_GND to provide a reference to both the bias currents and impedance calibration circuitry.</td>
</tr>
<tr>
<td>REXT_GND</td>
<td>56</td>
<td>I</td>
<td>External Reference Resistor Ground: Connect to an external resistor to REXT.</td>
</tr>
</tbody>
</table>

3.3 USB INTERFACE SIGNALS

<table>
<thead>
<tr>
<th>NAME</th>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>DP [4:1]</td>
<td>85, 93, 117, 124</td>
<td>I/O</td>
<td>USB D+ Signal: USB D+ analog signal covering HS/FS/LS. DP [x] is correspondent to Portx, where x=1,2,3,4.</td>
</tr>
<tr>
<td>DM [4:1]</td>
<td>84, 92, 116, 123</td>
<td>I/O</td>
<td>USB D- Signal: USB D- analog signal covering HS/FS/LS. DP [x] is correspondent to Portx, where x=1,2,3,4.</td>
</tr>
<tr>
<td>OCI [4:1]</td>
<td>7, 6, 5, 4</td>
<td>I</td>
<td>Over Current Input (Active LOW): These signals are asserted low to indicate that an over-current condition has occurred. OCI [x] is correspondent to Portx, where x=1,2,3,4.</td>
</tr>
<tr>
<td>POE [4:1]</td>
<td>13, 12, 11, 10</td>
<td>O</td>
<td>Power Output Enable (Active LOW): Power supply control output for USB Root Hub Port. When these signals are asserted low, they enable an external power switch to turn on the power supply. POE [x] is correspondent to Portx, where x=1,2,3,4.</td>
</tr>
<tr>
<td>RREP[4:1]</td>
<td>87, 95, 119, 126</td>
<td>I/O</td>
<td>External Resistor Connection for Current Reference: This analog signal is the connection to the external resistor. It sets the reference current. No external capacitor should be connected. The recommended value for the resistor is 6.04 kohm and accuracy of +/- 1%.</td>
</tr>
<tr>
<td>XI</td>
<td>102</td>
<td>I</td>
<td>Crystal Oscillator Input: A 12MHz crystal oscillator is required.</td>
</tr>
<tr>
<td>XO</td>
<td>103</td>
<td>O</td>
<td>Crystal Oscillator Output</td>
</tr>
<tr>
<td>PME_L</td>
<td>113</td>
<td>O</td>
<td>Power Management Event (Low Active): This signal is asserted whenever the USB power state is resumed to Operational State from Suspend State.</td>
</tr>
<tr>
<td>LEG_EMU_EN</td>
<td>20</td>
<td>O</td>
<td>OHCI Legacy Emulation Enable: This signal indicates that Legacy emulation support is enabled for the OHCI controller, and the application can read or write to I/O ports 60h/64h when I/O access for the OHCI controller is enabled. See section 5.2.1.1 for details of the Legacy Mode.</td>
</tr>
</tbody>
</table>
### 3.4 JTAG Boundary Scan Signals

<table>
<thead>
<tr>
<th>NAME</th>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCK</td>
<td>26</td>
<td>I</td>
<td>Test Clock: TCK is the test clock to synchronize the state information and data during boundary scan operation. When JTAG boundary scan function is not implemented, this pin should be left open (NC).</td>
</tr>
<tr>
<td>TMS</td>
<td>27</td>
<td>I</td>
<td>Test Mode Select: TMS controls the state of the Test Access Port (TAP) controller. When JTAG boundary scan function is not implemented, this pin should be pulled low through a 5.1K pull-down resistor.</td>
</tr>
<tr>
<td>TDO</td>
<td>25</td>
<td>O</td>
<td>Test Data Output: TDO is the test data output and connects to the end of the JTAG scan chain. When JTAG boundary scan function is not implemented, this pin should be left open (NC).</td>
</tr>
<tr>
<td>TDI</td>
<td>28</td>
<td>I</td>
<td>Test Data Input: TDI is the test data input and connects to the beginning of the JTAG scan chain. It allows the test instructions and data to be serially shifted into the Test Access Port. When JTAG boundary scan function is not implemented, this pin should be left open (NC).</td>
</tr>
<tr>
<td>TRST_L</td>
<td>29</td>
<td>I</td>
<td>Test Reset (Active LOW): TRST_L is the test reset to initialize the Test Access Port (TAP) controller. When JTAG boundary scan function is not implemented, this pin should be pulled low through a 5.1K pull-down resistor.</td>
</tr>
</tbody>
</table>
### MISCELLANEOUS SIGNALS

<table>
<thead>
<tr>
<th>NAME</th>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>EECLK</td>
<td>99</td>
<td>O</td>
<td>EEPROM Clock: Clock signal to the EEPROM interface.</td>
</tr>
<tr>
<td>EEPD</td>
<td>98</td>
<td>I/O</td>
<td>EEPROM Data: Bi-directional serial data interface to and from the EEPROM.</td>
</tr>
<tr>
<td>SMBCLK</td>
<td>21</td>
<td>I</td>
<td>SMBus Clock: System management Bus Clock.</td>
</tr>
<tr>
<td>SMBDATA</td>
<td>64</td>
<td>I/O</td>
<td>SMBus Data: Bi-Directional System Management Bus Data.</td>
</tr>
<tr>
<td>SCAN_EN</td>
<td>15</td>
<td>I/O</td>
<td>Full-Scan Enable Control: For normal operation, SCAN_EN is an output with a value of “0”. SCAN_EN becomes an input during manufacturing testing.</td>
</tr>
<tr>
<td>GPIO[7:0]</td>
<td>76, 75, 74, 73, 72, 71, 70, 69</td>
<td>I/O</td>
<td>General Purpose input and output: These eight general-purpose pins are programmed as either input-only or bi-directional pins by writing the GPIO output enable control register.</td>
</tr>
<tr>
<td>MAIN_DETECT</td>
<td>24</td>
<td>I</td>
<td>Main Power Detect: MAIN_DETECT should be tied to the Aux Power of the system through a 4.7K ohm pull-up resistor if the USB remote wakeup function is to be supported. Otherwise, this signal should be tied to the Main Power of the system through a 4.7K ohm pull-up resistor.</td>
</tr>
<tr>
<td>TEST1/3/4/5/6</td>
<td>1, 65, 77, 114, 66</td>
<td>I</td>
<td>Test Pins: For testing purposes only. TEST1 and TEST4 should be tied to ground, and TEST3, TEST5, and TEST6 should be tied to high for normal operation. The suggested value for the pull-up and pull-down resistor is 5.1K.</td>
</tr>
<tr>
<td>NC</td>
<td>2, 30, 31, 32, 43, 44, 47, 48, 55, 58, 59, 62, 63, 78, 79, 80, 88, 107, 108</td>
<td>Not Connected: These pins can be left floating.</td>
<td></td>
</tr>
</tbody>
</table>

### POWER PINS

<table>
<thead>
<tr>
<th>NAME</th>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDC</td>
<td>22, 35, 81, 100, 109, 111</td>
<td>P</td>
<td>VDDC Supply (1.0V): Used as digital core power pins.</td>
</tr>
<tr>
<td>VDDR</td>
<td>8, 33, 67, 105, 112</td>
<td>P</td>
<td>VDDR Supply (3.3V): Used as digital I/O power pins.</td>
</tr>
<tr>
<td>VDDA</td>
<td>83, 90, 91, 97, 115, 121, 122, 128</td>
<td>P</td>
<td>VDDA Supply (3.3V): Used as USB analog power pins.</td>
</tr>
<tr>
<td>AVDD</td>
<td>40, 46, 49, 60</td>
<td>P</td>
<td>AVDD Supply (1.0V): Used as PCI Express analog power pins.</td>
</tr>
<tr>
<td>AVDDH</td>
<td>54</td>
<td>P</td>
<td>AVDDH Supply (3.3V): Used as PCI Express analog high voltage power pins.</td>
</tr>
<tr>
<td>GND</td>
<td></td>
<td></td>
<td>GND: The central thermal pad underneath the package should be connected to ground.</td>
</tr>
</tbody>
</table>
## 4 PIN ASSIGNMENTS

### 4.1 PIN LIST of 128-PIN LQFP

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>PIN</th>
<th>NAME</th>
<th>PIN</th>
<th>NAME</th>
<th>PIN</th>
<th>NAME</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TEST1</td>
<td>33</td>
<td>VDDR</td>
<td>65</td>
<td>TEST3</td>
<td>97</td>
<td>VDDA</td>
</tr>
<tr>
<td>2</td>
<td>NC</td>
<td>34</td>
<td>VSS</td>
<td>66</td>
<td>TEST6</td>
<td>98</td>
<td>EEPD</td>
</tr>
<tr>
<td>3</td>
<td>IO_HIT_1</td>
<td>35</td>
<td>VDDC</td>
<td>67</td>
<td>VDDR</td>
<td>99</td>
<td>EECLK</td>
</tr>
<tr>
<td>4</td>
<td>OCI[1]</td>
<td>36</td>
<td>VSS</td>
<td>68</td>
<td>VSS</td>
<td>100</td>
<td>VDDC</td>
</tr>
<tr>
<td>5</td>
<td>OCI[2]</td>
<td>37</td>
<td>PERP</td>
<td>69</td>
<td>GPIO[0]</td>
<td>101</td>
<td>VSS</td>
</tr>
<tr>
<td>8</td>
<td>VDDR</td>
<td>40</td>
<td>AVDD</td>
<td>72</td>
<td>GPIO[3]</td>
<td>104</td>
<td>PERST_L</td>
</tr>
<tr>
<td>9</td>
<td>VSS</td>
<td>41</td>
<td>PETP</td>
<td>73</td>
<td>GPIO[4]</td>
<td>105</td>
<td>VDDR</td>
</tr>
<tr>
<td>13</td>
<td>POE[4]</td>
<td>45</td>
<td>VSS</td>
<td>77</td>
<td>TEST4</td>
<td>109</td>
<td>VDDC</td>
</tr>
<tr>
<td>14</td>
<td>SMI_O</td>
<td>46</td>
<td>AVDD</td>
<td>78</td>
<td>NC</td>
<td>110</td>
<td>VSS</td>
</tr>
<tr>
<td>15</td>
<td>SCAN_EN</td>
<td>47</td>
<td>NC</td>
<td>79</td>
<td>NC</td>
<td>111</td>
<td>VDDC</td>
</tr>
<tr>
<td>16</td>
<td>IRQ1_I</td>
<td>48</td>
<td>NC</td>
<td>80</td>
<td>NC</td>
<td>112</td>
<td>VDDR</td>
</tr>
<tr>
<td>17</td>
<td>IRQ12_I</td>
<td>49</td>
<td>AVDD</td>
<td>81</td>
<td>VDC</td>
<td>113</td>
<td>PME_L</td>
</tr>
<tr>
<td>18</td>
<td>IRQ1_O</td>
<td>50</td>
<td>VSS</td>
<td>82</td>
<td>VSS</td>
<td>114</td>
<td>TEST5</td>
</tr>
<tr>
<td>19</td>
<td>IRQ12_O</td>
<td>51</td>
<td>REFCLKP</td>
<td>83</td>
<td>VDDA</td>
<td>115</td>
<td>VDDA</td>
</tr>
<tr>
<td>22</td>
<td>VDDC</td>
<td>54</td>
<td>AVDDH</td>
<td>86</td>
<td>VSS</td>
<td>118</td>
<td>VSS</td>
</tr>
<tr>
<td>24</td>
<td>MAIN_DETECT</td>
<td>56</td>
<td>REXT_GND</td>
<td>88</td>
<td>NC</td>
<td>120</td>
<td>VSS</td>
</tr>
<tr>
<td>25</td>
<td>TDO</td>
<td>57</td>
<td>REXT</td>
<td>89</td>
<td>VSS</td>
<td>121</td>
<td>VDDA</td>
</tr>
<tr>
<td>26</td>
<td>TCK</td>
<td>58</td>
<td>NC</td>
<td>90</td>
<td>VDDA</td>
<td>122</td>
<td>VDDA</td>
</tr>
<tr>
<td>27</td>
<td>TMS</td>
<td>59</td>
<td>NC</td>
<td>91</td>
<td>VDDA</td>
<td>123</td>
<td>DM[1]</td>
</tr>
<tr>
<td>29</td>
<td>TRST_L</td>
<td>61</td>
<td>VSS</td>
<td>93</td>
<td>DP[3]</td>
<td>125</td>
<td>VSS</td>
</tr>
<tr>
<td>30</td>
<td>NC</td>
<td>62</td>
<td>NC</td>
<td>94</td>
<td>VSS</td>
<td>126</td>
<td>RREF[1]</td>
</tr>
<tr>
<td>31</td>
<td>NC</td>
<td>63</td>
<td>NC</td>
<td>95</td>
<td>RREF[3]</td>
<td>127</td>
<td>VSS</td>
</tr>
<tr>
<td>32</td>
<td>NC</td>
<td>64</td>
<td>SMBDATA</td>
<td>96</td>
<td>VSS</td>
<td>128</td>
<td>VDDA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>129</td>
<td>E_PAD</td>
</tr>
</tbody>
</table>
5 FUNCTIONAL DESCRIPTION

The PCI Express-to-USB Bridge contains two virtual PCI-to-PCI Bridges (VPPB) connected by a virtual PCI bus. One of the VPPB is implemented as the upstream port, and the other VPPB is implemented as the downstream port to connect to the USB Host Controllers (OHCI and EHCI). The upstream PCIe port encompasses complete PCIe architecture with the physical, data link, and transaction layers. One VPPB represents a single PCIe Port, which handles the transmission and reception of PCIe packets. The USB Host Controller is able to handle operational registers and descriptor link list, which provide a communication channel for Host Controller Driver (HCD) to initiate USB packet transactions to and from USB devices.

The operation of the PCIe to USB bridging functions are depicted as follows. The HCD first prepares the data structure of the USB commands or data. Then, the host controllers are notified to fetch the commands or data, which are eventually converted from PCIe into USB packet format. Depending on the direction of transfer, the host controller moves and converts the packet to/from USB devices. When the transfer is complete, an interrupt message will notify the HCD to process the data stored in the system memory the descriptor points to.

5.1 PCI EXPRESS INTERFACE FUNCTIONALITIES

5.1.1 PHYSICAL LAYER CIRCUIT

The physical layer circuit design is based on the PHY Interface for PCI Express Architecture (PIPE). It contains Physical Media Attachment (PMA) and Physical Coding Sub-layer (PCS) blocks. PMA includes Serializer/Deserializer (SERDES), PLL¹, Clock Recovery module, receiver detection circuits, beacon transmitter, electrical idle detector, and input/output buffers. PCS consists of framer, 8B/10B encoder/decoder, receiver elastic buffer, and PIPE PHY control/status circuitries. To provide the flexibility for port configuration, each lane has its own control and status signals for MAC to access individually. In addition, a pair of PRBS generator and checker is included for PHY built-in self test. The main functions of physical layer circuits include the conversion between serial-link and parallel bus, provision of clock source for the interface, resolving clock difference in receiver end, and detection of physical layer errors.

In order to meet the needs of different application, the drive amplitude, de-emphasis and equalization of each transmitting channels can be adjusted using EEPROM individually. De-emphasis of -3.5 db is implemented by the transmitters when full swing signaling is used, while an offset can be individually applied to each channel.

¹ Multiple lanes could share the PLL.
5.1.1.1 RECEIVER DETECTION

The physical layer circuits implement receiver detection, which detects the presence of an attached 50 ohm to ground termination as per PCI Express Specification. The detect circuits determine if the voltage levels of the receiver have crossed the internal threshold after a configurable time determined by the Receiver Detection Threshold field in the Physical Layer Control Register 2 (offset BCh, bit[6:4]) as listed in Table 5-1.

<table>
<thead>
<tr>
<th>Receiver Detection Threshold</th>
<th>Threshold</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>1.0 us</td>
</tr>
<tr>
<td>001</td>
<td>2.0 us</td>
</tr>
<tr>
<td>010</td>
<td>4.0 us (Recommended)</td>
</tr>
<tr>
<td>011</td>
<td>5.0 us</td>
</tr>
<tr>
<td>100</td>
<td>7.0 us</td>
</tr>
<tr>
<td>101</td>
<td>Reserved</td>
</tr>
<tr>
<td>110</td>
<td>Reserved</td>
</tr>
<tr>
<td>111</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

5.1.1.2 RECEIVER SIGNAL DETECTION

Receiver signal idling is detected with levels above a programmable threshold specified by Receiver Signal Detect field in the Physical Layer Control Register 2 (Offset BCh, bit[22:21]) as listed in Table 5-2, and can be configured on a per-port basis via EEPROM settings.

<table>
<thead>
<tr>
<th>Receiver Signal Detect</th>
<th>Min (mV ppd)</th>
<th>Max (mV ppd)</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>50</td>
<td>150</td>
</tr>
<tr>
<td>01 (Recommended)</td>
<td>65</td>
<td>175</td>
</tr>
<tr>
<td>10</td>
<td>75</td>
<td>200</td>
</tr>
<tr>
<td>11</td>
<td>120</td>
<td>240</td>
</tr>
</tbody>
</table>

5.1.1.3 RECEIVER EQUALIZATION

The receiver implements programmable equalizer via the Receiver Equalization field in the Physical Layer Control Register 2 (Offset BCh, bit[25:22]). There are 16 possible settings. It is recommended that customers determine the optimal equalization settings based on their environment to and their application.

5.1.1.4 TRANSMITTER SWING

The PCI Express transmitters support implementations of both full voltage swing and half (low) voltage swing. In full swing signaling mode, the transmitters implement de-emphasis, while in half swing mode, the transmitters do not. The Transmitter Swing field in the Physical Layer Control Register 2 (offset BCh, Bit[30]) is used for the selection of full swing signaling or half swing signaling.
Table 5-3 Transmitter Swing Settings

<table>
<thead>
<tr>
<th>Transmitter Swing</th>
<th>Mode</th>
<th>De-emphasis</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Full Voltage Swing</td>
<td>Implemented</td>
</tr>
<tr>
<td>1</td>
<td>Half Voltage Swing</td>
<td>Not implemented</td>
</tr>
</tbody>
</table>

5.1.1.5 DRIVE AMPLITUDE AND DE-EMPHASIS SETTINGS

Depending on the operation condition (voltage swing and de-emphasis condition), one of the Drive Amplitude Base Level fields in the Physical Layer Control Register 0 (offset B4h) and one of the Drive De-Emphasis Base Level fields in the Physical Layer Control Register 1 (offset B8h) are active for configuration of the amplitude and de-emphasis.

In addition, optional offset values can be added to the drive amplitude and drive de-emphasis on a per-port basis via EEPROM settings (EEPROM offset 70h, bit[3:0]). The final drive amplitude and drive de-emphasis are the summation of the base level value and the offset value. The offset value for drive amplitude is 25 mV pd, and 6.25 mV pd for drive de-emphasis.

The driver output waveform is the synthesis of amplitude and de-emphasis as shown in Figure 5-1. The driver amplitude without de-emphasis is specified as a peak differential voltage level (mVpd), and the driver de-emphasis modifies the driver amplitude.

![Figure 5-1 Driver Output Waveform](image-url)
5.1.1.6 DRIVE AMPLITUDE

Only one of the Drive Amplitude Level field in the Physical Control Register 0 (offset B4h, bit[20:16], bit[25:21] and bit[30:26]) listed in Table 5-4 is active depending on the de-emphasis and swing condition. The settings and the corresponding values of the amplitude level are listed in Table 5-5.

Table 5-4 Drive Amplitude Base Level Registers

<table>
<thead>
<tr>
<th>Active Register</th>
<th>De-Emphasis Condition</th>
<th>Swing Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drive Amplitude Level (3P5 Nom)</td>
<td>-3.5 db</td>
<td>Full</td>
</tr>
</tbody>
</table>

Table 5-5 Drive Amplitude Base Level Settings

<table>
<thead>
<tr>
<th>Setting</th>
<th>Amplitude (mV pd)</th>
<th>Setting</th>
<th>Amplitude (mV pd)</th>
<th>Setting</th>
<th>Amplitude (mV pd)</th>
</tr>
</thead>
<tbody>
<tr>
<td>00000</td>
<td>0</td>
<td>00111</td>
<td>175</td>
<td>01110</td>
<td>350</td>
</tr>
<tr>
<td>00001</td>
<td>25</td>
<td>01000</td>
<td>200</td>
<td>01111</td>
<td>375</td>
</tr>
<tr>
<td>00010</td>
<td>50</td>
<td>01001</td>
<td>225</td>
<td>10000</td>
<td>400</td>
</tr>
<tr>
<td>00011</td>
<td>75</td>
<td>01010</td>
<td>250</td>
<td>10001</td>
<td>425</td>
</tr>
<tr>
<td>00100</td>
<td>100</td>
<td>01011</td>
<td>275</td>
<td>10010</td>
<td>450</td>
</tr>
<tr>
<td>00101</td>
<td>125</td>
<td>01100</td>
<td>300</td>
<td>10011</td>
<td>475</td>
</tr>
<tr>
<td>00110</td>
<td>150</td>
<td>01101</td>
<td>325</td>
<td>Others</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

Note:
1. Nominal levels. Actual levels will vary with temperature, voltage and board effects.
2. The maximum nominal amplitude of the output driver is 475 mV pd. Combined values of driver amplitude and de-emphasis greater than 475 mV pd should be avoided.

5.1.1.7 DRIVE DE-EMPHASIS

The Drive De-Emphasis Level field in the Physical Control Register 1 (Offset B8h, bit[20:16]) listed in Table 5-6 controls the de-emphasis base level. The settings and the corresponding values of the de-emphasis level are listed in Table 5-7.

Table 5-6 Drive De-Emphasis Base Level Register

<table>
<thead>
<tr>
<th>Register</th>
<th>De-Emphasis Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drive De-Emphasis Level</td>
<td>-3.5 db</td>
</tr>
</tbody>
</table>

Table 5-7 Drive De-Emphasis Base Level Settings

<table>
<thead>
<tr>
<th>Setting</th>
<th>De-Emphasis (mV pd)</th>
<th>Setting</th>
<th>De-Emphasis (mV pd)</th>
<th>Setting</th>
<th>De-Emphasis (mV pd)</th>
</tr>
</thead>
<tbody>
<tr>
<td>00000</td>
<td>0</td>
<td>01011</td>
<td>68.75</td>
<td>10110</td>
<td>137.5</td>
</tr>
<tr>
<td>00001</td>
<td>6.25</td>
<td>01100</td>
<td>75.0</td>
<td>10111</td>
<td>143.75</td>
</tr>
<tr>
<td>00010</td>
<td>12.5</td>
<td>01101</td>
<td>81.25</td>
<td>11000</td>
<td>150.0</td>
</tr>
<tr>
<td>00011</td>
<td>18.75</td>
<td>01110</td>
<td>87.5</td>
<td>11001</td>
<td>156.25</td>
</tr>
<tr>
<td>00100</td>
<td>25.0</td>
<td>01111</td>
<td>93.75</td>
<td>11010</td>
<td>162.5</td>
</tr>
<tr>
<td>00101</td>
<td>31.25</td>
<td>10000</td>
<td>100.0</td>
<td>11011</td>
<td>168.75</td>
</tr>
<tr>
<td>00110</td>
<td>37.5</td>
<td>10001</td>
<td>106.25</td>
<td>11100</td>
<td>175.0</td>
</tr>
<tr>
<td>00111</td>
<td>43.75</td>
<td>10010</td>
<td>112.5</td>
<td>11101</td>
<td>181.25</td>
</tr>
<tr>
<td>01000</td>
<td>50.0</td>
<td>10011</td>
<td>118.75</td>
<td>11110</td>
<td>187.5</td>
</tr>
<tr>
<td>01001</td>
<td>56.25</td>
<td>10100</td>
<td>125.0</td>
<td>11111</td>
<td>194.75</td>
</tr>
<tr>
<td>01010</td>
<td>62.5</td>
<td>10101</td>
<td>131.25</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

Note:
1. Nominal levels. Actual levels will vary with temperature, voltage and board effects.
2. The maximum nominal amplitude of the output driver is 475 mV pd. Combined values of driver amplitude and de-emphasis greater than 475 mV pd should be avoided.
5.1.1.8 TRANSMITTER ELECTRICAL IDLE LATENCY

After the last character of the PCI Express transmission, the output current is reduced, and a differential voltage of less than 20 mV with common mode of VTX-CM-DC is established within 20 UI. This delay time is programmable via Transmitter PHY Latency field in the Physical Layer Control Register 2 (Offset BCh, bit[3:0]).

5.1.2 DATA LINK LAYER (DLL)

The Data Link Layer (DLL) provides a reliable data transmission between two PCI Express points. An ACK/NACK protocol is employed to guarantee the integrity of the packets delivered. Each Transaction Layer Packet (TLP) is protected by a 32-bit LCRC for error detection. The DLL receiver performs LCRC calculation to determine if the incoming packet is corrupted in the serial link. If an LCRC error is found, the DLL transmitter would issue a NACK data link layer packet (DLLP) to the opposite end to request a re-transmission, otherwise an ACK DLLP would be sent out to acknowledge on reception of a good TLP.

In the transmitter, a retry buffer is implemented to store the transmitted TLPs whose corresponding ACK/NACK DLLP have not been received yet. When an ACK is received, the TLPs with sequence number equals to and smaller than that carried in the ACK would be flushed out from the buffer. If a NACK is received or no ACK/NACK is returned from the link partner after the replay timer expires, then a replay mechanism built in DLL transmitter is triggered to re-transmit the corresponding packet that receives NACK or time-out and any other TLP transmitted after that packet.

Meanwhile, the DLL is also responsible for the initialization, updating, and monitoring of the flow-control credit. All of the flow control information is carried by DLLP to the other end of the link. Unlike TLP, DLLP is guarded by 16-bit CRC to detect if data corruption occurs.

In addition, the Media Access Control (MAC) block, which is consisted of LTSSM, multiple lanes deskew, scrambler/de-scrambler, clock correction from inserting skip order-set, and PIPE-related control/status circuits, is implemented to interface physical layer with data link layer.

5.1.3 TRANSACTION LAYER RECEIVE BLOCK (TLP DECAPSULATION)

The receiving end of the transaction layer performs header information retrieval and TC/VC mapping, and it validates the correctness of the transaction type and format. If the TLP is found to contain illegal header or the indicated packet length mismatches with the actual packet length, then a Malformed TLP is reported as an error associated with the receiving port. To ensure end-to-end data integrity, a 32-bit ECRC is checked against the TLP at the receiver if the digest bit is set in header.

5.1.4 ROUTING

The transaction layer implements three types of routing protocols: ID-based, address-based, and implicit routing. For configuration reads, configuration writes, transaction completion, and user-defined messages, the packets are routed by their destination ID constituted of bus number, device number, and function number. Address routing is employed to forward I/O or memory transactions to the destination port, which is located within the address range indicated by the address field carried in the packet header. The packet header indicates the packet types including memory read, memory write, IO read, IO write, Message Signaling Interrupt (MSI) and user-defined message. Implicit routing is mainly used to forward system message transactions such as virtual interrupt line, power management, and so on. The message type embedded in the packet header determines the routing mechanism.
If the incoming packet can not be forwarded to any other port due to a miss to hit the defined address range or targeted ID, this is considered as Unsupported Request (UR) packet, which is similar to a master abort event in PCI protocol.

5.1.5 TC/VC MAPPING

The 3-bit TC field defined in the header identifies the traffic class of the incoming packets. To enable the differential service, a TC/VC mapping table at destination port that is pre-programmed by system software or EEPROM pre-load is utilized to cast the TC labeled packets into the desired virtual channel. Note that all the traffic classes are mapped to VC0, since only VC0 is available on the interface. After the TC/VC mapping, the receive block dispatches the incoming request, completion, or data into the VC0 queues.

5.1.6 QUEUE

In PCI Express, it defines six different packet types to represent request, completion, and data. They are respectively Posted Request Header (PH), Posted Request Data payload (PD), Non-Posted Request Header (NPH), Non-Posted Data Payload (NPD), Completion Header (CPLH) and Completion Data payload (CPLD). Each packet with different type would be put into a separate queue in order to facilitate the following ordering processor. Since NPD usually contains one DW, it can be merged with the corresponding NPH into a common queue named NPHD.

5.1.6.1 PH

PH queue provides TLP header spaces for posted memory writes and various message request headers. Each header space occupies sixteen bytes to accommodate 3 DW or 4 DW headers.

5.1.6.2 PD

PD queue is used for storing posted request data. If the received TLP is of the posted request type and is determined to have payload coming with the header, the payload data would be put into PD queue.

5.1.6.3 NPHD

NPHD queue provides TLP header spaces for non-posted request packets, which include memory read, IO read, IO write, configuration read, and configuration write. Each header space takes twenty bytes to accommodate a 3-DW header, a 4-DW header, a 3-WD header with 1-DW data, and a 4-DW header with 1-DW data.

5.1.6.4 CPLH

CPLH queue provides TLP header space for completion packets. Each header space takes twelve bytes to accommodate a 3-DW header. Please note that there is no 4-DW completion headers.
5.1.6.5 CPLD

CPLD queue is used for storing completion data. If the received TLP is of the completion type and is determined to have payload coming with the header, the payload data would be put into CPLD queue.

5.1.7 TRANSACTION ORDERING

Within a VPPB, a set of ordering rules is defined to regulate the transactions on the PCI Express interface including Memory, IO, Configuration and Messages, in order to avoid deadlocks and to support the Producer-Consumer model. The ordering rules defined in table 5-4 apply within a single Traffic Class (TC). There is no ordering requirement among transactions within different TC labels.

<table>
<thead>
<tr>
<th>Table 5-8 Summary of PCI Express Ordering Rules</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Row Pass Column</strong></td>
</tr>
<tr>
<td>Posted Request</td>
</tr>
<tr>
<td>Read Request</td>
</tr>
<tr>
<td>Non-posted Write Request</td>
</tr>
<tr>
<td>Read Completion</td>
</tr>
<tr>
<td>Non-Posted Write Completion</td>
</tr>
</tbody>
</table>

1. When the Relaxed Ordering Attribute bit is cleared, the Posted Request transactions including memory write and message request must complete on the egress bus of VPPB in the order in which they are received on the ingress bus of VPPB. If the Relaxed Ordering Attribute bit is set, the Posted Request is permitted to pass over other Posted Requests occurring before it.

2. A Read Request transmitting in the same direction as a previously queued Posted Request transaction must push the posted write data ahead of it. The Posted Request transaction must complete on the egress bus before the Read Request can be attempted on the egress bus. The Read transaction can go to the same location as the Posted data. Therefore, if the Read transaction were to pass the Posted transaction, it would return stale data.

3. When the Relaxed Ordering Attribute bit is cleared, a Read completion must “pull” ahead of previously queued posted data transmitting in the same direction. In this case, the read data transmits in the same direction as the posted data, and the requestor of the read transaction is on the same side of the VPPB as the completer of the posted transaction. The posted transaction must deliver to the completer before the read data is returned to the requestor. If the Relaxed Ordering Attribute bit is set, then a read completion is permitted to pass a previously queued Memory Write or Message Request.

4. Non-Posted Write Completions are permitted to pass a previous Memory Write or Message Request transaction. Such transactions are actually transmitting in the opposite directions and hence have no ordering relationship.

5. Posted Request transactions must be given opportunities to pass Non-posted Read and Write Requests as well as Completions. Otherwise, deadlocks may occur when some older Bridges that do not support delayed transactions are mixed with PCIe interface in the same system. A fairness algorithm is used to arbitrate between the Posted Write queue and the Non-posted transaction queue.
5.1.8 FLOW CONTROL

PCI Express employs Credit-Based Flow Control mechanism to make buffer utilization more efficient. The transaction layer transmitter ensures that it does not transmit a TLP to an opposite receiver unless the receiver has enough buffer space to accept the TLP. The transaction layer receiver has the responsibility to advertise the free buffer space to an opposite transmitter to avoid packet stale. In this device, each port has separate queues for different traffic types and the credits are on the fly sent to data link layer, which compares the current available credits with the monitored one and reports the updated credit to the counterpart. If no new credit is acquired, the credit reported is scheduled for every 30 us to prevent from link entering retrain. On the other hand, the receiver at each egress port gets the usable credits from the opposite end in a link. It would broadcast them to all the other ingress ports for gating the packet transmission.

5.1.9 TRANSACTION LAYER TRANSMIT BLOCK (TLP ENCAPSULATION)

The transmit portion of transaction layer performs the following functions. They are to construct the all types of forwarded TLP generated from VC arbiter, respond with the completion packet when the local resource (i.e. configuration register) is accessed and regenerate the message that terminated at receiver to RC if acts as an upstream port.
5.2 USB HOST CONTROLLER FUNCTIONALITIES

5.2.1 OHCI HOST CONTROLLER

The OHCI Host Controller (HC) is responsible for communications between Host Controller Driver (HCD) software and USB Full Speed/Low Speed devices. The OHCI/HC and HCD exchange the information via operational registers, bulk transfer descriptors, control transfer descriptors and Host Controller Communication Area (HCCA), which are for interrupt and isochronous transfer types.

When communicating with operational registers, the OHCI/HC acts as a PCI target device to accept the commands provided by HCD and reports the status requested by HCD. The operational register contains the pointers that indicate the locations of HCCA and descriptors for bulk and control within the system memory. The HCD receives the IO Request Packet (IRP) from USB driver software and prepares the data structure of Endpoint Descriptor (ED) and Transfer Descriptor (TD) in the format of linked list in the system memory. After ED and TD are prepared, the HC is notified and acts as a PCI master to fetch the ED and TD and move data between the USB devices and memory area by following the instructions described in the descriptors.

An ED is comprised of the information including endpoint address, speed, data flow direction and maximum packet size, etc. A TD contains the information of data toggle, buffer position in system memory, complete status code and data buffer size. The EDs are linked together based on their transfer type, and each ED points to a list of TD queue that is used to transfer the data or command associated with a specific endpoint.

5.2.1.1 OHCI LEGACY SUPPORT

The OHCI host controller implements legacy support for emulation of PS/2 mouse and/or keyboard in operating systems, applications, and drivers that do not support USB functions. The emulation code translates the standard USB compliant keyboard/mouse data and transfers the data to/from PS/2 compatible legacy keyboard interface at I/O addresses 60h and 64h.

The legacy support interface is consisted of 7 hardware pins, LEG_EN, SMI_O, IO_HIT_I, IRQ_1_I, IRQ1_O, IRQ12_I and IRQ12_O, and 4 operational registers, HceControl, HceInput, HceOutput and HceStatus (offset 100h, 104h, 108h and 10Ch). When EmulationEnable bit in HceControl register is set to 1, legacy emulation is enabled. The host controller decodes accesses to I/O registers 60h and 64h, and generates IRQ1 and/or IRQ12 when appropriate.

When legacy emulation is enabled, reads and writes of the I/O register 60h and 64h are captured in HceInput, HceOutput, and HceStatus operational registers.

For details, refer to OpenHCI Specification 1.0, Appendix B.

5.2.2 EHCI HOST CONTROLLER

The EHCI Host Controller (HC) is responsible for communications between HC Driver software and USB High Speed devices. Similar to OHCI/HC, the EHCI/HC and HCD exchange the information via operational registers as well as data structure arranged in periodic schedule and asynchronous schedule traversals in the system memory.

The periodic schedule traversal is used for time-sensitive isochronous and interrupts transfer types while the asynchronous schedule traversal is for less time-sensitive control and bulk transfer types. The handling of EHCI data structure is similar to that in OHCI. However, EHCI data is more complicated due to micro-frame scheduling and split transaction support. For isochronous and interrupt transactions, the data structure contains High Speed
device isochronous transfer descriptors (iTD), Full Speed device split-transaction isochronous transfer descriptors (siTD) and queue head structure queue element descriptors (qTD) for interrupt devices. For bulk and control transactions, the HC utilizes the qTD to represent the asynchronous data transfer types for High Speed bulk and control devices.

5.2.3 PHYSICAL LAYER CIRCUIT

The USB physical layer circuit design is based on USB 2.0 Specification. The design contains PLL, bias current generator, voltage bandgap, clock and data recovery, sync detector, NRZI Encoder / Decoder, Serializer / De-Serializer, VBUS pulsing and discharge SRP circuit, and VBUS threshold comparators.

The USB physical layer parameters can be configured by setting the USB Physical Layer Control Register (Offset A0h for port 1, A4h for port 2, A8h for port 3, and ACh for port 4) and EEPROM. Each of the USB port has its own set of physical layer control parameters, and the configuration of the parameters is performed on a per-port basis.

5.2.3.1 HS DRIVER TIMING CONTROL

The timing of the HS Driver can be adjusted by changing the ratio of PMOS/NMOS strength. The PMOS Strength for HS Driver Timing and the PMOS Strength for HS Driver Timing fields (bit[0] and bit[2:1]) in the USB Physical Layer Control Register control the PMOS and NMOS strength respectively.

<table>
<thead>
<tr>
<th>PMOS Strength for HS Driver Timing</th>
<th>HS Driver Timing for PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 (default)</td>
<td>2x</td>
</tr>
<tr>
<td>1</td>
<td>8x</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>NMOS Strength for HS Driver Timing</th>
<th>HS Driver Timing for NMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>00 (default)</td>
<td>2x</td>
</tr>
<tr>
<td>01</td>
<td>4x</td>
</tr>
<tr>
<td>10</td>
<td>6x</td>
</tr>
<tr>
<td>11</td>
<td>8x</td>
</tr>
</tbody>
</table>

5.2.3.2 HS DRIVER AMPLITUDE

The amplitude of the HS driver current can be adjusted by setting the HS Driver Amplitude field (bit[4:3]) in the USB Physical Layer Control Register.

<table>
<thead>
<tr>
<th>HS Driver Amplitude</th>
<th>HS Driver Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>00 (default)</td>
<td>1</td>
</tr>
<tr>
<td>01</td>
<td>$1 + 2.5%$</td>
</tr>
<tr>
<td>10</td>
<td>$1 + 5%$</td>
</tr>
<tr>
<td>11</td>
<td>$1 + 7.5%$</td>
</tr>
</tbody>
</table>

Note: I=17.78mA
5.2.3.3 HS DRIVER SLOPE CONTROL

The rise/fall times of the HS Driver can be adjusted by setting the HS Driver Slope Control field (bit[8:5]) in the USB Physical Layer Control Register. The field controls the injection of additional charge and changes the RC constant.

Table 5-12 HS Driver Slope Control

<table>
<thead>
<tr>
<th>HS Driver Slope Control</th>
<th>Rise/Fall Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000 (default)</td>
<td>Actual values depend on boards, ambient temperatures, etc.</td>
</tr>
<tr>
<td>0001</td>
<td></td>
</tr>
<tr>
<td>0010</td>
<td></td>
</tr>
<tr>
<td>0011</td>
<td></td>
</tr>
<tr>
<td>0100</td>
<td></td>
</tr>
<tr>
<td>0101</td>
<td></td>
</tr>
<tr>
<td>0110</td>
<td></td>
</tr>
<tr>
<td>0111</td>
<td></td>
</tr>
<tr>
<td>1000</td>
<td></td>
</tr>
<tr>
<td>1001</td>
<td></td>
</tr>
<tr>
<td>1010</td>
<td></td>
</tr>
<tr>
<td>1011</td>
<td></td>
</tr>
<tr>
<td>1100</td>
<td></td>
</tr>
<tr>
<td>1101</td>
<td></td>
</tr>
<tr>
<td>1110</td>
<td></td>
</tr>
<tr>
<td>1111</td>
<td></td>
</tr>
</tbody>
</table>

5.2.3.4 REFERENCE VOLTAGE FOR DISCONNECT CIRCUIT

The reference voltage of the disconnect circuit can be adjusted by setting the Reference Voltage for Disconnect Circuit field (bit[10:9]) in the USB Physical Layer Control Register.

Table 5-13 Reference Voltage for Disconnect Circuit

<table>
<thead>
<tr>
<th>Reference Voltage for Disconnect Circuit</th>
<th>V_{\text{ref}}</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>(46 + 2) / 100 * vbg</td>
</tr>
<tr>
<td>01</td>
<td>(46 + 3) / 100 * vbg</td>
</tr>
<tr>
<td>10 (default)</td>
<td>(46 + 4) / 100 * vbg</td>
</tr>
<tr>
<td>11</td>
<td>(46 + 5) / 100 * vbg</td>
</tr>
</tbody>
</table>

5.2.3.5 REFERENCE VOLTAGE FOR SQUELCH CIRCUIT

The reference voltage of the squelch circuit can be adjusted by setting the Reference Voltage for Squelch Circuit field (bit[12:11]) in the USB Physical Layer Control Register.

Table 5-14 Reference Voltage for Squelch Circuit

<table>
<thead>
<tr>
<th>Reference Voltage for Squelch Circuit</th>
<th>Differential Reference Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>9 / 100 * vbg</td>
</tr>
<tr>
<td>01</td>
<td>(9 + 1) / 100 * vbg</td>
</tr>
<tr>
<td>10 (default)</td>
<td>(9 + 2) / 100 * vbg</td>
</tr>
<tr>
<td>11</td>
<td>(9 + 3) / 100 * vbg</td>
</tr>
</tbody>
</table>
5.2.3.6 REFERENCE VOLTAGE FOR CALIBRATION CIRCUIT

The reference voltage of the calibration circuit can be adjusted by setting the Reference Voltage for Calibration Circuit field (bit[15:13]) in the USB Physical Layer Control Register.

<table>
<thead>
<tr>
<th>Reference Voltage for Calibration Circuit</th>
<th>V_{ref575}simanm11</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>(46) / 100 * vbg</td>
</tr>
<tr>
<td>001</td>
<td>(46 + 1) / 100 * vbg</td>
</tr>
<tr>
<td>010</td>
<td>(46 + 2) / 100 * vbg</td>
</tr>
<tr>
<td>011</td>
<td>(46 + 3) / 100 * vbg</td>
</tr>
<tr>
<td>100 (default)</td>
<td>(46 + 4) / 100 * vbg</td>
</tr>
<tr>
<td>101</td>
<td>(46 + 5) / 100 * vbg</td>
</tr>
<tr>
<td>110</td>
<td>(46 + 6) / 100 * vbg</td>
</tr>
<tr>
<td>111</td>
<td>(46 + 7) / 100 * vbg</td>
</tr>
</tbody>
</table>

5.2.3.7 CHARGE PUMP CURRENT FOR PLL

The charge pump current can be adjusted by setting the Charge Pump Current for PLL field (bit[17:16]) in the USB Physical Layer Control Register.

<table>
<thead>
<tr>
<th>Charge Pump Current for PLL</th>
<th>Charge Pump Current (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>00 (default)</td>
<td>lcp</td>
</tr>
<tr>
<td>01</td>
<td>lcp * 0.5</td>
</tr>
<tr>
<td>10</td>
<td>lcp * 1.5</td>
</tr>
<tr>
<td>11</td>
<td>lcp * 2</td>
</tr>
</tbody>
</table>

Note: lcp=40uA

5.2.3.8 FS RISE/FALL TIME CONTROL

The rise/fall times for FS can be adjusted by setting the FS Rise/Fall Time Control field (bit[19:18]) in the USB Physical Layer Control Register.

<table>
<thead>
<tr>
<th>FS Rise/Fall Time Control</th>
<th>Rise/Fall Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Normal FS rise time - 30%</td>
</tr>
<tr>
<td>01 (default)</td>
<td>Normal FS rise time</td>
</tr>
<tr>
<td>10</td>
<td>Normal FS rise time</td>
</tr>
<tr>
<td>11</td>
<td>Normal FS rise time +30%</td>
</tr>
</tbody>
</table>

5.2.3.9 LS RISE/FALL TIME CONTROL

The rise/fall times for LS can be adjusted by setting the LS Rise/Fall Time Control field (bit[21:20]) in the USB Physical Layer Control Register.
Table 5-18 LS Rise/Fall Time Control

<table>
<thead>
<tr>
<th>LS Rise/Fall Time Control</th>
<th>Rise/Fall Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Normal LS rise time - 30%</td>
</tr>
<tr>
<td>01 (default)</td>
<td>Normal LS rise time</td>
</tr>
<tr>
<td>10</td>
<td>Normal LS rise time +30%</td>
</tr>
</tbody>
</table>

5.2.3.10 HS DRIVER PRE-EMPHASIS

The amplitude of the HS Driver can be adjusted by setting the HS Driver Pre-Emphasis field (bit[23:22]) in the USB Physical Layer Control Register.

Table 5-19 HS Driver Pre-Emphasis Control

<table>
<thead>
<tr>
<th>HS Driver Pre-Emphasis</th>
<th>HS Drive Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>00 (default)</td>
<td>I</td>
</tr>
<tr>
<td>01</td>
<td>I + 10%</td>
</tr>
<tr>
<td>10</td>
<td>I</td>
</tr>
<tr>
<td>11</td>
<td>I + 20%</td>
</tr>
</tbody>
</table>

Note: I=17.78mA
6  EEPROM INTERFACE AND SYSTEM MANAGEMENT BUS

The EEPROM interface consists of two pins: EECLK (EEPROM clock output) and EEPD (EEPROM bi-directional serial data). The Switch may control an ISSI IS24C04 or compatible parts using into 512x8 bits. The EEPROM is used to initialize a number of registers before enumeration. This is accomplished after PRST# is de-asserted, at which time the data from the EEPROM is loaded. The EEPROM interface is organized into a 16-bit base, and the Switch supplies a 7-bit EEPROM word address. The Switch does not control the EEPROM address input. It can only access the EEPROM with address input set to 0.

The System Management Bus interface consists of two pins: SMBCLK (System Management Bus Clock input) and SMBDATA (System Management Bus Data input/output).

6.1  EEPROM INTERFACE

6.1.1  AUTO MODE EEPROM ACCESS

The Swidge may access the EEPROM in a WORD format by utilizing the auto mode through a hardware sequencer. The EEPROM start-control, address, and read/write commands can be accessed through the configuration register. Before each access, the software should check the Autoload Status bit before issuing the next start.

6.1.2  EEPROM MODE AT RESET

During a reset, the Switch will automatically load the information/data from the EEPROM if the automatic load condition is met. The first offset in the EEPROM contains a signature. If the signature is recognized, the autoload initiates right after the reset.

During the autoload, the Bridge will read sequential words from the EEPROM and write to the appropriate registers. Before the Bridge registers can be accessed through the host, the autoload condition should be verified by reading bit [3] offset DCh (EEPROM Autoload Status). The host access is allowed only after the status of this bit is set to '0' which indicates that the autoload initialization sequence is complete.

6.1.3  EEPROM SPACE ADDRESS MAP

<table>
<thead>
<tr>
<th>15 – 8</th>
<th>7 – 0</th>
<th>BYTE OFFSET</th>
</tr>
</thead>
<tbody>
<tr>
<td>EEPROM Signature (1516h)</td>
<td>00h</td>
<td></td>
</tr>
<tr>
<td>Vendor ID for Port 0 ~ 3</td>
<td>02h</td>
<td></td>
</tr>
<tr>
<td>Device ID for Port 0 ~ 3</td>
<td>04h</td>
<td></td>
</tr>
<tr>
<td>Extended VC Count / Link Capability / Switch Mode Operation / Interrupt pin for Port 1 ~ 2</td>
<td>06h</td>
<td></td>
</tr>
<tr>
<td>Subsystem Vender ID for Port 0 ~ 3</td>
<td>08h</td>
<td></td>
</tr>
<tr>
<td>Subsystem ID for Port 0 ~ 3</td>
<td>0Ah</td>
<td></td>
</tr>
<tr>
<td>Misc Configuration for Port 0 ~ 3</td>
<td>0Ch</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>0Eh</td>
</tr>
<tr>
<td>Revision ID for Port 0 ~ 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FTS / RefClk ppm Difference / Scramble Control for Port 0</td>
<td>10h</td>
<td></td>
</tr>
<tr>
<td>FTS / RefClk ppm Difference / Scramble Control for Port 1</td>
<td>12h</td>
<td></td>
</tr>
<tr>
<td>FTS / RefClk ppm Difference / Scramble Control for Port 2</td>
<td>14h</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>16h</td>
</tr>
<tr>
<td>Physical Layer Control 0 for Port 0 ~ 2</td>
<td>18h</td>
<td></td>
</tr>
<tr>
<td>Physical Layer Control 1 for Port 0 ~ 2</td>
<td>1Ah</td>
<td></td>
</tr>
<tr>
<td>Physical Layer Control 2, Bit[6:0] for Port 0 ~ 2</td>
<td>1Ch</td>
<td></td>
</tr>
<tr>
<td>BYTE OFFSET</td>
<td>TC/VC Map for Port 0 (VC0)</td>
<td>TC/VC Map for Port 1 (VC0)</td>
</tr>
<tr>
<td>-------------</td>
<td>---------------------------</td>
<td>---------------------------</td>
</tr>
<tr>
<td>1Eh</td>
<td>Slot Clock / LPVC Count / Port Num, Port 0</td>
<td>Slot Implemented / Slot Clock / LPVC Count / Port Num, Port 1</td>
</tr>
<tr>
<td>20h</td>
<td>Vendor ID for Func 0</td>
<td>Vendor ID for Func 1</td>
</tr>
<tr>
<td>2Ah</td>
<td>Vendor ID for Func 0</td>
<td>Vendor ID for Func 1</td>
</tr>
<tr>
<td>2Ch</td>
<td>Device Control for Func 0</td>
<td>Device Control for Func 1</td>
</tr>
<tr>
<td>26h</td>
<td>Slot Capability 0 for Port 1</td>
<td>Slot Capability 0 for Port 2</td>
</tr>
<tr>
<td>30h</td>
<td>Slot Capability 0 for Port 1</td>
<td>Slot Capability 0 for Port 2</td>
</tr>
<tr>
<td>32h</td>
<td>Slot Capability 0 for Port 1</td>
<td>Slot Capability 0 for Port 2</td>
</tr>
<tr>
<td>34h</td>
<td>Slot Capability 0 for Port 1</td>
<td>Slot Capability 0 for Port 2</td>
</tr>
<tr>
<td>36h</td>
<td>Device ID for Func 0</td>
<td>Device ID for Func 1</td>
</tr>
<tr>
<td>38h</td>
<td>PM Data for Port 0</td>
<td>PM Data for Port 1</td>
</tr>
<tr>
<td>3Ah</td>
<td>PM Data for Port 0</td>
<td>PM Data for Port 1</td>
</tr>
<tr>
<td>3Ch</td>
<td>PM Data for Port 0</td>
<td>PM Data for Port 1</td>
</tr>
<tr>
<td>40h</td>
<td>PM Data for Port 0</td>
<td>PM Data for Port 1</td>
</tr>
<tr>
<td>50h</td>
<td>PM Data for Port 0</td>
<td>PM Data for Port 1</td>
</tr>
<tr>
<td>52h</td>
<td>PM Data for Port 0</td>
<td>PM Data for Port 1</td>
</tr>
<tr>
<td>54h</td>
<td>PM Data for Port 0</td>
<td>PM Data for Port 1</td>
</tr>
<tr>
<td>56h</td>
<td>PM Data for Port 0</td>
<td>PM Data for Port 1</td>
</tr>
<tr>
<td>58h</td>
<td>Class Code for Func 0</td>
<td>Class Code for Func 1</td>
</tr>
<tr>
<td>5Ah</td>
<td>Class Code for Func 0</td>
<td>Class Code for Func 1</td>
</tr>
<tr>
<td>5Ch</td>
<td>Class Code for Func 0</td>
<td>Class Code for Func 1</td>
</tr>
<tr>
<td>60h</td>
<td>USB Physical Layer Control Register (USB Port 1), Bit[15:0]</td>
<td>USB Physical Layer Control Register (USB Port 2), Bit[15:0]</td>
</tr>
<tr>
<td>62h</td>
<td>Power Budgeting Capability Register for Port 0</td>
<td>Power Budgeting Capability Register for Port 1</td>
</tr>
<tr>
<td>64h</td>
<td>Power Budgeting Capability Register for Port 0</td>
<td>Power Budgeting Capability Register for Port 1</td>
</tr>
<tr>
<td>66h</td>
<td>Power Budgeting Capability Register for Port 0</td>
<td>Power Budgeting Capability Register for Port 1</td>
</tr>
<tr>
<td>68h</td>
<td>Subsystem Vendor ID for Func 0</td>
<td>Subsystem Vendor ID for Func 1</td>
</tr>
<tr>
<td>6Ah</td>
<td>Subsystem Vendor ID for Func 0</td>
<td>Subsystem Vendor ID for Func 1</td>
</tr>
<tr>
<td>6Ch</td>
<td>Subsystem Vendor ID for Func 0</td>
<td>Subsystem Vendor ID for Func 1</td>
</tr>
<tr>
<td>70h</td>
<td>Device Control for Func 0</td>
<td>Device Control for Func 1</td>
</tr>
<tr>
<td>72h</td>
<td>Device Control for Func 0</td>
<td>Device Control for Func 1</td>
</tr>
<tr>
<td>74h</td>
<td>Device Control for Func 0</td>
<td>Device Control for Func 1</td>
</tr>
<tr>
<td>76h</td>
<td>Device Control for Func 0</td>
<td>Device Control for Func 1</td>
</tr>
<tr>
<td>78h</td>
<td>Device Control for Func 0</td>
<td>Device Control for Func 1</td>
</tr>
<tr>
<td>7Ah</td>
<td>Device Control for Func 0</td>
<td>Device Control for Func 1</td>
</tr>
<tr>
<td>7Ch</td>
<td>Device Control for Func 0</td>
<td>Device Control for Func 1</td>
</tr>
<tr>
<td>7Eh</td>
<td>Device Control for Func 0</td>
<td>Device Control for Func 1</td>
</tr>
<tr>
<td>80h</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>82h</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>84h</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>86h</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>88h</td>
<td>USB Physical Layer Control Register (USB Port 3), Bit[15:0]</td>
<td>USB Physical Layer Control Register (USB Port 3), Bit[15:0]</td>
</tr>
<tr>
<td>90h</td>
<td>PM Control Parameter / Rx Polarity for Port 0</td>
<td>PM Control Parameter / Rx Polarity for Port 0</td>
</tr>
<tr>
<td>92h</td>
<td>PM Control Parameter / Rx Polarity for Port 0</td>
<td>PM Control Parameter / Rx Polarity for Port 0</td>
</tr>
<tr>
<td>94h</td>
<td>PM Control Parameter / Rx Polarity for Port 0</td>
<td>PM Control Parameter / Rx Polarity for Port 0</td>
</tr>
<tr>
<td>96h</td>
<td>PM Capability for Func 0</td>
<td>PM Capability for Func 0</td>
</tr>
<tr>
<td>98h</td>
<td>PM Capability for Func 0</td>
<td>PM Capability for Func 0</td>
</tr>
<tr>
<td>9Ah</td>
<td>PM Capability for Func 0</td>
<td>PM Capability for Func 0</td>
</tr>
<tr>
<td>9Ch</td>
<td>PM Capability for Func 0</td>
<td>PM Capability for Func 0</td>
</tr>
<tr>
<td>9Eh</td>
<td>PM Capability for Func 0</td>
<td>PM Capability for Func 0</td>
</tr>
<tr>
<td>9Ah</td>
<td>PM Capability for Func 0</td>
<td>PM Capability for Func 0</td>
</tr>
<tr>
<td>9Ch</td>
<td>PM Capability for Func 0</td>
<td>PM Capability for Func 0</td>
</tr>
<tr>
<td>9Eh</td>
<td>PM Capability for Func 0</td>
<td>PM Capability for Func 0</td>
</tr>
<tr>
<td>9Ah</td>
<td>PM Capability for Func 0</td>
<td>PM Capability for Func 0</td>
</tr>
<tr>
<td>9Ch</td>
<td>PM Capability for Func 0</td>
<td>PM Capability for Func 0</td>
</tr>
<tr>
<td>9Eh</td>
<td>PM Capability for Func 0</td>
<td>PM Capability for Func 0</td>
</tr>
</tbody>
</table>
6.1.4 MAPPING EEPROM CONTENTS TO CONFIGURATION REGISTERS

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>PCI CFG OFFSET</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>00h ~ 01h</td>
<td>Vendor ID for Port 0~3</td>
</tr>
<tr>
<td>04h</td>
<td>02h ~ 03h</td>
<td>Device ID for Port 0~3</td>
</tr>
<tr>
<td>ADDRESS</td>
<td>PCI CFG OFFSET</td>
<td>DESCRIPTION</td>
</tr>
<tr>
<td>---------</td>
<td>---------------</td>
<td>-------------</td>
</tr>
<tr>
<td>06h</td>
<td>ECh (Port 0–2)</td>
<td>Link Capability for Port 0–2</td>
</tr>
<tr>
<td></td>
<td>ECh – Bit[14:12]</td>
<td>Bit[3:1]: It represents L0 Exit Latency for all ports</td>
</tr>
<tr>
<td></td>
<td>ECh – Bit[17:15]</td>
<td>Bit[6:4]: It represents L1 Exit Latency for all ports</td>
</tr>
<tr>
<td>B4h (Port 0–2)</td>
<td></td>
<td>Switch Mode Operation for Port 0–2</td>
</tr>
<tr>
<td>B4h – Bit[5]</td>
<td>Bit[8]: Ordering on Different Egress Port Mode</td>
<td></td>
</tr>
<tr>
<td>B4h – Bit[6]</td>
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|      | 08h – Bit[7:0] | • Bit[7:0]: Revision ID  
|      | 08h – Bit[15:8] | • Bit[15:8]: Programming Interface |
| 4Eh  | A0h (Port 0–2) | USB Physical Layer Control Register (USB Port 1), Bit[15:0]  
|      | A0h – Bit[15:0] | • Bit[15:0]: USB Physical Layer Control Register (USB Port 1), Bit[15:0] |
| 50h  | 84h (Port 0)   | No_Soft_Reset for Port 0  
|      | 84h – Bit[3]   | • Bit[0]: No_Soft_Reset.  
|      | 80h (Port 0)   | Power Management Capability for Port 0  
|      | 80h – Bit[24:22] | • Bit[3:1]: AUX Current  
|      | 80h – Bit[25]  | • Bit[4]: read only as 1 to indicate Bridge supports the D1 power management state |
|      | 80h – Bit[26]  | • Bit[5]: read only as 1 to indicate Bridge supports the D2 power management state |
|      | 80h – Bit[29:28] | • Bit[7:6]: PME Support for D2 and D1 states |
| 51h  | 84h (Port 0)   | Power Management Data for Port 0  
|      | 84h – Bit[31:24] | • Bit[15:8]: read only as Data register |
| 52h  | 84h (Port 1)   | No_Soft_Reset for Port 1  
|      | 84h – Bit[3]   | • Bit[0]: No_Soft_Reset. |
|      | 80h (Port 1)   | Power Management Capability for Port 1  
|      | 80h – Bit[24:22] | • Bit[3:1]: AUX Current |
|      | 80h – Bit[25]  | • Bit[4]: read only as 1 to indicate Bridge supports the D1 power management state  
|      | 80h – Bit[26]  | • Bit[5]: read only as 1 to indicate Bridge supports the D2 power management state  
|      | 80h – Bit[29:28] | • Bit[7:6]: PME Support for D2 and D1 states |
| 53h  | 84h (Port 1)   | Power Management Data for Port 1  
|      | 84h – Bit[31:24] | • Bit[15:8]: read only as Data register |
| 54h  | 84h (Port 2)   | No_Soft_Reset for Port 2  
|      | 84h – Bit[3]   | • Bit[0]: No_Soft_Reset.  
|      | 80h (Port 2)   | Power Management Capability for Port 2  
|      | 80h – Bit[24:22] | • Bit[3:1]: AUX Current  
|      | 80h – Bit[25]  | • Bit[4]: read only as 1 to indicate Bridge supports the D1 power management state |
|      | 80h – Bit[26]  | • Bit[5]: read only as 1 to indicate Bridge supports the D2 power management state |
|      | 80h – Bit[29:28] | • Bit[7:6]: PME Support for D2 and D1 states |
| 55h  | 84h (Port 2)   | Power Management Data for Port 2  
|      | 84h – Bit[31:24] | • Bit[15:8]: read only as Data register |
| 56h  | 84h (Port 3)   | No_Soft_Reset for Port 3  
|      | 84h – Bit[3]   | • Bit[0]: No_Soft_Reset. |
|      | 80h (Port 3)   | Power Management Capability for Port 3  
|      | 80h – Bit[24:22] | • Bit[3:1]: AUX Current  
|      | 80h – Bit[25]  | • Bit[4]: read only as 1 to indicate Bridge supports the D1 power management state  
|      | 80h – Bit[26]  | • Bit[5]: read only as 1 to indicate Bridge supports the D2 power management state  
|      | 80h – Bit[29:28] | • Bit[7:6]: PME Support for D2 and D1 states |
| 57h  | 84h (Port 3)   | Power Management Data for Port 3  
|      | 84h – Bit[31:24] | • Bit[15:8]: read only as Data register |
| 58h  | 08h (Func 0)   | Class Code for Func 0  
|      | 08h – Bit[23:16] | • Bit[7:0]: Sub-Class Code  
|      | 08h – Bit[31:24] | • Bit[15:8]: Base Class Code |
| 5Ah  | 08h (Func 1)   | Class Code for Func 1  
|      | 08h – Bit[23:16] | • Bit[7:0]: Sub-Class Code  
|      | 08h – Bit[31:24] | • Bit[15:8]: Base Class Code |
| 5Ch  | 08h (Func 2)   | Class Code for Func 2  
|      | 08h – Bit[23:16] | • Bit[7:0]: Sub-Class Code  
|      | 08h – Bit[31:24] | • Bit[15:8]: Base Class Code |
| 5Eh  | A4h (Func 0–2) | USB Physical Layer Control Register (USB Port 2), Bit[15:0]  
<p>|      | A4h – Bit[15:0] | • Bit[15:0]: USB Physical Layer Control Register (USB Port 2), Bit[15:0] |</p>
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<tr>
<td></td>
<td>80h – Bit[25]</td>
<td>• Bit[12]: D1 Power State Support</td>
</tr>
<tr>
<td></td>
<td>80h – Bit[26]</td>
<td>• Bit[13]: D2 Power State Support</td>
</tr>
<tr>
<td>9Ch</td>
<td>80h (Func 2)</td>
<td>Power Management Capability for Func 2</td>
</tr>
<tr>
<td></td>
<td>80h – Bit[15:8]</td>
<td>• Bit[7:0]: Next Item Pointer</td>
</tr>
<tr>
<td></td>
<td>80h – Bit[21]</td>
<td>• Bit[8]: Device Specific Initialization</td>
</tr>
<tr>
<td></td>
<td>80h – Bit[24:22]</td>
<td>• Bit[11:9]: AUX Current</td>
</tr>
<tr>
<td></td>
<td>80h – Bit[25]</td>
<td>• Bit[12]: D1 Power State Support</td>
</tr>
<tr>
<td></td>
<td>80h – Bit[26]</td>
<td>• Bit[13]: D2 Power State Support</td>
</tr>
<tr>
<td>ADDRESS</td>
<td>PCI CFG OFFSET</td>
<td>DESCRIPTION</td>
</tr>
<tr>
<td>---------</td>
<td>---------------</td>
<td>-------------</td>
</tr>
<tr>
<td>9Eh</td>
<td>ACh (Func 0–2)</td>
<td>USB Physical Layer Control Register (USB Port 4), Bit[15:0] - Bit[15:0]: USB Physical Layer Control Register (USB Port 4), Bit[15:0]</td>
</tr>
<tr>
<td></td>
<td>ACh – Bit[15:0]</td>
<td></td>
</tr>
<tr>
<td>A0h</td>
<td>B0h (Port 0)</td>
<td>Replay Time-out Counter for Port 0 - Bit[12:0]: Replay Time-out Counter</td>
</tr>
<tr>
<td></td>
<td>B0h – Bit[12 :0]</td>
<td></td>
</tr>
<tr>
<td>A2h</td>
<td>B0h (Port 1)</td>
<td>Replay Time-out Counter for Port 1 - Bit[12:0]: Replay Time-out Counter</td>
</tr>
<tr>
<td></td>
<td>B0h – Bit[12 :0]</td>
<td></td>
</tr>
<tr>
<td>A4h</td>
<td>B0h (Port 2)</td>
<td>Replay Time-out Counter for Port 2 - Bit[12:0]: Replay Time-out Counter</td>
</tr>
<tr>
<td></td>
<td>B0h – Bit[12 :0]</td>
<td></td>
</tr>
<tr>
<td>A8h</td>
<td>80h (Func 0)</td>
<td>Power Management Capability for Func 0 - Bit[4:0]: PME# Support</td>
</tr>
<tr>
<td></td>
<td>80h – Bit[31 :27]</td>
<td></td>
</tr>
<tr>
<td></td>
<td>84h (Func 0)</td>
<td>Power Management Data for Func 0 - Bit[5]: No_Soft_Reset</td>
</tr>
<tr>
<td></td>
<td>84h – Bit[3]</td>
<td></td>
</tr>
<tr>
<td></td>
<td>8Ch (Func 0)</td>
<td>Next Item Pointer for Func 0 - Bit[15:8]: Next Item Pointer</td>
</tr>
<tr>
<td></td>
<td>8Ch – Bit[15 :8]</td>
<td></td>
</tr>
<tr>
<td>AAh</td>
<td>80h (Func 1)</td>
<td>Power Management Capability for Func 1 - Bit[4:0]: PME# Support</td>
</tr>
<tr>
<td></td>
<td>80h – Bit[31 :27]</td>
<td></td>
</tr>
<tr>
<td></td>
<td>84h (Func 1)</td>
<td>Power Management Data for Func 1 - Bit[5]: No_Soft_Reset</td>
</tr>
<tr>
<td></td>
<td>84h – Bit[3]</td>
<td></td>
</tr>
<tr>
<td></td>
<td>8Ch (Func 1)</td>
<td>Next Item Pointer for Func 1 - Bit[15:8]: Next Item Pointer</td>
</tr>
<tr>
<td></td>
<td>8Ch – Bit[15 :8]</td>
<td></td>
</tr>
<tr>
<td>ACh</td>
<td>80h (Func 2)</td>
<td>Power Management Capability for Func 2 - Bit[4:0]: PME# Support</td>
</tr>
<tr>
<td></td>
<td>80h – Bit[31 :27]</td>
<td></td>
</tr>
<tr>
<td></td>
<td>84h (Func 2)</td>
<td>Power Management Data for Func 2 - Bit[5]: No_Soft_Reset</td>
</tr>
<tr>
<td></td>
<td>84h – Bit[3]</td>
<td></td>
</tr>
<tr>
<td></td>
<td>8Ch (Func 2)</td>
<td>Next Item Pointer for Func 2 - Bit[15:8]: Next Item Pointer</td>
</tr>
<tr>
<td></td>
<td>8Ch – Bit[15 :8]</td>
<td></td>
</tr>
<tr>
<td>AEh</td>
<td>E8h (Func 2)</td>
<td>PCI Express Capability for Func 2 - Bit[0]: Correctable Error Reporting Enable</td>
</tr>
<tr>
<td></td>
<td>E8h – Bit[0]</td>
<td></td>
</tr>
<tr>
<td></td>
<td>E8h – Bit[1]</td>
<td></td>
</tr>
<tr>
<td></td>
<td>E8h – Bit[2]</td>
<td></td>
</tr>
<tr>
<td></td>
<td>E8h – Bit[3]</td>
<td></td>
</tr>
<tr>
<td></td>
<td>E8h – Bit[7 :5]</td>
<td></td>
</tr>
<tr>
<td></td>
<td>E8h – Bit[10]</td>
<td></td>
</tr>
<tr>
<td>B0h</td>
<td>B0h (Port 0)</td>
<td>Acknowledge Latency Timer for Port 0 - Bit[14:0]: Acknowledge Latency Timer</td>
</tr>
<tr>
<td></td>
<td>B0h – Bit[30 :16]</td>
<td></td>
</tr>
<tr>
<td>B2h</td>
<td>B0h (Port 1)</td>
<td>Acknowledge Latency Timer for Port 1 - Bit[14:0]: Acknowledge Latency Timer</td>
</tr>
<tr>
<td></td>
<td>B0h – Bit[30 :16]</td>
<td></td>
</tr>
<tr>
<td>B4h</td>
<td>B0h (Port 2)</td>
<td>Acknowledge Latency Timer for Port 2 - Bit[14:0]: Acknowledge Latency Timer</td>
</tr>
<tr>
<td></td>
<td>B0h – Bit[30 :16]</td>
<td></td>
</tr>
<tr>
<td>B8h</td>
<td>E0h (Func 0)</td>
<td>PCI Express Capability for Func 0 - Bit[7:0]: Enhanced Capabilities ID</td>
</tr>
<tr>
<td></td>
<td>E0h – Bit[7 :0]</td>
<td></td>
</tr>
<tr>
<td></td>
<td>E0h – Bit[15 :8]</td>
<td></td>
</tr>
<tr>
<td>BAh</td>
<td>E0h (Func 1)</td>
<td>PCI Express Capability for Func 1 - Bit[7:0]: Enhanced Capabilities ID</td>
</tr>
<tr>
<td></td>
<td>E0h – Bit[7 :0]</td>
<td></td>
</tr>
<tr>
<td></td>
<td>E0h – Bit[15 :8]</td>
<td></td>
</tr>
<tr>
<td>BCh</td>
<td>E0h (Func 2)</td>
<td>PCI Express Capability for Func 2 - Bit[7:0]: Enhanced Capabilities ID</td>
</tr>
<tr>
<td></td>
<td>E0h – Bit[7 :0]</td>
<td></td>
</tr>
<tr>
<td></td>
<td>E0h – Bit[15 :8]</td>
<td></td>
</tr>
<tr>
<td>C0h</td>
<td>C0h – Bit[6 :0]</td>
<td>Physical Layer Control 3 for Port 0 - Bit[6:0]: Lane Mode</td>
</tr>
<tr>
<td>C8h</td>
<td>E0h (Func 0)</td>
<td>PCI Express Capability for Func 0 - Bit[3:0]: Capability Version</td>
</tr>
<tr>
<td></td>
<td>E0h – Bit[19 :16]</td>
<td></td>
</tr>
<tr>
<td></td>
<td>E0h – Bit[23 :20]</td>
<td></td>
</tr>
<tr>
<td>CAh</td>
<td>E0h (Func 1)</td>
<td>PCI Express Capability for Func 1 - Bit[3:0]: Capability Version</td>
</tr>
<tr>
<td></td>
<td>E0h – Bit[19 :16]</td>
<td></td>
</tr>
<tr>
<td></td>
<td>E0h – Bit[23 :20]</td>
<td></td>
</tr>
<tr>
<td>CCh</td>
<td>E0h (Func 2)</td>
<td>PCI Express Capability for Func 2 - Bit[3:0]: Capability Version</td>
</tr>
<tr>
<td></td>
<td>E0h – Bit[19 :16]</td>
<td></td>
</tr>
<tr>
<td></td>
<td>E0h – Bit[23 :20]</td>
<td></td>
</tr>
</tbody>
</table>
### 6.2 SMBus INTERFACE

The Swidge provides the System Management Bus (SMBus), a two-wire interface through which a simple device can communicate with the rest of the system. The SMBus interface on the Swidge is a bi-directional slave interface. It can receive data from the SMBus master or send data to the master. The interface allows full access to the configuration registers. A SMBus master, such as the processor or other SMBus devices, can read or write to every RW configuration register (read/write register). In addition, the RO and HwInt registers (read-only and hardware initialized registers) that can be auto-loaded by the EEPROM interface can also be read and written by the SMBus interface. This feature allows increases in the system expandability and flexibility in system implementation.

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>PCI CFG OFFSET</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEh</td>
<td>A0h (Func 0-2)</td>
<td>USh Physical Control Register (USB Port 1), Bit[23:16]</td>
</tr>
<tr>
<td></td>
<td>A0h – Bit[23 :16]</td>
<td>Bit[7:0]: USB Physical Control Register (USB Port 1), Bit[23:16]</td>
</tr>
<tr>
<td></td>
<td>A4h (Func 0-2)</td>
<td>USh Physical Control Register (USB Port 2), Bit[23:16]</td>
</tr>
<tr>
<td></td>
<td>A4h – Bit[23 :16]</td>
<td>Bit[15:8]: USB Physical Control Register (USB Port 1), Bit[23:16]</td>
</tr>
<tr>
<td>D8h</td>
<td>E4h (Func 0)</td>
<td>Device Capability 0 for Func 0</td>
</tr>
<tr>
<td></td>
<td>E4h – Bit[2:0]</td>
<td>Bit[2:0]: Max_Payload_Size Supported</td>
</tr>
<tr>
<td></td>
<td>E4h – Bit[15]</td>
<td>Bit[15]: Role_Base Error Reporting</td>
</tr>
<tr>
<td>DAh</td>
<td>E4h (Func 1)</td>
<td>Device Capability 0 for Func 1</td>
</tr>
<tr>
<td></td>
<td>E4h – Bit[2:0]</td>
<td>Bit[2:0]: Max_Payload_Size Supported</td>
</tr>
<tr>
<td></td>
<td>E4h – Bit[15]</td>
<td>Bit[15]: Role_Base Error Reporting</td>
</tr>
<tr>
<td>DCh</td>
<td>E4h (Func 2)</td>
<td>Device Capability 0 for Func 2</td>
</tr>
<tr>
<td></td>
<td>E4h – Bit[2:0]</td>
<td>Bit[2:0]: Max_Payload_Size Supported</td>
</tr>
<tr>
<td></td>
<td>E4h – Bit[15]</td>
<td>Bit[15]: Role_Base Error Reporting</td>
</tr>
<tr>
<td>DEh</td>
<td>A8h (Func 0-2)</td>
<td>USB Physical Control Register (USB Port 3), Bit[23:16]</td>
</tr>
<tr>
<td></td>
<td>A8h – Bit[23 :16]</td>
<td>Bit[7:0]: USB Physical Control Register (USB Port 1), Bit[23:16]</td>
</tr>
<tr>
<td></td>
<td>ACh (Func 0-2)</td>
<td>USB Physical Control Register (USB Port 4), Bit[23:16]</td>
</tr>
<tr>
<td></td>
<td>ACh – Bit[23 :16]</td>
<td>Bit[15:8]: USB Physical Control Register (USB Port 1), Bit[23:16]</td>
</tr>
<tr>
<td>E8h</td>
<td>E4h (Func 0)</td>
<td>PCI Express Capability 1 for Func 0</td>
</tr>
<tr>
<td></td>
<td>E4h – Bit[25 :18]</td>
<td>Bit[9:2]: Captured Slot Power Limit Value</td>
</tr>
<tr>
<td></td>
<td>E4h – Bit[27 :26]</td>
<td>Bit[11:10]: Captured Slot Power Limit Scale</td>
</tr>
<tr>
<td>EAh</td>
<td>E4h (Func 1)</td>
<td>PCI Express Capability 1 for Func 1</td>
</tr>
<tr>
<td></td>
<td>E4h – Bit[25 :18]</td>
<td>Bit[9:2]: Captured Slot Power Limit Value</td>
</tr>
<tr>
<td></td>
<td>E4h – Bit[27 :26]</td>
<td>Bit[11:10]: Captured Slot Power Limit Scale</td>
</tr>
<tr>
<td>ECh</td>
<td>E4h (Func 2)</td>
<td>PCI Express Capability 1 for Func 2</td>
</tr>
<tr>
<td></td>
<td>E4h – Bit[25 :18]</td>
<td>Bit[9:2]: Captured Slot Power Limit Value</td>
</tr>
<tr>
<td></td>
<td>E4h – Bit[27 :26]</td>
<td>Bit[11:10]: Captured Slot Power Limit Scale</td>
</tr>
</tbody>
</table>
The SMBus interface on the Swidge consists of one SMBus clock pin (SMBCLK), a SMBus data pin (SMBDATA), and 3 SMBus address pins (GPIO[5:7]). The SMBus clock pin provides or receives the clock signal. The SMBus data pin facilitates the data transmission and reception. Both of the clock and data pins are bi-directional. The SMBus address pins determine the address to which the Swidge responds to. The SMBus address pins generate addresses according to the following table:

**Table 6-1 SMBus Address Pin Configuration**

<table>
<thead>
<tr>
<th>BIT</th>
<th>SMBus Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>GPIO[5]</td>
</tr>
<tr>
<td>1</td>
<td>GPIO[6]</td>
</tr>
<tr>
<td>2</td>
<td>GPIO[7]</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
</tr>
</tbody>
</table>
7 REGISTER DESCRIPTION

7.1 REGISTER TYPES

<table>
<thead>
<tr>
<th>REGISTER TYPE</th>
<th>DEFINITION</th>
</tr>
</thead>
<tbody>
<tr>
<td>HwInt</td>
<td>Hardware Initialization</td>
</tr>
<tr>
<td>RO</td>
<td>Read Only</td>
</tr>
<tr>
<td>RW</td>
<td>Read / Write</td>
</tr>
<tr>
<td>RWC</td>
<td>Read / Write 1 to Clear</td>
</tr>
<tr>
<td>RWCS</td>
<td>Sticky - Read Only / Write 1 to Clear</td>
</tr>
<tr>
<td>RWS</td>
<td>Sticky - Read / Write</td>
</tr>
<tr>
<td>ROS</td>
<td>Sticky – Read Only</td>
</tr>
</tbody>
</table>

7.2 PCI EXPRESS CONFIGURATION REGISTERS

When the PCI Express port of the Swidge is set to operate at the transparent mode, it is represented by a logical PCI-to-PCI bridge that implements type 1 configuration space header. The following table details the allocation of the register fields of the PCI 2.3 compatible type 1 configuration space header.

```
<table>
<thead>
<tr>
<th>BYTE OFFSET</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>Device ID</td>
</tr>
<tr>
<td>04h</td>
<td>Vendor ID</td>
</tr>
<tr>
<td>08h</td>
<td>Revision ID</td>
</tr>
<tr>
<td>0Ch</td>
<td>Header Type</td>
</tr>
<tr>
<td>10h – 17h</td>
<td>Primary Latency Timer</td>
</tr>
<tr>
<td>18h</td>
<td>Secondary Latency Timer</td>
</tr>
<tr>
<td>1Ch</td>
<td>Class Code</td>
</tr>
<tr>
<td>1Ch</td>
<td>Command</td>
</tr>
<tr>
<td>20h</td>
<td>Secondary Status</td>
</tr>
<tr>
<td>24h – 28h</td>
<td>Subordinate Bus Number</td>
</tr>
<tr>
<td>29h</td>
<td>Secondary Bus Number</td>
</tr>
<tr>
<td>2Ah</td>
<td>Memory Limit Address</td>
</tr>
<tr>
<td>2Ch</td>
<td>Memory Base Address</td>
</tr>
<tr>
<td>2Dh</td>
<td>Prefetchable Memory Limit Address</td>
</tr>
<tr>
<td>30h</td>
<td>Prefetchable Memory Limit Address Upper 32-bit</td>
</tr>
<tr>
<td>31h</td>
<td>I/O Limit Address Upper 16-bit</td>
</tr>
<tr>
<td>34h</td>
<td>Capability Pointer to 80h</td>
</tr>
<tr>
<td>38h</td>
<td>Bridge Control</td>
</tr>
<tr>
<td>3Ch</td>
<td>Interrupt Pin</td>
</tr>
<tr>
<td>40h – 7Fh</td>
<td>Interrupt Line</td>
</tr>
<tr>
<td>80h</td>
<td>Power Management Capabilities</td>
</tr>
<tr>
<td>84h</td>
<td>PM Data</td>
</tr>
<tr>
<td>8Ch</td>
<td>Power Management Data</td>
</tr>
<tr>
<td>90h</td>
<td>Message Control</td>
</tr>
<tr>
<td>94h</td>
<td>Message Upper Address</td>
</tr>
<tr>
<td>98h</td>
<td>Message Data</td>
</tr>
<tr>
<td>9Ch</td>
<td>VPD Register</td>
</tr>
<tr>
<td>A0h</td>
<td>VPD Data Register</td>
</tr>
<tr>
<td>A4h</td>
<td>Length in Bytes (14h)</td>
</tr>
<tr>
<td>A8h</td>
<td>XPIP CSR0</td>
</tr>
<tr>
<td>ACh</td>
<td>XPIP CSR1</td>
</tr>
<tr>
<td>B0h</td>
<td>ACK Latency Timer</td>
</tr>
<tr>
<td>B4h</td>
<td>Physical Layer Control 0</td>
</tr>
<tr>
<td>B8h</td>
<td>Physical Layer Control 1</td>
</tr>
<tr>
<td>BCh</td>
<td>Physical Layer Control 2</td>
</tr>
<tr>
<td>C0h</td>
<td>Reserved</td>
</tr>
<tr>
<td>C4h</td>
<td>Next Item Pointer=8C</td>
</tr>
<tr>
<td>C8h – D7h</td>
<td>SSID/SSVID</td>
</tr>
</tbody>
</table>
```
Other than the PCI 2.3 compatible configuration space header, the Swidge also implements PCI express extended configuration space header, which includes advanced error reporting, virtual channel, and power budgeting capability registers. The following table details the allocation of the register fields of PCI express extended capability space header. The first extended capability always begins at offset 100h with a PCI Express Enhanced Capability header and the rest of capabilities are located at an offset greater than 0FFh relative to the beginning of PCI compatible configuration space.

### Extended Capability Space Header

<table>
<thead>
<tr>
<th>BYTE OFFSET</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>PCI Express Extended Capability ID=0001h</td>
</tr>
<tr>
<td>100h</td>
<td>PCI Express Extended Capability ID=0002h</td>
</tr>
<tr>
<td>104h</td>
<td>Uncorrectable Error Status Register</td>
</tr>
<tr>
<td>108h</td>
<td>Uncorrectable Error Mask Register</td>
</tr>
<tr>
<td>110h</td>
<td>Correctable Error Status Register</td>
</tr>
<tr>
<td>114h</td>
<td>Correctable Error Mask Register</td>
</tr>
<tr>
<td>118h</td>
<td>Advanced Error Capabilities and Control Register</td>
</tr>
<tr>
<td>11Ch – 128h</td>
<td>Header Log Register</td>
</tr>
<tr>
<td>12Ch – 13Fh</td>
<td>Reserved</td>
</tr>
<tr>
<td>20Ch</td>
<td>PCI Express Extended Capability ID=0004h</td>
</tr>
<tr>
<td>210h</td>
<td>Data Register</td>
</tr>
<tr>
<td>214h</td>
<td>Data Select Register</td>
</tr>
<tr>
<td>218h</td>
<td>Power Budget Capability Register</td>
</tr>
</tbody>
</table>

### Vendor ID Register – Offset 00h

<table>
<thead>
<tr>
<th>BIT</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:0</td>
<td>Vendor ID</td>
</tr>
<tr>
<td>RO</td>
<td>Identifies Pericom as the vendor of this device. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 12D8h.</td>
</tr>
</tbody>
</table>
### 7.2.2 DEVICE ID REGISTER – OFFSET 00h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>Device ID</td>
<td>RO</td>
<td>Identifies this device as the PI7C9X440. The default value may be changed by SMBus or auto-loading from EEPROM. Resets to 400Ch.</td>
</tr>
</tbody>
</table>

### 7.2.3 COMMAND REGISTER – OFFSET 04h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
</table>
| 0     | I/O Space Enable              | RW   | 0b: Ignores I/O transactions on the primary interface  
  1b: Enables responses to I/O transactions on the primary interface  
  Resets to 0b.                                                                                  |
| 1     | Memory Space Enable           | RW   | 0b: Ignores memory transactions on the primary interface  
  1b: Enables responses to memory transactions on the primary interface  
  Reset to 0b.                                                                                   |
| 2     | Bus Master Enable             | RW   | 0b: Does not initiate memory or I/O transactions on the upstream port and handles as an Unsupported Request (UR) to memory and I/O transactions on the downstream port. For Non-Posted Requests, a completion with UR completion status must be returned  
  1b: Enables the Swidge Port to forward memory and I/O Read/Write transactions in the upstream direction  
  Reset to 0b.                                                                                   |
| 3     | Special Cycle Enable          | RO   | Does not apply to PCI Express. Must be hardwired to 0b.                                                                                  |
| 4     | Memory Write And Invalidate Enable | RO | Does not apply to PCI Express. Must be hardwired to 0b.                                                                                  |
| 5     | VGA Palette Snoop Enable      | RO   | Does not apply to PCI Express. Must be hardwired to 0b.                                                                                  |
| 6     | Parity Error Response Enable  | RW   | 0b: Swidge may ignore any parity errors that it detects and continue normal operation  
  1b: Swidge must take its normal action when a parity error is detected  
  Reset to 0b.                                                                                   |
| 7     | Wait Cycle Control            | RO   | Does not apply to PCI Express. Must be hardwired to 0.                                                                                     |
| 8     | SERR# enable                  | RW   | 0b: Disables the reporting of Non-fatal and Fatal errors detected by the Swidge to the Root Complex  
  1b: Enables the Non-fatal and Fatal error reporting to Root Complex  
  Reset to 0b.                                                                                   |
| 9     | Fast Back-to-Back Enable      | RO   | Does not apply to PCI Express. Must be hardwired to 0b.                                                                                  |
| 10    | Interrupt Disable             | RW   | Controls the ability of a PCI Express device to generate INTx Interrupt Messages. In the Swidge, this bit does not affect the forwarding of INTx messages from the downstream ports.  
  Reset to 0b.                                                                                   |
| 15:11 | Reserved                      | RO   | Reset to 0b.                                                                                                                                     |

### 7.2.4 PRIMARY STATUS REGISTER – OFFSET 04h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>18:16</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 000b.</td>
</tr>
<tr>
<td>19</td>
<td>Interrupt Status</td>
<td>RO</td>
<td>Indicates that an INTx Interrupt Message is pending internally to the device. In the Swidge, the forwarding of INTx messages from the downstream device of the Swidge port is not reflected in this bit. Must be hardwired to 0b.</td>
</tr>
<tr>
<td>20</td>
<td>Capabilities List</td>
<td>RO</td>
<td>Set to 1 to enable support for the capability list (offset 34h is the pointer to the data structure).</td>
</tr>
</tbody>
</table>
## BIT FUNCTION TYPE DESCRIPTION

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>21</td>
<td>66MHz Capable</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 0b. Reset to 1b.</td>
</tr>
<tr>
<td>22</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>23</td>
<td>Fast Back-to-Back Capable</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 0b.</td>
</tr>
<tr>
<td>24</td>
<td>Master Data Parity Error</td>
<td>RWC</td>
<td>Set to 1 (by a requester) whenever a Parity error is detected or forwarded on the primary side of the port in a Swidge. If the Parity Error Response Enable bit is cleared, this bit is never set. Reset to 0b.</td>
</tr>
<tr>
<td>26:25</td>
<td>DEVSEL# timing</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 0b.</td>
</tr>
<tr>
<td>27</td>
<td>Signaled Target Abort</td>
<td>RO</td>
<td>Set to 1 (by a completer) whenever completing a request on the primary side using the Completer Abort Completion Status. Reset to 0b.</td>
</tr>
<tr>
<td>28</td>
<td>Received Target Abort</td>
<td>RO</td>
<td>Set to 1 (by a requestor) whenever receiving a Completion with Completer Abort Completion Status on the primary side. Reset to 0b.</td>
</tr>
<tr>
<td>29</td>
<td>Received Master Abort</td>
<td>RO</td>
<td>Set to 1 (by a requestor) whenever receiving a Completion with Unsupported Request Completion Status on primary side. Reset to 0b.</td>
</tr>
<tr>
<td>30</td>
<td>Signaled System Error</td>
<td>RWC</td>
<td>Set to 1 when the Swidge sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Command register is 1. Reset to 0b.</td>
</tr>
<tr>
<td>31</td>
<td>Detected Parity Error</td>
<td>RWC</td>
<td>Set to 1 whenever the primary side of the port in a Swidge receives a Poisoned TLP. Reset to 0b.</td>
</tr>
</tbody>
</table>

### 7.2.5 REVISION ID REGISTER – OFFSET 08h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Revision</td>
<td>RO</td>
<td>Indicates revision number of device. Hardwired to 00h.</td>
</tr>
</tbody>
</table>

### 7.2.6 CLASS CODE REGISTER – OFFSET 08h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:8</td>
<td>Programming Interface</td>
<td>RO</td>
<td>Read as 00h to indicate no programming interfaces have been defined for PCI-to-PCI Bridges.</td>
</tr>
<tr>
<td>23:16</td>
<td>Sub-Class Code</td>
<td>RO</td>
<td>Read as 04h to indicate device is a PCI-to-PCI Bridge.</td>
</tr>
<tr>
<td>31:24</td>
<td>Base Class Code</td>
<td>RO</td>
<td>Read as 06h to indicate device is a Bridge device.</td>
</tr>
</tbody>
</table>

### 7.2.7 CACHE LINE REGISTER – OFFSET 0Ch

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Cache Line Size</td>
<td>RW</td>
<td>The cache line size register is set by the system firmware and the operating system cache line size. This field is implemented by PCI Express devices as a RW field for legacy compatibility, but it has no impact on any PCI Express device functionality. Reset to 0b.</td>
</tr>
</tbody>
</table>
7.2.8 PRIMARY LATENCY TIMER REGISTER – OFFSET 0Ch

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:8</td>
<td>Primary Latency timer</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 00h.</td>
</tr>
</tbody>
</table>

7.2.9 HEADER TYPE REGISTER – OFFSET 0Ch

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:16</td>
<td>Header Type</td>
<td>RO</td>
<td>Read as 01h to indicate that the register layout conforms to the standard PCI-to-PCI Bridge layout.</td>
</tr>
</tbody>
</table>

7.2.10 PRIMARY BUS NUMBER REGISTER – OFFSET 18h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Primary Bus Number</td>
<td>RW</td>
<td>Indicates the number of the PCI bus to which the primary interface is connected. The value is set in software during configuration. Reset to 00h.</td>
</tr>
</tbody>
</table>

7.2.11 SECONDARY BUS NUMBER REGISTER – OFFSET 18h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:8</td>
<td>Secondary Bus Number</td>
<td>RW</td>
<td>Indicates the number of the PCI bus to which the secondary interface is connected. The value is set in software during configuration. Reset to 00h.</td>
</tr>
</tbody>
</table>

7.2.12 SUBORDINATE BUS NUMBER REGISTER – OFFSET 18h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:16</td>
<td>Subordinate Bus Number</td>
<td>RW</td>
<td>Indicates the number of the PCI bus with the highest number that is subordinate to the Bridge. The value is set in software during configuration. Reset to 00h.</td>
</tr>
</tbody>
</table>

7.2.13 SECONDARY LATENCY TIMER REGISTER – OFFSET 18h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td>Secondary Latency Timer</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 00h.</td>
</tr>
</tbody>
</table>

7.2.14 I/O BASE ADDRESS REGISTER – OFFSET 1Ch

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>3:0</td>
<td>32-bit Indicator</td>
<td>RO</td>
<td>Read as 01h to indicate 32-bit I/O addressing.</td>
</tr>
<tr>
<td>7:4</td>
<td>I/O Base Address [15:12]</td>
<td>RW</td>
<td>Defines the bottom address of the I/O address range for the Bridge to determine when to forward I/O transactions from one interface to the other. The upper 4 bits correspond to address bits [15:12] and are writable. The lower 12 bits corresponding to address bits [11:0] are assumed to be 0. The upper 16 bits corresponding to address bits [31:16] are defined in the I/O base</td>
</tr>
</tbody>
</table>
### 7.2.15 I/O LIMIT ADDRESS REGISTER – OFFSET 1Ch

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>11:8</td>
<td>32-bit Indicator</td>
<td>RO</td>
<td>Defines the top address of the I/O address range for the Bridge to determine when to forward I/O transactions from one interface to the other. The upper 4 bits correspond to address bits [15:12] and are writable. The lower 12 bits corresponding to address bits [11:0] are assumed to be FFFh. The upper 16 bits corresponding to address bits [31:16] are defined in the I/O limit address upper 16 bits address register. Reset to 0h.</td>
</tr>
<tr>
<td>15:12</td>
<td>I/O Limit Address [15:12]</td>
<td>RW</td>
<td>Reset to 0h.</td>
</tr>
</tbody>
</table>

### 7.2.16 SECONDARY STATUS REGISTER – OFFSET 1Ch

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>20:16</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 000000h.</td>
</tr>
<tr>
<td>21</td>
<td>66MHz Capable</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 0b.</td>
</tr>
<tr>
<td>22</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0h.</td>
</tr>
<tr>
<td>23</td>
<td>Fast Back-to-Back Capable</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 0b.</td>
</tr>
<tr>
<td>24</td>
<td>Master Data Parity Error</td>
<td>RWC</td>
<td>Set to 1 (by a requestor) whenever a Parity error is detected or forwarded on the secondary side of the port in a Swidge. If the Parity Error Response Enable bit is cleared, this bit is never set. Reset to 0h.</td>
</tr>
<tr>
<td>26:25</td>
<td>DEVSEL_L timing</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 0b.</td>
</tr>
<tr>
<td>27</td>
<td>Signaled Target Abort</td>
<td>RO</td>
<td>Set to 1 (by a completer) whenever completing a request in the secondary side using Completer Abort Completion Status. Reset to 0b.</td>
</tr>
<tr>
<td>28</td>
<td>Received Target Abort</td>
<td>RO</td>
<td>Set to 1 (by a requestor) whenever receiving a Completion with Completer Abort Completion Status in the secondary side. Reset to 0b.</td>
</tr>
<tr>
<td>29</td>
<td>Received Master Abort</td>
<td>RO</td>
<td>Set to 1 (by a requestor) whenever receiving a Completion with Unsupported Request Completion Status in secondary side. Reset to 0b.</td>
</tr>
<tr>
<td>30</td>
<td>Received System Error</td>
<td>RWC</td>
<td>Set to 1 when the Swidge sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Bridge Control register is 1. Reset to 0b.</td>
</tr>
<tr>
<td>31</td>
<td>Detected Parity Error</td>
<td>RWC</td>
<td>Set to 1 whenever the secondary side of the port in a Swidge receives a Poisoned TLP. Reset to 0b.</td>
</tr>
</tbody>
</table>

### 7.2.17 MEMORY BASE ADDRESS REGISTER – OFFSET 20h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>3:0</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0h.</td>
</tr>
<tr>
<td>15:4</td>
<td>Memory Base Address [15:4]</td>
<td>RW</td>
<td>Defines the bottom address of an address range for the Bridge to determine when to forward memory transactions from one interface to the other. The</td>
</tr>
</tbody>
</table>
### MEMORY LIMIT ADDRESS REGISTER – OFFSET 20h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>19:16</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0h.</td>
</tr>
<tr>
<td>31:20</td>
<td>Memory Limit Address [31:20]</td>
<td>RW</td>
<td>Defines the top address of an address range for the Bridge to determine when to forward memory transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are writable. The lower 20 bits corresponding to address bits [19:0] are assumed to be FFFFFh. Reset to 000h.</td>
</tr>
</tbody>
</table>

### PREFETCHABLE MEMORY BASE ADDRESS REGISTER – OFFSET 24h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0:3</td>
<td>64-bit addressing</td>
<td>RO</td>
<td>Read as 0001b to indicate 64-bit addressing.</td>
</tr>
<tr>
<td>15:4</td>
<td>Prefetchable Memory Base Address [31:20]</td>
<td>RW</td>
<td>Defines the bottom address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are writable. The lower 20 bits are assumed to be 0. The memory base register upper 32 bits contain the upper half of the base address. Reset to 000h.</td>
</tr>
</tbody>
</table>

### PREFETCHABLE MEMORY LIMIT ADDRESS REGISTER – OFFSET 24h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>19:16</td>
<td>64-bit addressing</td>
<td>RO</td>
<td>Read as 0001b to indicate 64-bit addressing.</td>
</tr>
<tr>
<td>31:20</td>
<td>Prefetchable Memory Limit Address [31:20]</td>
<td>RW</td>
<td>Defines the top address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are writable. The lower 20 bits are assumed to be FFFFFh. The memory limit upper 32 bits register contains the upper half of the limit address. Reset to 000h.</td>
</tr>
</tbody>
</table>

### PREFETCHABLE MEMORY BASE ADDRESS UPPER 32-BITS REGISTER – OFFSET 28h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>Prefetchable Memory Base Address, Upper 32-bits [63:32]</td>
<td>RW</td>
<td>Defines the upper 32-bits of a 64-bit bottom address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other. Reset to 00000000h.</td>
</tr>
</tbody>
</table>
### 7.2.22 PREFETCHABLE MEMORY LIMIT ADDRESS UPPER 32-BITS REGISTER – OFFSET 2Ch

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>Prefetchable Memory Limit Address, Upper 32-bits [63:32]</td>
<td>RW</td>
<td>Defines the upper 32-bits of a 64-bit top address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other. Reset to 00000000h.</td>
</tr>
</tbody>
</table>

### 7.2.23 I/O BASE ADDRESS UPPER 16-BITS REGISTER – OFFSET 30h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:0</td>
<td>I/O Base Address, Upper 16-bits [31:16]</td>
<td>RW</td>
<td>Defines the upper 16-bits of a 32-bit bottom address of an address range for the Bridge to determine when to forward I/O transactions from one interface to the other. Reset to 000h.</td>
</tr>
</tbody>
</table>

### 7.2.24 I/O LIMIT ADDRESS UPPER 16-BITS REGISTER – OFFSET 30h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>I/O Limit Address, Upper 16-bits [31:16]</td>
<td>RW</td>
<td>Defines the upper 16-bits of a 32-bit top address of an address range for the Bridge to determine when to forward I/O transactions from one interface to the other. Reset to 000h.</td>
</tr>
</tbody>
</table>

### 7.2.25 CAPABILITY POINTER REGISTER – OFFSET 34h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Capability Pointer</td>
<td>RO</td>
<td>Pointer points to the PCI power management registers (80h). Reset to 80h.</td>
</tr>
</tbody>
</table>

### 7.2.26 INTERRUPT LINE REGISTER – OFFSET 3Ch

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Interrupt Line</td>
<td>RW</td>
<td>Reset to 00h.</td>
</tr>
</tbody>
</table>

### 7.2.27 INTERRUPT PIN REGISTER – OFFSET 3Ch

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:8</td>
<td>Interrupt Pin</td>
<td>RO</td>
<td>The Swidge implements INTA virtual wire interrupt signals to represent hot-plug events at downstream ports. The default value on the downstream ports may be changed by SMBus or auto-loading from EEPROM. Reset to 00h.</td>
</tr>
</tbody>
</table>
### 7.2.28 BRIDGE CONTROL REGISTER – OFFSET 3Ch

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>Parity Error Response</td>
<td>RW</td>
<td>0b: Ignore Poisoned TLPs on the secondary interface</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1b: Enable the Poisoned TLPs reporting and detection on the secondary</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>interface</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>17</td>
<td>S_SERR# enable</td>
<td>RW</td>
<td>0b: Enables the forwarding of EER_COR, ERR_NONFATAL and ERR_FATAL from</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>secondary to primary interface</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1b: Enables the forwarding of EER_COR, ERR_NONFATAL and ERR_FATAL from</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>secondary to primary interface</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>18</td>
<td>ISA Enable</td>
<td>RW</td>
<td>0b: Forwards downstream all I/O addresses in the address range defined by</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>the I/O Base, I/O Base, and Limit registers</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1b: Forwards upstream all I/O addresses in the address range defined by</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>the I/O Base and Limit registers that are in the first 64KB of PCI I/O</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>address space (top 768 bytes of each 1KB block)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>19</td>
<td>VGA Enable</td>
<td>RW</td>
<td>0: Ignores access to the VGA memory or I/O address range</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Forwards transactions targeted at the VGA memory or I/O address range</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>VGA memory range starts from 000A 0000h to 000B FFFFh</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>VGA IO addresses are in the first 64KB of IO address space. AD [9:0] is</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>in the ranges 3B0 to 3BBh and 3C0h to 3DFh.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 0b. Please note that this bit is reserved in Port 2.</td>
</tr>
<tr>
<td>20</td>
<td>VGA 16-bit decode</td>
<td>RW</td>
<td>0b: Executes 10-bit address decoding on VGA I/O accesses</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1b: Executes 16-bit address decoding on VGA I/O accesses</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 0b. Please note that this bit is reserved in Port 2.</td>
</tr>
<tr>
<td>21</td>
<td>Master Abort Mode</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 0b.</td>
</tr>
<tr>
<td>22</td>
<td>Secondary Bus Reset</td>
<td>RW</td>
<td>0b: Does not trigger a hot reset on the corresponding PCI Express Port</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1b: Triggers a hot reset on the corresponding PCI Express Port</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>At the downstream port, it asserts PORT_RST# to the attached downstream</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>device.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>At the upstream port, it asserts the PORT_RST# at all the downstream</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>ports.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>23</td>
<td>Fast Back-to-Back</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 0b.</td>
</tr>
<tr>
<td></td>
<td>Enable</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>Primary Master</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 0b.</td>
</tr>
<tr>
<td></td>
<td>Timeout</td>
<td></td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>Secondary Master</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 0b.</td>
</tr>
<tr>
<td></td>
<td>Timeout</td>
<td></td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>Master Timeout Status</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 0b.</td>
</tr>
<tr>
<td></td>
<td>Status</td>
<td></td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>Discard Timer SERR#</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 0b.</td>
</tr>
<tr>
<td></td>
<td>enable</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31:28</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0h.</td>
</tr>
</tbody>
</table>

### 7.2.29 POWER MANAGEMENT CAPABILITY ID REGISTER – OFFSET 80h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Enhanced Capabilities ID</td>
<td>RO</td>
<td>Read as 01h to indicate that these are power management enhanced capability</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>registers.</td>
</tr>
</tbody>
</table>

**Note:**
- Enhanced Capabilities ID: 01h
- Secondary Bus Reset: 0b does not trigger a hot reset, 1b triggers it.
- Secondary Master Timeout: Does not apply to PCI Express. Must be hardwired to 0b.
- Master Timeout Status: Does not apply to PCI Express. Must be hardwired to 0b.
- Discard Timer SERR# enable: Does not apply to PCI Express. Must be hardwired to 0b.
### 7.2.30 NEXT ITEM POINTER REGISTER – OFFSET 80h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:8</td>
<td>Next Item Pointer</td>
<td>RO</td>
<td>At upstream ports, the pointer points to the Vital Protocol Data (VPD) capability register (9Ch). At downstream ports, the pointer points to the Message capability register (8Ch). Reset to 9Ch (Upstream port). Reset to 8Ch (Downstream port).</td>
</tr>
</tbody>
</table>

### 7.2.31 POWER MANAGEMENT CAPABILITIES REGISTER – OFFSET 80h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>18:16</td>
<td>Power Management Revision</td>
<td>RO</td>
<td>Read as 01b to indicate the device is compliant to Revision 1.2 of PCI Power Management Interface Specifications.</td>
</tr>
<tr>
<td>19</td>
<td>PME# Clock</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 0b.</td>
</tr>
<tr>
<td>20</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>21</td>
<td>Device Specific Initialization</td>
<td>RO</td>
<td>Read as 0b to indicate Swidge does not have device specific initialization requirements. The default value may be changed by SMBus or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>24:22</td>
<td>AUX Current</td>
<td>RO</td>
<td>Reset as 11b to indicate the Swidge needs 375 mA in D3 state. The default value may be changed by SMBus or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>25</td>
<td>D1 Power State Support</td>
<td>RO</td>
<td>Read as 1b to indicate Swidge supports the D1 power management state. The default value may be changed by SMBus or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>26</td>
<td>D2 Power State Support</td>
<td>RO</td>
<td>Read as 1b to indicate Swidge supports the D2 power management state. The default value may be changed by SMBus or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>31:27</td>
<td>PME# Support</td>
<td>RO</td>
<td>Read as 1111b to indicate Swidge supports the forwarding of PME# message in all power states. The default value may be changed by SMBus or auto-loading from EEPROM.</td>
</tr>
</tbody>
</table>

### 7.2.32 POWER MANAGEMENT DATA REGISTER – OFFSET 84h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:0</td>
<td>Power State</td>
<td>RW</td>
<td>Indicates the current power state of the Swidge. Writing a value of D0 when the previous state was D3 cause a hot reset without asserting DWRST_L. 00b: D0 state 01b: D1 state 10b: D2 state 11b: D3 hot state Reset to 00b.</td>
</tr>
<tr>
<td>2</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>3</td>
<td>No_Soft_Reset</td>
<td>RO</td>
<td>When set, this bit indicates that device transitioning from D3hot to D0 does not perform an internal reset. When clear, an internal reset is performed when power state transits from D3hot to D0. This bit can be rewritten with EEPROM programming. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 1b.</td>
</tr>
<tr>
<td>7:4</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>8</td>
<td>PME# Enable</td>
<td>RWS</td>
<td>When asserted, the Swidge will generate the PME# message. Reset to 0b.</td>
</tr>
<tr>
<td>12:9</td>
<td>Data Select</td>
<td>RW</td>
<td>Select data registers.</td>
</tr>
<tr>
<td>14:13</td>
<td>Data Scale</td>
<td>RO</td>
<td>Reset to 00b.</td>
</tr>
<tr>
<td>15</td>
<td>PME status</td>
<td>ROS</td>
<td>Read as 0b as the PME# message is not implemented.</td>
</tr>
</tbody>
</table>
7.2.33 PPB SUPPORT EXTENSIONS – OFFSET 84h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>21:16</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 000000b.</td>
</tr>
<tr>
<td>22</td>
<td>B2_B3 Support for D3HOT</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 0b.</td>
</tr>
<tr>
<td>23</td>
<td>Bus Power / Clock Control Enable</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 0b.</td>
</tr>
</tbody>
</table>

7.2.34 DATA REGISTER – OFFSET 84h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td>Data Register</td>
<td>RO</td>
<td>Data Register. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.</td>
</tr>
</tbody>
</table>

7.2.35 MSI CAPABILITY ID REGISTER – OFFSET 8Ch (Downstream Port Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Enhanced Capabilities ID</td>
<td>RO</td>
<td>Read as 05h to indicate that this is message signal interrupt capability register.</td>
</tr>
</tbody>
</table>

7.2.36 NEXT ITEM POINTER REGISTER – OFFSET 8Ch (Downstream Port Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:8</td>
<td>Next Item Pointer</td>
<td>RO</td>
<td>Pointer points to Vendor specific capability register (A4h). Reset to A4h.</td>
</tr>
</tbody>
</table>

7.2.37 MESSAGE CONTROL REGISTER – OFFSET 8Ch (Downstream Port Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>MSI Enable</td>
<td>RW</td>
<td>0b: The function is prohibited from using MSI to request service 1b: The function is permitted to use MSI to request service and is prohibited from using its INTx # pin Reset to 0b.</td>
</tr>
<tr>
<td>19:17</td>
<td>Multiple Message Capable</td>
<td>RO</td>
<td>Read as 000b.</td>
</tr>
<tr>
<td>22:20</td>
<td>Multiple Message Enable</td>
<td>RW</td>
<td>Reset to 000b.</td>
</tr>
<tr>
<td>23</td>
<td>64-bit address capable</td>
<td>RO</td>
<td>0b: The function is not capable of generating a 64-bit message address 1b: The function is capable of generating a 64-bit message address Reset to 1b.</td>
</tr>
<tr>
<td>31:24</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 00h.</td>
</tr>
</tbody>
</table>

7.2.38 MESSAGE ADDRESS REGISTER – OFFSET 90h (Downstream Port Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:0</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 00b.</td>
</tr>
</tbody>
</table>
7.2.39 MESSAGE UPPER ADDRESS REGISTER – OFFSET 94h (Downstream Port Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>Message Upper Address</td>
<td>RW</td>
<td>This register is only effective if the device supports a 64-bit message address is set. Reset to 00000000h.</td>
</tr>
</tbody>
</table>

7.2.40 MESSAGE DATA REGISTER – OFFSET 98h (Downstream Port Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:0</td>
<td>Message Data</td>
<td>RW</td>
<td>Reset to 0000h.</td>
</tr>
</tbody>
</table>

7.2.41 VPD CAPABILITY ID REGISTER – OFFSET 9Ch (Upstream Port Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Enhanced Capabilities ID</td>
<td>RO</td>
<td>Read as 03h to indicate that these are VPD enhanced capability registers. Reset to 03h.</td>
</tr>
</tbody>
</table>

7.2.42 NEXT ITEM POINTER REGISTER – OFFSET 9Ch (Upstream Port Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:8</td>
<td>Next Item Pointer</td>
<td>RO</td>
<td>Pointer points to the Vendor specific capability register (A4h). Reset to A4h.</td>
</tr>
</tbody>
</table>

7.2.43 VPD REGISTER – OFFSET 9Ch (Upstream Port Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>17:16</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 00b.</td>
</tr>
<tr>
<td>23:18</td>
<td>VPD Address</td>
<td>RW</td>
<td>Contains DWORD address that is used to generate read or write cycle to the VPD table stored in EEPROM. Reset to 0000000b.</td>
</tr>
<tr>
<td>30:24</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0000000b.</td>
</tr>
</tbody>
</table>
| 31   | VPD operation | RW   | 0b: Performs VPD read command to VPD table at the location as specified in VPD address. This bit is kept ‘0’ and then set to ‘1’ automatically after EEPROM cycle is finished.  
1b: Performs VPD write command to VPD table at the location as specified in VPD address. This bit is kept ‘1’ and then set to ‘0’ automatically after EEPROM cycle is finished. Reset to 0b. |
7.2.44 VPD DATA REGISTER – OFFSET A0h (Upstream Port Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
</table>
| 31:0  | VPD Data       | RW   | When read, it returns the last data read from VPD table at the location as specified in VPD Address.  
When written, it places the current data into VPD table at the location as specified in VPD Address. |

7.2.45 VENDOR SPECIFIC CAPABILITY ID REGISTER – OFFSET A4h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
</table>
| 7:0   | Enhanced Capabilities ID | RO   | Read as 09h to indicate that these are vendor specific capability registers.  
Reset to 09h.                              |

7.2.46 NEXT ITEM POINTER REGISTER – OFFSET A4h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
</table>
| 15:8  | Next Item Pointer | RO   | Pointer points to the SSID/SSVID capability register (C0h).    
Reset to C4h.                                      |

7.2.47 LENGTH REGISTER – OFFSET A4h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
</table>
| 31:16 | Length Information   | RO   | The length field provides the information for number of bytes in the capability structure (including the ID and Next pointer bytes).  
Reset to 000Ch.                             |

7.2.48 XPIP CSR0 – OFFSET A8h (Test Purpose Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>Reserved</td>
<td>RW</td>
<td>Reset to 04001060h.</td>
</tr>
</tbody>
</table>

7.2.49 XPIP CSR1 – OFFSET ACh (Test Purpose Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>Reserved</td>
<td>RW</td>
<td>Reset to 04000800h.</td>
</tr>
</tbody>
</table>

7.2.50 REPLAY TIME-OUT COUNTER – OFFSET B0h (Upstream Port)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
</table>
| 11:0  | User Replay Timer | RW   | A 12-bit register contains a user-defined value. The default value may be changed by SMBus or auto-loading from EEPROM.  
Reset to 000h.                             |
## 7.2.51 ACKNOWLEDGE LATENCY TIMER – OFFSET B0h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>Enable User Replay Timer</td>
<td>RW</td>
<td>When asserted, the user-defined replay time-out value is be employed. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.</td>
</tr>
<tr>
<td>13</td>
<td>Power Management Capability</td>
<td>RO</td>
<td>The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.</td>
</tr>
<tr>
<td>14</td>
<td>MSI Capability</td>
<td>RO</td>
<td>The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.</td>
</tr>
<tr>
<td>15</td>
<td>AER Capability</td>
<td>RO</td>
<td>The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.</td>
</tr>
</tbody>
</table>

### 7.2.52 SWITCH OPERATION MODE – OFFSET B4h (Upstream Port)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Store-Forward</td>
<td>RW</td>
<td>When set, a store-forward mode is used. Otherwise, the chip is working under cut-through mode. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.</td>
</tr>
<tr>
<td>2:1</td>
<td>Cut-through Threshold</td>
<td>RW</td>
<td>Cut-through Threshold. When forwarding a packet from low-speed port to high-speed mode, the chip provides the capability to adjust the forwarding threshold. The default value may be changed by SMBus or auto-loading from EEPROM. 00b: the threshold is set at the middle of forwarding packet 01b: the threshold is set ahead 1-cycle of middle point 10b: the threshold is set ahead 2-cycle of middle point. 11b: the threshold is set ahead 3-cycle of middle point. Reset to 01b.</td>
</tr>
<tr>
<td>3</td>
<td>Port Arbitration Mode</td>
<td>RW</td>
<td>When set, the round-robin arbitration will stay in the arbitrated port even if the credit is not enough but request is pending. When clear, the round-robin arbitration will always go to the requesting port, which the outgoing credit is enough for the packet queued in the port. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.</td>
</tr>
</tbody>
</table>
### BIT FUNCTION TYPE DESCRIPTION

<table>
<thead>
<tr>
<th>4</th>
<th>Credit Update Mode</th>
<th>RW</th>
<th>When set, the frequency of releasing new credit to the link partner will be one credit per update. When clear, the frequency of releasing new credit to the link partner will be two credits per update. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>Ordering on Different Egress Port Mode</td>
<td>RW</td>
<td>When set, there has ordering rule on packets for different egress port. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.</td>
</tr>
<tr>
<td>6</td>
<td>Ordering on Different Tag of Completion Mode</td>
<td>RW</td>
<td>When set, there has ordering rule between completion packet with different tag. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.</td>
</tr>
<tr>
<td>7</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0.</td>
</tr>
<tr>
<td>13:8</td>
<td>Power management Control Parameter</td>
<td>RW</td>
<td>The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 000001b.</td>
</tr>
<tr>
<td>14</td>
<td>RX Polarity Inversion Disable</td>
<td>RO</td>
<td>The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.</td>
</tr>
<tr>
<td>15</td>
<td>Compliance Pattern Parity Control Disable</td>
<td>RO</td>
<td>The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.</td>
</tr>
</tbody>
</table>

### 7.2.53 PHYSICAL LAYER CONTROL 0 – OFFSET B4h (Upstream Port)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>20:16</td>
<td>Drive Amplitude Level (3P5 Nom)</td>
<td>RO</td>
<td>Low Driver Current (LODRV). The default value may be changed by SMBus. Reset to 10111b.</td>
</tr>
<tr>
<td>25:21</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 01101b.</td>
</tr>
<tr>
<td>30:26</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 01000b.</td>
</tr>
</tbody>
</table>

### 7.2.54 SWITCH OPERATION MODE – OFFSET B4h (Downstream Port)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0.</td>
</tr>
<tr>
<td>13:8</td>
<td>Power Management Control Parameter</td>
<td>RW</td>
<td>The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 000001b.</td>
</tr>
<tr>
<td>14</td>
<td>RX Polarity Inversion Disable</td>
<td>RW</td>
<td>The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.</td>
</tr>
<tr>
<td>15</td>
<td>Compliance Pattern Parity Control Disable</td>
<td>RW</td>
<td>The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.</td>
</tr>
</tbody>
</table>
### 7.2.55 PHYSICAL LAYER CONTROL 0 – OFFSET B4h (Downstream Port)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>20:16</td>
<td>Drive Amplitude Level (3P5 Nom)</td>
<td>RO</td>
<td>It indicates the status of the strapping pin LODRV. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 10111b.</td>
</tr>
<tr>
<td>25:21</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 01101b.</td>
</tr>
<tr>
<td>30:26</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 01000b.</td>
</tr>
</tbody>
</table>

### 7.2.56 XPIP CSR2 / TL CSR – OFFSET B8h (Test Purpose Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>FTS Number</td>
<td>RO</td>
<td>Reset to 30h.</td>
</tr>
<tr>
<td>9:8</td>
<td>Scramble control</td>
<td>RO</td>
<td>Reset to 00b.</td>
</tr>
<tr>
<td>10</td>
<td>Both L0s</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>11</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>15:12</td>
<td>TL CSR</td>
<td>RO</td>
<td>Reset to 0100b.</td>
</tr>
</tbody>
</table>

### 7.2.57 PHYSICAL LAYER CONTROL 1 – OFFSET B8h (Test Purpose Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>20:16</td>
<td>Drive De-Emphasis Level</td>
<td>RO</td>
<td>Reset to 10010b.</td>
</tr>
<tr>
<td>25:21</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 01110b.</td>
</tr>
<tr>
<td>30:26</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 10100b.</td>
</tr>
</tbody>
</table>

### 7.2.58 PHYSICAL LAYER CONTROL 2 – OFFSET BCh

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>3:0</td>
<td>Transmitter PHY Latency</td>
<td>RO</td>
<td>Reset to 0111b.</td>
</tr>
<tr>
<td>6:4</td>
<td>Receiver Detection Threshold</td>
<td>RO</td>
<td>Reset to 010b.</td>
</tr>
<tr>
<td>7</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>8</td>
<td>CDR Loop Bandwidth Enable</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>10:9</td>
<td>CDR Threshold</td>
<td>RO</td>
<td>Reset to 11b.</td>
</tr>
<tr>
<td>12:11</td>
<td>CDR Loop Bandwidth Gain</td>
<td>RO</td>
<td>Reset to 11b.</td>
</tr>
<tr>
<td>15:13</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>16</td>
<td>Per-Lane Main Drive Offset Enable (Margining)</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>17</td>
<td>Per-Lane Main Drive Offset Enable (Nominal)</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>18</td>
<td>Per-Lane De-Emphasis Drive Offset Enable (Margining)</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>19</td>
<td>Per-Lane De-Emphasis Drive Offset Enable (Nominal)</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>21:20</td>
<td>Receiver Signal Detection</td>
<td>RO</td>
<td>Reset to 01b.</td>
</tr>
<tr>
<td>BIT</td>
<td>FUNCTION</td>
<td>TYPE</td>
<td>DESCRIPTION</td>
</tr>
<tr>
<td>-----</td>
<td>----------------</td>
<td>------</td>
<td>------------------------------------</td>
</tr>
<tr>
<td>25:22</td>
<td>Receiver Equalization</td>
<td>RO</td>
<td>Reset to 0011b.</td>
</tr>
<tr>
<td>29:26</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0110b.</td>
</tr>
<tr>
<td>30</td>
<td>Transmitter Swing</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>31</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
</tbody>
</table>

**7.2.59 PHYSICAL LAYER CONTROL 3 REGISTER – OFFSET C0h**

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>6:0</td>
<td>Lane Mode</td>
<td>RW</td>
<td>Reset to 0</td>
</tr>
<tr>
<td>31:7</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0</td>
</tr>
</tbody>
</table>

**7.2.60 SSID/SSVID CAPABILITY ID REGISTER – OFFSET C4h**

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>SSID/SSVID Capabilities ID</td>
<td>RO</td>
<td>Read as 0Dh to indicate that these are SSID/SSVID capability registers.</td>
</tr>
</tbody>
</table>

**7.2.61 NEXT ITEM POINTER REGISTER – OFFSET C4h**

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:8</td>
<td>Next Item Pointer</td>
<td>RO</td>
<td>Pointer points to the PCI Express capability register (E0h).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to E0h.</td>
</tr>
</tbody>
</table>

**7.2.62 SUBSYSTEM VENDOR ID REGISTER – OFFSET C8h**

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:0</td>
<td>SSVID</td>
<td>RO</td>
<td>It indicates the sub-system vendor id. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0000h.</td>
</tr>
</tbody>
</table>

**7.2.63 SUBSYSTEM ID REGISTER – OFFSET C8h**

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>SSID</td>
<td>RO</td>
<td>It indicates the sub-system device id. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0000h.</td>
</tr>
</tbody>
</table>

**7.2.64 GPIO CONTROL REGISTER – OFFSET D8h (Upstream Port Only)**

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>GPIO [0] Input</td>
<td>RO</td>
<td>State of GPIO [0] pin</td>
</tr>
<tr>
<td>1</td>
<td>GPIO [0] Output Enable</td>
<td>RW</td>
<td>0b: GPIO [0] is an input pin</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1b: GPIO [0] is an output pin</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>BIT</td>
<td>FUNCTION</td>
<td>TYPE</td>
<td>DESCRIPTION</td>
</tr>
<tr>
<td>-----</td>
<td>--------------------------</td>
<td>------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>2</td>
<td>GPIO [0] Output Register</td>
<td>RW</td>
<td>Value of this bit will be output to GPIO [0] pin if GPIO [0] is configured as an output pin. Reset to 0b.</td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>6</td>
<td>GPIO [1] Output Register</td>
<td>RW</td>
<td>Value of this bit will be output to GPIO [1] pin if GPIO [1] is configured as an output pin. Reset to 0b.</td>
</tr>
<tr>
<td>7</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>11</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>15</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>19</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>23</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>27</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
</tbody>
</table>
### 7.2.65 EEPROM CONTROL REGISTER – OFFSET DCh (Upstream Port Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
</table>
Reset to 0b. |
Reset to 0b. |
| 31  | Reserved | RO   | Reset to 0b. |

### 7.2.66 EEPROM ADDRESS REGISTER – OFFSET DCh (Upstream Port Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
</tbody>
</table>
| 15:9| EEPROM Address | RW   | Contains the EEPROM address.  
Reset to 0b. |
### 7.2.67 EEPROM DATA REGISTER – OFFSET DCh (Upstream Port Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>EEPROM Data</td>
<td>RW</td>
<td>Contains the data to be written to the EEPROM. After completion of a read cycle, this register will contain the data from the EEPROM. Reset to 0000h.</td>
</tr>
</tbody>
</table>

### 7.2.68 PCI EXPRESS CAPABILITY ID REGISTER – OFFSET E0h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Enhanced Capabilities ID</td>
<td>RO</td>
<td>Read as 10h to indicate that these are PCI express enhanced capability registers.</td>
</tr>
</tbody>
</table>

### 7.2.69 NEXT ITEM POINTER REGISTER – OFFSET E0h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:8</td>
<td>Next Item Pointer</td>
<td>RO</td>
<td>Read as 00h. No other ECP registers.</td>
</tr>
</tbody>
</table>

### 7.2.70 PCI EXPRESS CAPABILITIES REGISTER – OFFSET E0h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>19:16</td>
<td>Capability Version</td>
<td>RO</td>
<td>Read as 0001b to indicate the device is compliant to the PCI Express Base Specifications.</td>
</tr>
<tr>
<td>23:20</td>
<td>Device/Port Type</td>
<td>RO</td>
<td>Indicates the type of PCI Express logical device. Reset to 0101b (Upstream port). Reset to 0110b (Downstream port).</td>
</tr>
<tr>
<td>24</td>
<td>Slot Implemented</td>
<td>HwIn</td>
<td>When set, indicates that the PCIe Link associated with this Port is connected to a slot. This field is valid for downstream port of the Swidge. The default value may be changed by the status of strapped pin, SMBUs, or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>29:25</td>
<td>Interrupt Message Number</td>
<td>RO</td>
<td>Read as 0b. No MSI messages are generated in the transparent mode.</td>
</tr>
<tr>
<td>31:30</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 00b.</td>
</tr>
</tbody>
</table>

### 7.2.71 DEVICE CAPABILITIES REGISTER – OFFSET E4h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>2:0</td>
<td>Max_Payload_Size Supported</td>
<td>RO</td>
<td>Indicates the maximum payload size that the device can support for TLPs. Each port of the Swidge supports 256 bytes max payload size. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 001b.</td>
</tr>
<tr>
<td>4:3</td>
<td>Phantom Functions Supported</td>
<td>RO</td>
<td>Indicates the support for use of unclaimed function numbers as Phantom functions. Read as 00b, since the Swidge does not act as a requester. Reset to 00b.</td>
</tr>
<tr>
<td>5</td>
<td>Extended Tag Field Supported</td>
<td>RO</td>
<td>Indicates the maximum supported size of Tag field as a Requester. Read as 0, since the Swidge does not act as a requester. Reset to 0b.</td>
</tr>
</tbody>
</table>
### BIT FUNCTION

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>8:6</td>
<td>Endpoint L0s Acceptable Latency</td>
<td>RO</td>
<td>Acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state. For Swidge, the ASPM software would not check this value. Reset to 000b.</td>
</tr>
<tr>
<td>11:9</td>
<td>Endpoint L1 Acceptable Latency</td>
<td>RO</td>
<td>Acceptable total latency that an Endpoint can withstand due to the transition from L1 state to the L0 state. For Swidge, the ASPM software would not check this value. Reset to 000b.</td>
</tr>
<tr>
<td>14:12</td>
<td>Reserved</td>
<td>RO</td>
<td>When set, indicates that the device implements the functionality originally defined in the Error Reporting ECN. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 1b.</td>
</tr>
<tr>
<td>15</td>
<td>Role-Based Error Reporting</td>
<td>RO</td>
<td>It applies to Upstream Port only. In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. This value is set by the Set_Slot_Power_Limit message or hardwired to 00h. Reset to 00h.</td>
</tr>
<tr>
<td>25:18</td>
<td>Captured Slot Power Limit Value</td>
<td>RO</td>
<td>It applies to Upstream Port only. Specifies the scale used for the Slot Power Limit Value. This value is set by the Set_Slot_Power_Limit message or hardwired to 00b. Reset to 00b.</td>
</tr>
<tr>
<td>27:26</td>
<td>Captured Slot Power Limit Scale</td>
<td>RO</td>
<td>This field sets maximum TLP payload size for the device. Permissible values that can be programmed are indicated by the Max_Payload_Size Supported in the Device Capabilities register. Any value exceeding the Max_Payload_Size Supported written to this register results into clamping to the Max_Payload_Size Supported value. Reset to 000b.</td>
</tr>
</tbody>
</table>

#### 7.2.72 DEVICE CONTROL REGISTER – OFFSET E8h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Correctable Error Reporting Enable</td>
<td>RW</td>
<td>0b: Disable Correctable Error Reporting 1b: Enable Correctable Error Reporting Reset to 0b.</td>
</tr>
<tr>
<td>1</td>
<td>Non-Fatal Error Reporting Enable</td>
<td>RW</td>
<td>0b: Disable Non-Fatal Error Reporting 1b: Enable Non-Fatal Error Reporting Reset to 0b.</td>
</tr>
<tr>
<td>2</td>
<td>Fatal Error Reporting Enable</td>
<td>RW</td>
<td>0b: Disable Fatal Error Reporting 1b: Enable Fatal Error Reporting Reset to 0b.</td>
</tr>
<tr>
<td>3</td>
<td>Unsupported Request Reporting Enable</td>
<td>RW</td>
<td>0b: Disable Unsupported Request Reporting 1b: Enable Unsupported Request Reporting Reset to 0b.</td>
</tr>
<tr>
<td>4</td>
<td>Enable Relaxed Ordering</td>
<td>RO</td>
<td>When set, it permits the device to set the Relaxed Ordering bit in the attribute field of transaction. Since the Swidge can not either act as a requester or alter the content of packet it forwards, this bit always returns ‘0’ when read. Reset to 0b.</td>
</tr>
<tr>
<td>7:5</td>
<td>Max_Payload_Size</td>
<td>RW</td>
<td>This field sets maximum TLP payload size for the device. Permissible values that can be programmed are indicated by the Max_Payload_Size Supported in the Device Capabilities register. Any value exceeding the Max_Payload_Size Supported written to this register results into clamping to the Max_Payload_Size Supported value. Reset to 000b.</td>
</tr>
</tbody>
</table>
### DEVICE STATUS REGISTER – OFFSET E8h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>Correctable Error Detected</td>
<td>RW1C</td>
<td>Asserted when correctable error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.</td>
</tr>
<tr>
<td>17</td>
<td>Non-Fatal Error Detected</td>
<td>RW1C</td>
<td>Asserted when non-fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.</td>
</tr>
<tr>
<td>18</td>
<td>Fatal Error Detected</td>
<td>RW1C</td>
<td>Asserted when fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.</td>
</tr>
<tr>
<td>19</td>
<td>Unsupported Request Detected</td>
<td>RW1C</td>
<td>Asserted when unsupported request is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.</td>
</tr>
<tr>
<td>20</td>
<td>AUX Power Detected</td>
<td>RO</td>
<td>Asserted when the AUX power is detected by the Swidge. Reset to 1b.</td>
</tr>
<tr>
<td>21</td>
<td>Transactions Pending</td>
<td>RO</td>
<td>Each port of Swidge does not issue Non-posted Requests on its own behalf, so this bit is hardwired to 0b. Reset to 0b.</td>
</tr>
<tr>
<td>31:22</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0.</td>
</tr>
</tbody>
</table>

### LINK CAPABILITIES REGISTER – OFFSET EC

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>3:0</td>
<td>Maximum Link Speed</td>
<td>RO</td>
<td>Read as 0001b to indicate the maximum speed of the Express link is 2.5 Gb/s.</td>
</tr>
<tr>
<td>BIT</td>
<td>FUNCTION</td>
<td>TYPE</td>
<td>DESCRIPTION</td>
</tr>
<tr>
<td>-------</td>
<td>-----------------------------------------------</td>
<td>-------</td>
<td>-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>9:4</td>
<td>Maximum Link Width</td>
<td>RO</td>
<td>Indicates the maximum width of the given PCIe Link. The width of each port is determined by strapped pin or EEPROM pre-loaded value.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 000001b (x1) for Port 0. Reset to 000001b (x1) for Port 1. Reset to 000001b (x1) for Port 2.</td>
</tr>
<tr>
<td>11:10</td>
<td>Active State Power Management (ASPM) Support</td>
<td>RO</td>
<td>Indicates the level of ASPM supported on the given PCIe Link. Each port of Swidge supports L0s and L1 entry. The default value may be changed by SMBus or auto-loading from EEPROM.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 01b.</td>
</tr>
<tr>
<td>14:12</td>
<td>L0s Exit Latency</td>
<td>RO</td>
<td>Indicates the L0s exit latency for the given PCIe Link. The length of time this port requires to complete transition from L0s to L0 is in the range of 256ns to less than 512ns. The default value may be changed by SMBus or auto-loading from EEPROM.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 011b.</td>
</tr>
<tr>
<td>17:15</td>
<td>L1 Exit Latency</td>
<td>RO</td>
<td>Indicates the L1 exit latency for the given PCIe Link. The length of time this port requires to complete transition from L1 to L0 is in the range of 16us to less than 32us. The default value may be changed by SMBus or auto-loading from EEPROM.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 000b.</td>
</tr>
<tr>
<td>18</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>19</td>
<td>Surprise Down Error Reporting Capable</td>
<td>RO</td>
<td>For a Downstream port, this bit must be set to 1b if the component supports the optional capability of detecting and reporting a Surprise Down error condition.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>For Upstream Ports, which does not support this optional capability, this bit must be hardwired to 0b.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Rest to 0b.</td>
</tr>
<tr>
<td>20</td>
<td>Data Link Layer Active Reporting Capable</td>
<td>RO</td>
<td>For a Downstream Port, this bit must be set to 1b if the component supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. For a hot-plug capable Downstream Port, this bit must be set to 1b.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>For Upstream Port, this bit must be hardwired to 0b.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 0b for upstream port. Reset to 1b for downstream ports with hot-plug capable</td>
</tr>
<tr>
<td>23:21</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 000b</td>
</tr>
<tr>
<td>31:24</td>
<td>Port Number</td>
<td>RO</td>
<td>Indicates the PCIe Port Number for the given PCIe Link. The default value may be changed by SMBus or auto-loading from EEPROM.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 00h for Port 0. Reset to 01h for Port 1. Reset to 02h for Port 2.</td>
</tr>
</tbody>
</table>

### 7.2.75 LINK CONTROL REGISTER – OFFSET F0h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:0</td>
<td>Active State Power Management (ASPM) Control</td>
<td>RW</td>
<td>00b: ASPM is Disabled 01b: L0s Entry Enabled 10b: L1 Entry Enabled 11b: L0s and L1 Entry Enabled Note that the receiver must be capable of entering L0s even when the field is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 00b.</td>
</tr>
<tr>
<td>2</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>BIT</td>
<td>FUNCTION</td>
<td>TYPE</td>
<td>DESCRIPTION</td>
</tr>
<tr>
<td>-----</td>
<td>-----------------------------------</td>
<td>------</td>
<td>----------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>3</td>
<td>Read Completion Boundary (RCB)</td>
<td>RO</td>
<td>Does not apply to PCI Express Swidge. Returns ‘0’ when read.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>4</td>
<td>Link Disable</td>
<td>RW</td>
<td>At upstream port, it is not allowed to disable the link, so this bit is hardwired to ‘0’. For downstream ports, it disables the link when this bit is set.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>5</td>
<td>Retrain Link</td>
<td>RW</td>
<td>At upstream port, it is not allowed to retrain the link, so this bit is hardwired to 0b. For downstream ports, it initiates Link Retraining when this bit is set.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This bit always returns 0b when read.</td>
</tr>
<tr>
<td>6</td>
<td>Common Clock Configuration</td>
<td>RW</td>
<td>0b: The components at both ends of a link are operating with asynchronous reference clock 1b: The components at both ends of a link are operating with a distributed common reference clock</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>7</td>
<td>Extended Synch</td>
<td>RW</td>
<td>When set, it transmits 4096 FTS ordered sets in the L0s state for entering L0 state and transmits 1024 TS1 ordered sets in the L1 state for entering L0 state.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>8</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 00h.</td>
</tr>
</tbody>
</table>

### 7.2.76 LINK STATUS REGISTER – OFFSET F0h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>19:16</td>
<td>Link Speed</td>
<td>RO</td>
<td>Read as 0001b to indicate the negotiated speed of the Express link is 2.5 Gb/s.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Indicates the negotiated width of the given PCIe link.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 000001b (x1).</td>
</tr>
<tr>
<td>25:20</td>
<td>Negotiated Link Width</td>
<td>RO</td>
<td>When set, indicates a Link training error occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by hardware upon successful training of the link to the L0 link state.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>26</td>
<td>Training Error</td>
<td>RO</td>
<td>When set, indicates the link training is in progress. Hardware clears this bit once link training is complete.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>27</td>
<td>Link Training</td>
<td>RO</td>
<td>0b: the Swidge uses an independent clock irrespective of the presence of a reference on the connector</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1b: the Swidge uses the same reference clock that the platform provides on the connector</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The default value may be changed by the status of strapped pin, SMBus, or auto-loading from EEPROM.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>28</td>
<td>Slot Clock Configuration</td>
<td>HwInt</td>
<td>Indicates the status of the Data Link Control and Management State Machine.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>It returns a 1b to indicate the DL_Active state, 0b otherwise.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>29</td>
<td>Data Link Layer Link Active</td>
<td>RO</td>
<td>Reset to 00b.</td>
</tr>
</tbody>
</table>
### 7.2.77 SLOT CAPABILITIES REGISTER (Downstream Port Only) – OFFSET F4h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Attention Button Present</td>
<td>RO</td>
<td>When set, it indicates that an Attention Button is implemented on the chassis for this slot. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.</td>
</tr>
<tr>
<td>1</td>
<td>Power Controller Present</td>
<td>RO</td>
<td>When set, it indicates that a Power Controller is implemented for this slot. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.</td>
</tr>
<tr>
<td>2</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>3</td>
<td>Attention Indicator Present</td>
<td>RO</td>
<td>When set, it indicates that an Attention Indicator is implemented on the chassis for this slot. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.</td>
</tr>
<tr>
<td>4</td>
<td>Power Indicator Present</td>
<td>RO</td>
<td>When set, it indicates that a Power Indicator is implemented on the chassis for this slot. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.</td>
</tr>
<tr>
<td>5</td>
<td>Hot-Plug Surprise</td>
<td>RO</td>
<td>When set, it indicates that a device present in this slot might be removed from the system without any prior notification. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.</td>
</tr>
<tr>
<td>6</td>
<td>Hot-Capable</td>
<td>HwInt</td>
<td>When set, it indicates that this slot is capable of supporting Hot-Plug operation. The default value may be changed by the status of strapped pin or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>14:7</td>
<td>Slot Power Limit Value</td>
<td>RW</td>
<td>It applies to Downstream Port only. In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. Writes to this register also cause the Port to send the Set_Slot_Power_Limit message. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 00h.</td>
</tr>
<tr>
<td>16:15</td>
<td>Slot Power Limit Scale</td>
<td>RW</td>
<td>It applies to Downstream Port only. Specifies the scale used for the Slot Power Limit Value. Writes to this register also cause the Port to send the Set_Slot_Power_Limit message. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 00b.</td>
</tr>
<tr>
<td>18:17</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 00b.</td>
</tr>
<tr>
<td>31:19</td>
<td>Physical Slot Number</td>
<td>RO</td>
<td>It indicates the physical slot number attached to this Port. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0.</td>
</tr>
</tbody>
</table>

### 7.2.78 SLOT CONTROL REGISTER (Downstream Port Only) – OFFSET F8h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Attention Button Pressed Enable</td>
<td>RW</td>
<td>When set, it enables the generation of Hot-Plug interrupt or wakeup event on an attention button pressed event. Reset to 0b.</td>
</tr>
<tr>
<td>1</td>
<td>Power Fault Detected Enable</td>
<td>RW</td>
<td>When set, it enables the generation of Hot-Plug interrupt or wakeup event on a power fault event. Reset to 0b.</td>
</tr>
<tr>
<td>2</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>BIT</td>
<td>FUNCTION</td>
<td>TYPE</td>
<td>DESCRIPTION</td>
</tr>
<tr>
<td>-----</td>
<td>---------------------------</td>
<td>------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>3</td>
<td>Presence Detect Changed Enable</td>
<td>RW</td>
<td>When set, it enables the generation of Hot-Plug interrupt or wakeup event on a presence detect changed event. Reset to 0b.</td>
</tr>
<tr>
<td>4</td>
<td>Command Completed Interrupt Enable</td>
<td>RW</td>
<td>When set, it enables the generation of Hot-Plug interrupt when the Hot-Plug Controller completes a command. Reset to 0b.</td>
</tr>
<tr>
<td>5</td>
<td>Hot-Plug Interrupt Enable</td>
<td>RW</td>
<td>When set, it enables generation of Hot-Plug interrupt on enabled Hot-Plug events. Reset to 0b.</td>
</tr>
</tbody>
</table>
| 7:6 | Attention Indicator Control | RW   | Controls the display of Attention Indicator.  
00b: Reserved  
01b: On  
10b: Blink  
11b: Off  
Writes to this register also cause the Port to send the ATTENTION_INDICATOR_* Messages. Reset to 11b. |
| 9:8 | Power Indicator Control | RW   | Controls the display of Power Indicator.  
00b: Reserved  
01b: On  
10b: Blink  
11b: Off  
Writes to this register also cause the Port to send the POWER_INDICATOR_* Messages. Reset to 11b. |
| 10  | Power Controller Control | RW   | 0b: reset the power state of the slot (Power On)  
1b: set the power state of the slot (Power Off)  
Reset to 0b. |
| 11  | Reserved | RO   | Reset to 0b. |
| 12  | Data Link Layer State Changed Enable | RW   | If the Data Link Layer Link Active capability is implemented, when set to 1b, this field enables software notification when Data Link Layer Link Active field is changed. Reset to 0b. |
| 15:13 | Reserved | RO   | Reset to 000b |

### 7.2.79 SLOT STATUS REGISTER (Downstream Port Only) – OFFSET F8h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>Attention Button Pressed</td>
<td>RW1C</td>
<td>When set, it indicates the Attention Button is pressed. Reset to 0b.</td>
</tr>
<tr>
<td>17</td>
<td>Power Fault Detected</td>
<td>RW1C</td>
<td>When set, it indicates a Power Fault is detected. Reset to 0b.</td>
</tr>
<tr>
<td>18</td>
<td>MRL Sensor Changed</td>
<td>RO</td>
<td>When set, it indicates a MRL Sensor Changed is detected. Reset to 0b.</td>
</tr>
<tr>
<td>19</td>
<td>Presence Detect Changed</td>
<td>RW1C</td>
<td>When set, it indicates a Presence Detect Changed is detected. Reset to 0b.</td>
</tr>
<tr>
<td>20</td>
<td>Command Completed</td>
<td>RW1C</td>
<td>When set, it indicates the Hot-Plug Controller completes an issued command. Reset to 0b.</td>
</tr>
</tbody>
</table>
### BIT FUNCTION TYPE DESCRIPTION

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>21</td>
<td>MRL Sensor State</td>
<td>RO</td>
<td>Reflects the status of MRL Sensor.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0b: MRL Closed</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1b: MRL Opened</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>22</td>
<td>Presence Detect State</td>
<td>RO</td>
<td>Indicates the presence of a card in the slot.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0b: Slot Empty</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1b: Card Present in slot</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This register is implemented on all Downstream Ports that implement slots.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>For Downstream Ports not connected to slots (where the Slot Implemented</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>bit of the PCI Express Capabilities register is 0b), this bit returns 1b.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 1b.</td>
</tr>
<tr>
<td>23</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0.</td>
</tr>
<tr>
<td>24</td>
<td>Data Link Layer State Changed</td>
<td>RW1C</td>
<td>This bit is set when the value reported in the Data Link Layer Link Active</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>field of the Link Status register is changed.</td>
</tr>
<tr>
<td>31:25</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0.</td>
</tr>
</tbody>
</table>

### 7.2.80 PCI EXPRESS ADVANCED ERROR REPORTING CAPABILITY ID REGISTER – OFFSET 100h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:0</td>
<td>Extended Capabilities ID</td>
<td>RO</td>
<td>Read as 0001h to indicate that these are PCI express extended capability</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>registers for advance error reporting.</td>
</tr>
</tbody>
</table>

### 7.2.81 CAPABILITY VERSION – OFFSET 100h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>19:16</td>
<td>Capability Version</td>
<td>RO</td>
<td>Read as 1h. Indicates PCI-SIG defined PCI Express capability structure</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>version number.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 1h.</td>
</tr>
</tbody>
</table>

### 7.2.82 NEXT ITEM POINTER REGISTER – OFFSET 100h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:20</td>
<td>Next Capability Offset</td>
<td>RO</td>
<td>Pointer points to the PCI Express Extended VC capability register (140h).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 140h (upstream port).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 20Ch (downstream port).</td>
</tr>
</tbody>
</table>

### 7.2.83 UNCORRECTABLE ERROR STATUS REGISTER – OFFSET 104h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Training Error Status</td>
<td>RW1CS</td>
<td>When set, indicates that the Training Error event has occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>3:1</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 00b.</td>
</tr>
<tr>
<td>4</td>
<td>Data Link Protocol Error Status</td>
<td>RW1CS</td>
<td>When set, indicates that the Data Link Protocol Error event has occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>11:5</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0.</td>
</tr>
</tbody>
</table>
### BIT | FUNCTION | TYPE | DESCRIPTION
--- | --- | --- | ---
12 | Poisoned TLP Status | RW1CS | When set, indicates that a Poisoned TLP has been received or generated. Reset to 0b.
13 | Flow Control Protocol Error Status | RW1CS | When set, indicates that the Flow Control Protocol Error event has occurred. Reset to 0b.
14 | Completion Timeout Status | RW1CS | When set, indicates that the Completion Timeout event has occurred. Reset to 0b.
15 | Completer Abort Status | RW1CS | When set, indicates that the Completer Abort event has occurred. Reset to 0b.
16 | Unexpected Completion Status | RW1CS | When set, indicates that the Unexpected Completion event has occurred. Reset to 0b.
17 | Receiver Overflow Status | RW1CS | When set, indicates that the Receiver Overflow event has occurred. Reset to 0b.
18 | Malformed TLP Status | RW1CS | When set, indicates that a Malformed TLP has been received. Reset to 0b.
19 | ECRC Error Status | RW1CS | When set, indicates that an ECRC Error has been detected. Reset to 0b.
20 | Unsupported Request Error Status | RW1CS | When set, indicates that an Unsupported Request event has occurred. Reset to 0b.
31:21 | Reserved | RO | Reset to 0.

#### 7.2.84 UNCORRECTABLE ERROR MASK REGISTER – OFFSET 108h

| BIT | FUNCTION | TYPE | DESCRIPTION |
--- | --- | --- | ---
0 | Training Error Mask | RWS | When set, the Training Error event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
3:1 | Reserved | RO | Reset to 000b.
4 | Data Link Protocol Error Mask | RWS | When set, the Data Link Protocol Error event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
11:5 | Reserved | RO | Reset to 0.
12 | Poisoned TLP Mask | RWS | When set, an event of Poisoned TLP has been received or generated is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
13 | Flow Control Protocol Error Mask | RWS | When set, the Flow Control Protocol Error event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
14 | Completion Timeout Mask | RWS | When set, the Completion Timeout event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
15 | Completer Abort Mask | RWS | When set, the Completer Abort event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
16 | Unexpected Completion Mask | RWS | When set, the Unexpected Completion event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>17</td>
<td>Receiver Overflow Mask</td>
<td>RWS</td>
<td>When set, the Receiver Overflow event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.</td>
</tr>
<tr>
<td>18</td>
<td>Malformed TLP Mask</td>
<td>RWS</td>
<td>When set, an event of Malformed TLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.</td>
</tr>
<tr>
<td>19</td>
<td>ECRC Error Mask</td>
<td>RWS</td>
<td>When set, an event of ECRC Error has been detected is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.</td>
</tr>
<tr>
<td>20</td>
<td>Unsupported Request Error Mask</td>
<td>RWS</td>
<td>When set, the Unsupported Request event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.</td>
</tr>
<tr>
<td>31:21</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0.</td>
</tr>
</tbody>
</table>

7.2.85 UNCORRECTABLE ERROR SEVERITY REGISTER – Offset 10Ch

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Training Error Severity</td>
<td>RWS</td>
<td>0b: Non-Fatal 1b: Fatal Reset to 1b.</td>
</tr>
<tr>
<td>3:1</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 000b.</td>
</tr>
<tr>
<td>4</td>
<td>Data Link Protocol Error Severity</td>
<td>RWS</td>
<td>0b: Non-Fatal 1b: Fatal Reset to 1b.</td>
</tr>
<tr>
<td>11:5</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0.</td>
</tr>
<tr>
<td>12</td>
<td>Poisoned TLP Severity</td>
<td>RWS</td>
<td>0b: Non-Fatal 1b: Fatal Reset to 0b.</td>
</tr>
<tr>
<td>13</td>
<td>Flow Control Protocol Error Severity</td>
<td>RWS</td>
<td>0b: Non-Fatal 1b: Fatal Reset to 1b.</td>
</tr>
<tr>
<td>14</td>
<td>Completion Timeout Error Severity</td>
<td>RWS</td>
<td>0b: Non-Fatal 1b: Fatal Reset to 0b.</td>
</tr>
<tr>
<td>15</td>
<td>Completer Abort Severity</td>
<td>RWS</td>
<td>0b: Non-Fatal 1b: Fatal Reset to 0b.</td>
</tr>
<tr>
<td>16</td>
<td>Unexpected Completion Severity</td>
<td>RWS</td>
<td>0b: Non-Fatal 1b: Fatal Reset to 0b.</td>
</tr>
<tr>
<td>17</td>
<td>Receiver Overflow Severity</td>
<td>RWS</td>
<td>0b: Non-Fatal 1b: Fatal Reset to 1b.</td>
</tr>
<tr>
<td>18</td>
<td>Malformed TLP Severity</td>
<td>RWS</td>
<td>0b: Non-Fatal 1b: Fatal Reset to 1b.</td>
</tr>
<tr>
<td>19</td>
<td>ECRC Error Severity</td>
<td>RWS</td>
<td>0b: Non-Fatal 1b: Fatal Reset to 0.</td>
</tr>
</tbody>
</table>
### 7.2.86 CORRECTABLE ERROR STATUS REGISTER – OFFSET 110h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
</table>
| 20  | Unsupported Request Error Severity | RWS | 0b: Non-Fatal  
|     |  |     | 1b: Fatal  
|     |  |     | Reset to 0b. |
| 31:21 | Reserved | RO | Reset to 0. |

### 7.2.87 CORRECTABLE ERROR MASK REGISTER – OFFSET 114h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
</table>
| 0   | Receiver Error Mask | RWS | When set, the Receiver Error event is not logged in the Header Log register and not issued as an Error Message to RC either.  
|     |  |     | Reset to 0b. |
| 5:1 | Reserved | RO | Reset to 00000b. |
| 6   | Bad TLP Mask | RWS | When set, the event of Bad TLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either.  
|     |  |     | Reset to 0b. |
| 7   | Bad DLLP Mask | RWS | When set, the event of Bad DLLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either.  
|     |  |     | Reset to 0b. |
| 8   | REPLAY_NUM Rollover Mask | RWS | When set, the REPLAY_NUM Rollover event is not logged in the Header Log register and not issued as an Error Message to RC either.  
|     |  |     | Reset to 0b. |
| 11:9 | Reserved | RO | Reset to 000b. |
| 12  | Replay Timer Timeout Mask | RWS | When set, the Replay Timer Timeout event is not logged in the Header Log register and not issued as an Error Message to RC either.  
|     |  |     | Reset to 0b. |
| 13  | Advisory Non-Fatal Error Mask | RWS | When set, the Advisory Non-Fatal Error event is not logged in the Header Log register and not issued as an Error Message to RC either.  
|     |  |     | Reset to 0b. |
| 31:14 | Reserved | RO | Reset to 0. |
### 7.2.88 ADVANCE ERROR CAPABILITIES AND CONTROL REGISTER – OFFSET 118h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>4:0</td>
<td>First Error Pointer</td>
<td>ROS</td>
<td>It indicates the bit position of the first error reported in the Uncorrectable Error Status register. Reset to 00000b.</td>
</tr>
<tr>
<td>5</td>
<td>ECRC Generation Capable</td>
<td>RO</td>
<td>When set, it indicates the Swidge has the capability to generate ECRC.</td>
</tr>
<tr>
<td>6</td>
<td>ECRC Generation Enable</td>
<td>RWS</td>
<td>When set, it enables the generation of ECRC when needed.</td>
</tr>
<tr>
<td>7</td>
<td>ECRC Check Capable</td>
<td>RO</td>
<td>When set, it indicates the Swidge has the capability to check ECRC.</td>
</tr>
<tr>
<td>8</td>
<td>ECRC Check Enable</td>
<td>RWS</td>
<td>When set, the function of checking ECRC is enabled.</td>
</tr>
<tr>
<td>31:9</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0.</td>
</tr>
</tbody>
</table>

### 7.2.89 HEADER LOG REGISTER – OFFSET From 11Ch to 128h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>1st DWORD</td>
<td>ROS</td>
<td>Hold the 1st DWORD of TLP Header. The Head byte is in big endian.</td>
</tr>
<tr>
<td>63:32</td>
<td>2nd DWORD</td>
<td>ROS</td>
<td>Hold the 2nd DWORD of TLP Header. The Head byte is in big endian.</td>
</tr>
<tr>
<td>95:64</td>
<td>3rd DWORD</td>
<td>ROS</td>
<td>Hold the 3rd DWORD of TLP Header. The Head byte is in big endian.</td>
</tr>
<tr>
<td>127:96</td>
<td>4th DWORD</td>
<td>ROS</td>
<td>Hold the 4th DWORD of TLP Header. The Head byte is in big endian.</td>
</tr>
</tbody>
</table>

### 7.2.90 PCI EXPRESS VIRTUAL CHANNEL CAPABILITY ID REGISTER – OFFSET 140h (Upstream Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:0</td>
<td>Extended Capabilities ID</td>
<td>RO</td>
<td>Read as 0002h to indicate that these are PCI express extended capability registers for virtual channel.</td>
</tr>
</tbody>
</table>

### 7.2.91 CAPABILITY VERSION – OFFSET 140h (Upstream Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>19:16</td>
<td>Capability Version</td>
<td>RO</td>
<td>Read as 1h. Indicates PCIe Base Specification compliance. Reset to 1h.</td>
</tr>
</tbody>
</table>

### 7.2.92 NEXT ITEM POINTER REGISTER – OFFSET 140h (Upstream Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:20</td>
<td>Next Capability Offset</td>
<td>RO</td>
<td>Pointer points to the PCI Express Power Budgeting Capability register (20Ch). Reset to 20Ch.</td>
</tr>
</tbody>
</table>
7.2.93 PORT VC CAPABILITY REGISTER 1 – OFFSET 144h (Upstream Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>2:0</td>
<td>Extended VC Count</td>
<td>RO</td>
<td>It indicates the number of extended Virtual Channels in addition to the default VC supported by the Swidge. Reset to 000b.</td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>6:4</td>
<td>Low Priority Extended VC Count</td>
<td>RO</td>
<td>It indicates the number of extended Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 000b.</td>
</tr>
<tr>
<td>7</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>9:8</td>
<td>Reference Clock</td>
<td>RO</td>
<td>It indicates the reference clock for Virtual Channels that support time-based WRR Port Arbitration. Defined encoding is 00b for 100 ns reference clock. Reset to 00b.</td>
</tr>
<tr>
<td>11:10</td>
<td>Port Arbitration Table Entry Size</td>
<td>RO</td>
<td>Read as 10b to indicate the size of Port Arbitration table entry in the device is 4 bits. Reset to 10b.</td>
</tr>
<tr>
<td>31:12</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0.</td>
</tr>
</tbody>
</table>

7.2.94 PORT VC CAPABILITY REGISTER 2 – OFFSET 148h (Upstream Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>VC Arbitration Capability</td>
<td>RO</td>
<td>It indicates the types of VC Arbitration supported by the device for the LPVC group. This field is valid when LPVC is greater than 0. The Swidge supports Hardware fixed arbitration scheme, e.g., Round Robin and Weight Round Robin arbitration with 32 phases in LPVC. Reset to 00000000b.</td>
</tr>
<tr>
<td>23:8</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0.</td>
</tr>
<tr>
<td>31:24</td>
<td>VC Arbitration Table Offset</td>
<td>RO</td>
<td>It indicates the location of the VC Arbitration Table as an offset from the base address of the Virtual Channel Capability register in the unit of DQWD (16 bytes). Reset to 00h.</td>
</tr>
</tbody>
</table>

7.2.95 PORT VC CONTROL REGISTER – OFFSET 14Ch (Upstream Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Load VC Arbitration Table</td>
<td>RW</td>
<td>When set, the programmed VC Arbitration Table is applied to the hardware. This bit always returns 0b when read. Reset to 0b.</td>
</tr>
<tr>
<td>3:1</td>
<td>VC Arbitration Select</td>
<td>RW</td>
<td>This field is used to configure the VC Arbitration by selecting one of the supported VC Arbitration schemes. The valid values for the schemes supported by Swidge are 0b and 1b. Other value than these written into this register will be treated as default. Reset to 0b.</td>
</tr>
<tr>
<td>15:4</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0.</td>
</tr>
</tbody>
</table>
### 7.2.96 PORT VC STATUS REGISTER – OFFSET 14Ch (Upstream Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>VC Arbitration Table Status</td>
<td>RO</td>
<td>When set, it indicates that any entry of the VC Arbitration Table is written by software. This bit is cleared when hardware finishes loading values stored in the VC Arbitration Table after the bit of “Load VC Arbitration Table” is set. Reset to 0b.</td>
</tr>
<tr>
<td>31:17</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0.</td>
</tr>
</tbody>
</table>

### 7.2.97 VC RESOURCE CAPABILITY REGISTER (0) – OFFSET 150h (Upstream Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Port Arbitration Capability</td>
<td>RO</td>
<td>It indicates the types of Port Arbitration supported by the VC resource. The Swidge supports Hardware fixed arbitration scheme, e.g., Round Robin, Weight Round Robin (WRR) arbitration with 128 phases (3–4 enabled ports) and Time-based WRR with 128 phases (3–4 enabled ports). Reset to 00001001b.</td>
</tr>
<tr>
<td>13:8</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 000000b.</td>
</tr>
<tr>
<td>14</td>
<td>Advanced Packet Switching</td>
<td>RO</td>
<td>When set, it indicates the VC resource only supports transaction optimized for Advanced Packet Switching (AS). Reset to 0b.</td>
</tr>
<tr>
<td>15</td>
<td>Reject Snoop Transactions</td>
<td>RO</td>
<td>This bit is not applied to PCIe Switch. Reset to 0b.</td>
</tr>
<tr>
<td>22:16</td>
<td>Maximum Time Slots</td>
<td>RO</td>
<td>It indicates the maximum numbers of time slots (minus one) are allocated for Isochronous traffic. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 7Fh.</td>
</tr>
<tr>
<td>31:24</td>
<td>Port Arbitration Table Offset</td>
<td>RO</td>
<td>It indicates the location of the Port Arbitration Table (n) as an offset from the base address of the Virtual Channel Capability register in the unit of DQWD (16 bytes). Reset to 04h for Port Arbitration Table (0).</td>
</tr>
</tbody>
</table>

### 7.2.98 VC RESOURCE CONTROL REGISTER (0) – OFFSET 154h (Upstream Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>TC/VC Map</td>
<td>RW</td>
<td>This field indicates the TCs that are mapped to the VC resource. Bit locations within this field correspond to TC values. When the bits in this field are set, it means that the corresponding TCs are mapped to the VC resource. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to FFh.</td>
</tr>
<tr>
<td>15:8</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 00h.</td>
</tr>
<tr>
<td>16</td>
<td>Load Port Arbitration Table</td>
<td>RW</td>
<td>When set, the programmed Port Arbitration Table is applied to the hardware. This bit always returns 0b when read. Reset to 0b.</td>
</tr>
<tr>
<td>19:17</td>
<td>Port Arbitration Select</td>
<td>RW</td>
<td>This field is used to configure the Port Arbitration by selecting one of the supported Port Arbitration schemes. The permissible values for the schemes supported by Swidge are 000b and 011b at VC0, other value than these written into this register will be treated as default. Reset to 000b.</td>
</tr>
</tbody>
</table>
### 7.2.99 VC RESOURCE STATUS REGISTER (0) – OFFSET 158h (Upstream Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:20</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0h.</td>
</tr>
<tr>
<td>26:24</td>
<td>VC ID</td>
<td>RO</td>
<td>This field assigns a VC ID to the VC resource.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 000h.</td>
</tr>
<tr>
<td>30:27</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0h.</td>
</tr>
<tr>
<td>31</td>
<td>VC Enable</td>
<td>RW</td>
<td>0b: it disables this Virtual Channel</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1b: it enables this Virtual Channel</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 1b.</td>
</tr>
</tbody>
</table>

### 7.2.100 PORT ARBITRATION TABLE REGISTER (0) – OFFSET 180h-1BCh (Upstream Only)

The Port arbitration table is a read-write register array that contains a table for Port arbitration. Each table entry allocates two bits to represent Port Number. The table entry size is dependent on the number of enabled ports (refer to bit 10 and 11 of Port VC capability register 1). The arbitration table contains 128 entries if three or four ports are to be enabled. The following table shows the register array layout for the size of entry equal to two.

#### Table 7-1 Table Entry Size in 4 Bits

<table>
<thead>
<tr>
<th>63 - 56</th>
<th>55 - 48</th>
<th>47 - 40</th>
<th>39 - 32</th>
<th>31 - 24</th>
<th>23 - 16</th>
<th>15 - 8</th>
<th>7 - 0</th>
<th>Byte Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>00h</td>
</tr>
<tr>
<td>[31:30]</td>
<td>[29:28]</td>
<td>[27:26]</td>
<td>[25:24]</td>
<td>[23:22]</td>
<td>[21:20]</td>
<td>[19:18]</td>
<td>[17:16]</td>
<td>08h</td>
</tr>
<tr>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>10h</td>
</tr>
<tr>
<td>[47:46]</td>
<td>[45:44]</td>
<td>[43:42]</td>
<td>[41:40]</td>
<td>[39:38]</td>
<td>[37:36]</td>
<td>[35:34]</td>
<td>[33:32]</td>
<td>18h</td>
</tr>
<tr>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>20h</td>
</tr>
<tr>
<td>[63:62]</td>
<td>[61:60]</td>
<td>[59:58]</td>
<td>[57:56]</td>
<td>[55:54]</td>
<td>[53:52]</td>
<td>[51:50]</td>
<td>[49:48]</td>
<td>28h</td>
</tr>
<tr>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>30h</td>
</tr>
<tr>
<td>[95:94]</td>
<td>[93:92]</td>
<td>[91:90]</td>
<td>[89:88]</td>
<td>[87:86]</td>
<td>[85:84]</td>
<td>[83:82]</td>
<td>[81:80]</td>
<td>38h</td>
</tr>
<tr>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td></td>
</tr>
<tr>
<td>[111:110]</td>
<td>[109:108]</td>
<td>[107:106]</td>
<td>[105:104]</td>
<td>[103:102]</td>
<td>[101:100]</td>
<td>[99:98]</td>
<td>[97:96]</td>
<td></td>
</tr>
<tr>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td>Phase</td>
<td></td>
</tr>
<tr>
<td>[127:126]</td>
<td>[125:124]</td>
<td>[123:122]</td>
<td>[121:120]</td>
<td>[119:118]</td>
<td>[117:116]</td>
<td>[115:114]</td>
<td>[113:112]</td>
<td></td>
</tr>
</tbody>
</table>
7.2.101 PCI EXPRESS POWER BUDGETING CAPABILITY ID REGISTER – OFFSET 20Ch

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:0</td>
<td>Extended Capabilities ID</td>
<td>RO</td>
<td>Read as 0000h to indicate that these are PCI express extended capability registers for power budgeting.</td>
</tr>
</tbody>
</table>

7.2.102 CAPABILITY VERSION – OFFSET 20Ch

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>19:16</td>
<td>Capability Version</td>
<td>RO</td>
<td>Read as 1h. Indicates PCIe Base Specification compliance.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 1h.</td>
</tr>
</tbody>
</table>

7.2.103 NEXT ITEM POINTER REGISTER – OFFSET 20Ch

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:20</td>
<td>Next Capability Offset</td>
<td>RO</td>
<td>Read as 00h. No other ECP registers.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 00h.</td>
</tr>
</tbody>
</table>

7.2.104 DATA SELECT REGISTER – OFFSET 210h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Data Selection</td>
<td>RW</td>
<td>It indexes the power budgeting data reported through the data register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When 00h, it selects D0 Max power budget</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When 01h, it selects D0 Sustained power budget</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Other values would return zero power budgets, which means not supported</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 00h.</td>
</tr>
<tr>
<td>31:8</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 000000h.</td>
</tr>
</tbody>
</table>

7.2.105 POWER BUDGETING DATA REGISTER – OFFSET 214h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Base Power</td>
<td>RO</td>
<td>It specifies the base power value in watts. This value represents the required</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>power budget in the given operation condition. The default value may be changed by auto-loading</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>from EEPROM.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 04h.</td>
</tr>
<tr>
<td>9:8</td>
<td>Data Scale</td>
<td>RO</td>
<td>It specifies the scale to apply to the base power value. The default value may be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>changed by auto-loading from EEPROM.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 00b.</td>
</tr>
<tr>
<td>12:10</td>
<td>PM Sub State</td>
<td>RO</td>
<td>It specifies the power management sub state of the given operation condition.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>It is initialized to the default sub state.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 000b.</td>
</tr>
<tr>
<td>14:13</td>
<td>PM State</td>
<td>RO</td>
<td>It specifies the power management state of the given operation condition.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>It defaults to the D0 power state. The default value may be changed by auto-loading from EEPROM.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 00b.</td>
</tr>
</tbody>
</table>
### BIT FUNCTION TYPE DESCRIPTION

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>17:15</td>
<td>Type</td>
<td>RO</td>
<td>It specifies the type of the given operation condition.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>It defaults to the Maximum power state. The default value may be changed by</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>auto-loading from EEPROM.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 111b.</td>
</tr>
<tr>
<td>20:18</td>
<td>Power Rail</td>
<td>RO</td>
<td>It specifies the power rail of the given operation condition.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 010b.</td>
</tr>
<tr>
<td>31:21</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0.</td>
</tr>
</tbody>
</table>

#### 7.2.106 POWER BUDGET CAPABILITY REGISTER – OFFSET 218h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>System Allocated</td>
<td>RO</td>
<td>When set, it indicates that the power budget for the device is included within</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>the system power budget. The default value may be changed by auto-loading</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>from EEPROM.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>31:1</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0.</td>
</tr>
</tbody>
</table>
7.3 USB DEVICE CONFIGURATION REGISTERS (FUNC0/FUNC1/FUNC2)

The swidge contains two Open HCI (OHCI) host controllers (function number 0 and 1) and one Enhanced HCI (EHCI) controller (function number 2). OHCI host controllers handle full-speed and low-speed device while EHCI host controller handles high speed device. The OHCI and EHCI host controllers are connected to an internal PCI express port (device number 3).

The following table details the allocation of the register fields of the PCI 2.3 compatible type 0 configuration space header.

<table>
<thead>
<tr>
<th>BYTE OFFSET</th>
<th>31 – 24</th>
<th>23 – 16</th>
<th>15 – 8</th>
<th>7 – 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device ID</td>
<td>Vendor ID</td>
<td>00h</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Status</td>
<td>Command</td>
<td>04h</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Class Code</td>
<td>Revision ID</td>
<td>08h</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>Header Type</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>Master Latency</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Base Address Register 0</td>
<td>Cache Line Size</td>
<td>0Ch</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>Interrupt Pin</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>Interrupt Line</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>40h – 5Fh</td>
<td>Port Wake Capability Register</td>
<td>FLADJ</td>
<td>SBRN</td>
<td>60h</td>
</tr>
<tr>
<td>Reserved</td>
<td>Capability Pointer</td>
<td>34h</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>Miscellaneous Register</td>
<td>68h</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6Ch – 7Fh</td>
<td>Power Management Capabilities</td>
<td>Next ID = 8C</td>
<td>Capability ID = 01</td>
<td>80h</td>
</tr>
<tr>
<td>PM Data</td>
<td>Power Management Data</td>
<td>84h</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Message Control Register</td>
<td>Next ID =E0</td>
<td>Capability ID = 05</td>
<td>8Ch</td>
<td></td>
</tr>
<tr>
<td>Low 32-bit Message Address</td>
<td>Message Data Register</td>
<td>90h</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>USB Physical Layer Control Register (USB Port 1)</td>
<td>A0h</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>USB Physical Layer Control Register (USB Port 2)</td>
<td>A4h</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>USB Physical Layer Control Register (USB Port 3)</td>
<td>A8h</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>USB Physical Layer Control Register (USB Port 4)</td>
<td>ACh</td>
<td></td>
<td></td>
</tr>
<tr>
<td>80h – DCCh</td>
<td>PCI Express Capability Register</td>
<td>Next ID = 00h</td>
<td>Capability ID = 10</td>
<td>E0h</td>
</tr>
<tr>
<td>Device Capability</td>
<td>Device Control</td>
<td>E4h</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Link Capability</td>
<td>Link Control</td>
<td>ECh</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
| Reserved    | F4h - FCh

7.3.1 VENDOR ID REGISTER – OFFSET 00h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:0</td>
<td>Vendor ID</td>
<td>RO</td>
<td>Identifies Pericom as the vendor of this device. The default value may be changed by auto-loading from EEPROM. Reset to 12D8h.</td>
</tr>
</tbody>
</table>
### 7.3.2 DEVICE ID REGISTER – OFFSET 00h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>Device ID</td>
<td>RO</td>
<td>Identifies this device as the PCIe to OHCI/EHCI I/O bridge. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 400Eh for OHCI (Func 0 /Func 1). Reset to 400Fh for EHCI (Func 2).</td>
</tr>
</tbody>
</table>

### 7.3.3 COMMAND REGISTER – OFFSET 04h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>I/O Space Enable</td>
<td>RW</td>
<td>Controls a device’s response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. Reset to 0b.</td>
</tr>
<tr>
<td>1</td>
<td>Memory Space Enable</td>
<td>RW</td>
<td>Controls a device’s response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to Memory Space accesses. Reset to 0b.</td>
</tr>
<tr>
<td>2</td>
<td>Bus Master Enable</td>
<td>RO</td>
<td>Controls a device’s ability to act as a master on the PCI bus. A value of 0 disables the device from generating PCI accesses. A value of 1 allows the device to behave as a bus master. Reset to 0b.</td>
</tr>
<tr>
<td>3</td>
<td>Special Cycle Enable</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 0b.</td>
</tr>
<tr>
<td>4</td>
<td>Memory Write And Invalidate Enable</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 0b.</td>
</tr>
<tr>
<td>5</td>
<td>VGA Palette Snoop Enable</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 0b.</td>
</tr>
<tr>
<td>6</td>
<td>Parity Error Response Enable</td>
<td>RW</td>
<td>Controls the device’s response to parity errors. When the bit is set, the device must take its normal action when a parity error is detected. When the bit is 0, the device sets its Detected Parity Error Status bit when an error is detected. Reset to 0b.</td>
</tr>
<tr>
<td>7</td>
<td>Wait Cycle Control</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 0b.</td>
</tr>
<tr>
<td>8</td>
<td>SERR# enable</td>
<td>RW</td>
<td>This bit, when set, enables reporting of Non-fatal and Fatal errors detected by the device to the Root Complex. Reset to 0b.</td>
</tr>
<tr>
<td>9</td>
<td>Fast Back-to-Back Enable</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 0b.</td>
</tr>
<tr>
<td>10</td>
<td>Interrupt Disable</td>
<td>RW</td>
<td>Controls the ability of the I/O bridge to generate INTx interrupt Messages. Reset to 0b.</td>
</tr>
<tr>
<td>15:11</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 00000b.</td>
</tr>
</tbody>
</table>

### 7.3.4 STATUS REGISTER – OFFSET 04h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>18:16</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 000b.</td>
</tr>
<tr>
<td>19</td>
<td>Interrupt Status</td>
<td>RO</td>
<td>Indicates that an INTx interrupt Message is pending internally to the device. Reset to 0b.</td>
</tr>
<tr>
<td>20</td>
<td>Capabilities List</td>
<td>RO</td>
<td>Set to 1 to enable support for the capability list (offset 34h is the pointer to the data structure) Reset to 1b.</td>
</tr>
<tr>
<td>21</td>
<td>66MHz Capable</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 0b.</td>
</tr>
<tr>
<td>BIT</td>
<td>FUNCTION</td>
<td>TYPE</td>
<td>DESCRIPTION</td>
</tr>
<tr>
<td>-------</td>
<td>-----------------------------------</td>
<td>--------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>22</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>23</td>
<td>Fast Back-to-Back Capable</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 0b.</td>
</tr>
<tr>
<td>24</td>
<td>Master Data Parity Error</td>
<td>RWC</td>
<td>It is not implemented. Hardwired to 0b.</td>
</tr>
<tr>
<td>26:25</td>
<td>DEVSEL# Timing</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 0b.</td>
</tr>
<tr>
<td>27</td>
<td>Signaled Target Abort</td>
<td>RWC</td>
<td>Set to 1 (by a completer) whenever completing a request in the I/O bridge side using Completer Abort Completion Status. Reset to 0b.</td>
</tr>
<tr>
<td>28</td>
<td>Received Target Abort</td>
<td>RWC</td>
<td>It is not implemented. Hardwired to 0b.</td>
</tr>
<tr>
<td>29</td>
<td>Received Master Abort</td>
<td>RWC</td>
<td>It is not implemented. Hardwired to 0b.</td>
</tr>
<tr>
<td>30</td>
<td>Signaled System Error</td>
<td>RWC</td>
<td>Set to 1 when the I/O bridge sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Command register is 1. Reset to 0b.</td>
</tr>
<tr>
<td>31</td>
<td>Detected Parity Error</td>
<td>RWC</td>
<td>Set to 1 whenever the I/O bridge receives a Poisoned TLP.                   Reset to 0b.</td>
</tr>
</tbody>
</table>

### 7.3.5 REVISION ID REGISTER – OFFSET 08h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Revision</td>
<td>RO</td>
<td>Indicates revision number of the I/O bridge. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 00h.</td>
</tr>
</tbody>
</table>

### 7.3.6 CLASS CODE REGISTER – OFFSET 08h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:8</td>
<td>Programming Interface</td>
<td>RO</td>
<td>Read as 10h to indicate no programming interfaces have been defined for OHCI controllers. Read as 20h to indicate no programming interfaces have been defined for EHCI controllers. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>23:16</td>
<td>Sub-Class Code</td>
<td>RO</td>
<td>Read as 03h to indicate device is USB bus controller. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>31:24</td>
<td>Base Class Code</td>
<td>RO</td>
<td>Read as 0Ch to indicate device is a serial bus controller. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
</tbody>
</table>

### 7.3.7 CACHE LINE REGISTER – OFFSET 0Ch

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Cache Line Size</td>
<td>RW</td>
<td>The cache line size register is set by the system firmware and the operating system to system cache line size. This field is implemented by PCI Express devices as a RW field for legacy compatibility purposes but has no impact on any PCI Express device functionality. Reset to 00h.</td>
</tr>
</tbody>
</table>
### 7.3.8 MASTER LATENCY TIMER REGISTER – OFFSET 0Ch

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:8</td>
<td>Latency timer</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 00h.</td>
</tr>
</tbody>
</table>

### 7.3.9 HEADER TYPE REGISTER – OFFSET 0Ch

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:16</td>
<td>Header Type</td>
<td>RO</td>
<td>Read as 80h to indicate it is a multi-function device.</td>
</tr>
</tbody>
</table>

### 7.3.10 BASE ADDRESS REGISTER 0 – OFFSET 10h (Func 0 and Func 1)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>11:0</td>
<td>Base Address 0</td>
<td>RO</td>
<td>Reset to 000h.</td>
</tr>
<tr>
<td>31:12</td>
<td>Base Address 0</td>
<td>RW</td>
<td>Use this I/O base address to map the OHCI registers.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 000000h.</td>
</tr>
</tbody>
</table>

### 7.3.11 BASE ADDRESS REGISTER 0 – OFFSET 10h (Func 2 Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Base Address 0</td>
<td>RO</td>
<td>Reset to 00h.</td>
</tr>
<tr>
<td>31:8</td>
<td>Base Address 0</td>
<td>RW</td>
<td>Use this I/O base address to map the EHCI registers.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 0000000h.</td>
</tr>
</tbody>
</table>

### 7.3.12 SUBSYSTEM VENDOR REGISTER – OFFSET 2Ch

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:0</td>
<td>Sub Vendor ID</td>
<td>RO</td>
<td>Indicates the sub-system vendor id. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 12D8h.</td>
</tr>
</tbody>
</table>

### 7.3.13 SUBSYSTEM ID REGISTER – OFFSET 2Ch

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>Sub System ID</td>
<td>RO</td>
<td>Indicates the sub-system device id. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 400Eh for OHCI (Func 0 /Func 1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 400Fh for EHCI (Func 2)</td>
</tr>
</tbody>
</table>

### 7.3.14 CAPABILITIES POINTER REGISTER – OFFSET 34h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Capabilities Pointer</td>
<td>RO</td>
<td>This optional register points to a linked list of new capabilities implemented by the device. This default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The default value is 80h.</td>
</tr>
</tbody>
</table>
### 7.3.15 INTERRUPT LINE REGISTER – OFFSET 3Ch

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Interrupt Line</td>
<td>RW</td>
<td>Used to communicate interrupt line routing information. POST software will write the routing information into this register as it initializes and configures the system. Reset to 00h.</td>
</tr>
</tbody>
</table>

### 7.3.16 INTERRUPT PIN REGISTER – OFFSET 3Ch

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:8</td>
<td>Interrupt Pin</td>
<td>RO</td>
<td>Identifies the legacy interrupt Message(s) the device uses. Reset to 01h for Func 0, Reset to 02h for Func 1, Reset to 03h for Func 2</td>
</tr>
</tbody>
</table>

### 7.3.17 SERIAL BUS RELEASE NUMBER REGISTER – OFFSET 60h (Func 2 Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Serial Bus Release Number</td>
<td>RO</td>
<td>Release Number. All other combinations are reserved. Reset to 20h</td>
</tr>
</tbody>
</table>

### 7.3.18 FRAME LENGTH ADJUSTMENT REGISTER – OFFSET 60h (Func 2 Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>13:8</td>
<td>Frame Length Adjustment</td>
<td>RW</td>
<td>Frame Length Timing Value. Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is 32 (20h), which gives a SOF cycle time of 6000.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Frame Length (# High Speed bit times) (decimal)</th>
<th>FLADJ Value (Decimal)</th>
</tr>
</thead>
<tbody>
<tr>
<td>59488</td>
<td>0 (00h)</td>
</tr>
<tr>
<td>59504</td>
<td>1 (01h)</td>
</tr>
<tr>
<td>59520</td>
<td>2 (02h)</td>
</tr>
<tr>
<td>59536</td>
<td>3 (03h)</td>
</tr>
<tr>
<td>59552</td>
<td>4 (04h)</td>
</tr>
<tr>
<td>59568</td>
<td>5 (05h)</td>
</tr>
<tr>
<td>59584</td>
<td>6 (06h)</td>
</tr>
<tr>
<td>59600</td>
<td>7 (07h)</td>
</tr>
<tr>
<td>59616</td>
<td>8 (08h)</td>
</tr>
<tr>
<td>59632</td>
<td>9 (09h)</td>
</tr>
<tr>
<td>59648</td>
<td>10 (0Ah)</td>
</tr>
<tr>
<td>59664</td>
<td>11 (0Bh)</td>
</tr>
<tr>
<td>59680</td>
<td>12 (0Ch)</td>
</tr>
<tr>
<td>59696</td>
<td>13 (0Dh)</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>60480</td>
<td>62 (3Ah)</td>
</tr>
<tr>
<td>60500</td>
<td>63 (3Bh)</td>
</tr>
<tr>
<td>60520</td>
<td>...</td>
</tr>
<tr>
<td>60540</td>
<td>...</td>
</tr>
<tr>
<td>60560</td>
<td>...</td>
</tr>
</tbody>
</table>

Reset to 20h

| 15:14 | Reserved | RO | Reset to 0 |

### 7.3.19 PORT WAKE CAPABILITY REGISTER – OFFSET 60h (Func 2 Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>20:16</td>
<td>Port Wake Capability Mask</td>
<td>RW</td>
<td>Bit position zero of this register indicates whether the register is implemented. A one in bit position zero indicates that the register is implemented. Bit positions 1 through 4 correspond to a physical port implemented on this host controller. For example, bit position 1 corresponds to port 1, position 2 to port 2, etc.</td>
</tr>
</tbody>
</table>
### MISCELLANEOUS REGISTER – OFFSET 68h (Func 2 Only)

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Enable Basic Mode</td>
<td>RW</td>
<td>When set, only one USB controller will activate at the same time. Otherwise,</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>all USB controllers allow active at the same time. The default value may be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>1</td>
<td>Enable Boundary 64-byte</td>
<td>RW</td>
<td>When set, the max_read_request_size is set to 64 byte. The default value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>2</td>
<td>Enable EHCI Prefetch</td>
<td>RW</td>
<td>When set, EHCI will enable the prefetch function. The default value may</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
<td>RW</td>
<td>Reset to 0.</td>
</tr>
<tr>
<td>4</td>
<td>Enable User Max_Read_Request_Size</td>
<td>RW</td>
<td>A 2-bit register contains a user-defined value. The default value may be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>6:5</td>
<td>User Max_Read_Request_Size</td>
<td>RW</td>
<td>A 7-bit register contains a user-defined value for the prefetch size and the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>unit is dword. The default value may be changed by SMBUS or auto-loading</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>from EEPROM.</td>
</tr>
<tr>
<td>7</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0.</td>
</tr>
<tr>
<td>14:8</td>
<td>Prefetch DW Size</td>
<td>RW</td>
<td>The pointer points to the Message capability register (8Ch). The default value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>15</td>
<td>Reserved</td>
<td>RW</td>
<td>Reset to 1b.</td>
</tr>
<tr>
<td>31:16</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0000h.</td>
</tr>
</tbody>
</table>

### POWER MANAGEMENT CAPABILITY ID REGISTER – OFFSET 80h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Enhanced Capabilities ID</td>
<td>RO</td>
<td>Read as 01h to indicate that these are power management enhanced capability</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>registers.</td>
</tr>
</tbody>
</table>

### NEXT ITEM POINTER REGISTER – OFFSET 80h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:8</td>
<td>Next Item Pointer</td>
<td>RO</td>
<td>The pointer points to the Message capability register (8Ch). The default value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 8Ch.</td>
</tr>
</tbody>
</table>
## 7.3.23 POWER MANAGEMENT CAPABILITIES REGISTER – OFFSET 80h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>18:16</td>
<td>Power Management Revision</td>
<td>RO</td>
<td>Read as 011b to indicate the I/O bridge is compliant to Revision 1.1 of PCI Power Management Interface Specifications.</td>
</tr>
<tr>
<td>19</td>
<td>PME# Clock</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 0b.</td>
</tr>
<tr>
<td>20</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>21</td>
<td>Device Specific Initialization</td>
<td>RO</td>
<td>Read as 0b to indicate the I/O bridge does not have device specific initialization requirements. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>24:22</td>
<td>AUX Current</td>
<td>RO</td>
<td>Reset as 111b to indicate the I/O bridge need 375 mA in D3 state. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>25</td>
<td>D1 Power State Support</td>
<td>RO</td>
<td>Read as 1b to indicate the I/O bridge supports the D1 power management state. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>26</td>
<td>D2 Power State Support</td>
<td>RO</td>
<td>Read as 1b to indicate the I/O bridge supports the D2 power management state. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>31:27</td>
<td>PME# Support</td>
<td>RO</td>
<td>Read as 11111b to indicate the I/O bridge supports the forwarding of PME# message in all power states. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
</tbody>
</table>

## 7.3.24 POWER MANAGEMENT DATA REGISTER – OFFSET 84h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:0</td>
<td>Power State</td>
<td>RW</td>
<td>Indicates the current power state of the I/O bridge. Writing a value of D0 causes a hot reset without asserting PEREST_L when the previous state was D3.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00b: D0 state</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01b: D1 state</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10b: D2 state</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11b: D3 hot state</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 00b.</td>
</tr>
<tr>
<td>2</td>
<td>Reserved</td>
<td>RO</td>
<td>Read as 0b.</td>
</tr>
<tr>
<td>3</td>
<td>No_Soft_Reset</td>
<td>RO</td>
<td>When set, this bit indicates that I/O bridge transitioning from D3hot to D0 does not perform an internal reset. When clear, an internal reset is performed when power state transits from D3hot to D0. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 1b.</td>
</tr>
<tr>
<td>7:4</td>
<td>Reserved</td>
<td>RO</td>
<td>Read as 0b.</td>
</tr>
<tr>
<td>8</td>
<td>PME# Enable</td>
<td>RW</td>
<td>When asserted, the I/O bridge will generate the PME# message.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>12:9</td>
<td>Data Select</td>
<td>RW</td>
<td>Select data registers.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 0h.</td>
</tr>
<tr>
<td>14:13</td>
<td>Data Scale</td>
<td>RO</td>
<td>Read as 00b.</td>
</tr>
<tr>
<td>15</td>
<td>PME status</td>
<td>RWC /RO</td>
<td>Indicates that the PME# message is pending internally to the I/O bridge for Func 0 and Func 1. This bit is reserved for Func 2 and always read as 0.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 0b (RWC) for OHCI (Func 0 /Func 1).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Read as 0b (RO) for EHCI (Func 2)</td>
</tr>
</tbody>
</table>
### 7.3.25 PPB SUPPORT EXTENSIONS – OFFSET 84h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>21:16</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 000000b.</td>
</tr>
<tr>
<td>22</td>
<td>B2_B3 Support for D3HOT</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 0b.</td>
</tr>
<tr>
<td>23</td>
<td>Bus Power / Clock Control Enable</td>
<td>RO</td>
<td>Does not apply to PCI Express. Must be hardwired to 0b.</td>
</tr>
</tbody>
</table>

### 7.3.26 PM DATA REGISTER – OFFSET 84h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td>PM Data Register</td>
<td>RO</td>
<td>PM Data Register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 00h.</td>
</tr>
</tbody>
</table>

### 7.3.27 MESSAGE SIGNALED INTERRUPT (MSI) Capability ID Register 8Ch

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Enhanced Capability ID</td>
<td>RO</td>
<td>Read as 05h to indicate that this is Message Signaled Interrupt capability register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The MSI Function is not implemented on this device.</td>
</tr>
</tbody>
</table>

### 7.3.28 MESSAGE SIGNALED INTERRUPT (MSI) NEXT ITEM POINTER 8Ch

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:8</td>
<td>Next Item Pointer</td>
<td>RO</td>
<td>The pointer points to the PCI Express capability register (E0h). The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to E0h.</td>
</tr>
</tbody>
</table>

### 7.3.29 MESSAGE CONTROL REGISTER – OFFSET 8Ch

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>MSI Enable</td>
<td>RW</td>
<td>The MSI Function is not implemented on this device.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>19:17</td>
<td>Multiple Message Capable</td>
<td>RO</td>
<td>The MSI Function is not implemented on this device.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Read as 000b.</td>
</tr>
<tr>
<td>22:20</td>
<td>Multiple Message Enable</td>
<td>RW</td>
<td>The MSI Function is not implemented on this device.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 000b.</td>
</tr>
<tr>
<td>23</td>
<td>64-bit address capable</td>
<td>RO</td>
<td>The MSI Function is not implemented on this device.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>31:24</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 00h.</td>
</tr>
</tbody>
</table>

### 7.3.30 MESSAGE ADDRESS REGISTER – OFFSET 90h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:0</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 00b.</td>
</tr>
</tbody>
</table>
### 7.3.31 MESSAGE DATA REGISTER – OFFSET 94h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>Message Address</td>
<td>RW</td>
<td>The MSI Function is not implemented on this device. Reset to 0.</td>
</tr>
</tbody>
</table>

### 7.3.32 USB PHYSICAL LAYER CONTROL REGISTER (USB PORT 1) – OFFSET A0h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>PMOS Strength for HS Driver Timing Control</td>
<td>RO</td>
<td>Reset to 0b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>2:1</td>
<td>NMOS Strength for HS Driver Timing Control</td>
<td>RO</td>
<td>Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>4:3</td>
<td>HS Driver Amplitude</td>
<td>RO</td>
<td>Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>8:5</td>
<td>HS Driver Slope Control</td>
<td>RO</td>
<td>Reset to 0000b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>10:9</td>
<td>Reference Voltage for Disconnect Circuit</td>
<td>RO</td>
<td>Reset to 10b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>12:11</td>
<td>Reference Voltage for Squelch Circuit</td>
<td>RO</td>
<td>Reset to 10b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>15:13</td>
<td>Reference Voltage for Calibration Circuit</td>
<td>RO</td>
<td>Reset to 100b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>17:16</td>
<td>Charge Pump Current for PLL</td>
<td>RO</td>
<td>Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>19:18</td>
<td>FS Rise/Fall Time Control</td>
<td>RO</td>
<td>Reset to 01b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>21:20</td>
<td>LS Rise/Fall Time Control</td>
<td>RO</td>
<td>Reset to 01b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>23:22</td>
<td>HS Driver Pre-Emphasis</td>
<td>RO</td>
<td>Reset to 0b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
</tbody>
</table>

### 7.3.33 USB PHYSICAL LAYER CONTROL REGISTER (USB PORT 2) – OFFSET A4h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>PMOS Strength for HS Driver Timing Control</td>
<td>RO</td>
<td>Reset to 0b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>2:1</td>
<td>NMOS Strength for HS Driver Timing Control</td>
<td>RO</td>
<td>Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>4:3</td>
<td>HS Driver Amplitude</td>
<td>RO</td>
<td>Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>8:5</td>
<td>HS Driver Slope Control</td>
<td>RO</td>
<td>Reset to 0000b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>10:9</td>
<td>Reference Voltage for Disconnect</td>
<td>RO</td>
<td>Reset to 10b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>BIT</td>
<td>FUNCTION</td>
<td>TYPE</td>
<td>DESCRIPTION</td>
</tr>
<tr>
<td>-------</td>
<td>-----------------------------------------------</td>
<td>------</td>
<td>-------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>12:11</td>
<td>Reference Voltage for Squelch Circuit</td>
<td>RO</td>
<td>Reset to 10b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>15:13</td>
<td>Reference Voltage for Calibration Circuit</td>
<td>RO</td>
<td>Reset to 100b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>17:16</td>
<td>Charge Pump Current for PLL.</td>
<td>RO</td>
<td>Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>19:18</td>
<td>FS Rise/Fall Time Control</td>
<td>RO</td>
<td>Reset to 01b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>21:20</td>
<td>LS Rise/Fall Time Control</td>
<td>RO</td>
<td>Reset to 01b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>23:22</td>
<td>HS Driver Pre-Emphasis</td>
<td>RO</td>
<td>Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
</tbody>
</table>

### 7.3.34 USB PHYSICAL LAYER CONTROL REGISTER (USB PORT 3) – OFFSET A8h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>PMOS Strength for HS Driver Timing Control</td>
<td>RO</td>
<td>Reset to 0b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>2:1</td>
<td>NMOS Strength for HS Driver Timing Control</td>
<td>RO</td>
<td>Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>4:3</td>
<td>HS Driver Amplitude</td>
<td>RO</td>
<td>Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>8:5</td>
<td>HS Driver Slope Control</td>
<td>RO</td>
<td>Reset to 0000b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>10:9</td>
<td>Reference Voltage for Disconnect Circuit</td>
<td>RO</td>
<td>Reset to 10b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>12:11</td>
<td>Reference Voltage for Squelch Circuit</td>
<td>RO</td>
<td>Reset to 10b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>15:13</td>
<td>Reference Voltage for Calibration Circuit</td>
<td>RO</td>
<td>Reset to 100b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>17:16</td>
<td>Charge Pump Current for PLL.</td>
<td>RO</td>
<td>Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>19:18</td>
<td>FS Rise/Fall Time Control</td>
<td>RO</td>
<td>Reset to 01b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>21:20</td>
<td>LS Rise/Fall Time Control</td>
<td>RO</td>
<td>Reset to 01b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>23:22</td>
<td>HS Driver Pre-Emphasis</td>
<td>RO</td>
<td>Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
</tbody>
</table>

### 7.3.35 USB PHYSICAL LAYER CONTROL REGISTER (USB PORT 4) – OFFSET ACh

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>PMOS Strength for HS Driver Timing Control</td>
<td>RO</td>
<td>Reset to 0b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>2:1</td>
<td>NMOS Strength for HS Driver Timing Control</td>
<td>RO</td>
<td>Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>4:3</td>
<td>HS Driver Amplitude</td>
<td>RO</td>
<td>Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>8:5</td>
<td>HS Driver Slope Control</td>
<td>RO</td>
<td>Reset to 0000b. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
</tbody>
</table>
### 7.3.36 PCI EXPRESS CAPABILITY ID REGISTER – OFFSET E0h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Enhanced Capabilities ID</td>
<td>RO</td>
<td>Read as 10h to indicate that these are PCI express enhanced capability registers. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
</tbody>
</table>

### 7.3.37 NEXT ITEM POINTER REGISTER – OFFSET E0h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:8</td>
<td>Next Item Pointer</td>
<td>RO</td>
<td>Read as 00h. No other ECP registers. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 00h.</td>
</tr>
</tbody>
</table>

### 7.3.38 PCI EXPRESS CAPABILITIES REGISTER – OFFSET E0h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>19:16</td>
<td>Capability Version</td>
<td>RO</td>
<td>Read as 001h to indicate the I/O bridge is compliant to Revision 1.0a of PCI Express Base Specifications. The default value may be changed by SMBUS or auto-loading from EEPROM.</td>
</tr>
<tr>
<td>23:20</td>
<td>Device/Port Type</td>
<td>RO</td>
<td>Indicates the type of Legacy PCI Express Endpoint device. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 1h.</td>
</tr>
<tr>
<td>24</td>
<td>Slot Implemented</td>
<td>RO</td>
<td>It is not implemented. Hardwired to 0b.</td>
</tr>
<tr>
<td>29:25</td>
<td>Interrupt Message Number</td>
<td>RO</td>
<td>It is not implemented. Hardwired to 0000b.</td>
</tr>
<tr>
<td>31:30</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 00b.</td>
</tr>
</tbody>
</table>

### 7.3.39 DEVICE CAPABILITIES REGISTER – OFFSET E4h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>2:0</td>
<td>Max_Payload_Size Supported</td>
<td>RO</td>
<td>Indicates the maximum payload size that the I/O bridge can support for TLPs. The I/O bridge supports 256 bytes max payload size. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 001b.</td>
</tr>
</tbody>
</table>
### 7.3.40 DEVICE CONTROL REGISTER – OFFSET E8h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Correctable Error Reporting Enable</td>
<td>RW</td>
<td>0b: Disable Correctable Error Reporting. 1b: Enable Correctable Error Reporting. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 0b.</td>
</tr>
<tr>
<td>1</td>
<td>Non-Fatal Error Reporting Enable</td>
<td>RW</td>
<td>0b: Disable Non-Fatal Error Reporting. 1b: Enable Non-Fatal Error Reporting. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 0b.</td>
</tr>
<tr>
<td>2</td>
<td>Fatal Error Reporting Enable</td>
<td>RW</td>
<td>0b: Disable Fatal Error Reporting. 1b: Enable Fatal Error Reporting. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 0b.</td>
</tr>
<tr>
<td>3</td>
<td>Unsupported Request Reporting Enable</td>
<td>RW</td>
<td>0b: Disable Unsupported Request Reporting. 1b: Enable Unsupported Request Reporting. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 0b.</td>
</tr>
</tbody>
</table>
### BIT FUNCTION TYPE DESCRIPTION

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>Enable Relaxed Ordering</td>
<td>RW</td>
<td>This field sets maximum TLP payload size for the device. Permissible values that can be programmed are indicated by the Max_Payload_Size Supported in the Device Capabilities register. Any value exceeding the Max_Payload_Size Supported written to this register results into clamping to the Max_Payload_Size Supported value. The default value may be SMBUS or changed by auto-loading from EEPROM. Reset to 0b.</td>
</tr>
<tr>
<td>7:5</td>
<td>Max_Payload_Size</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Extended Tag Field Enable</td>
<td>RO</td>
<td>It is not implemented. Hardwired to 0b.</td>
</tr>
<tr>
<td>9</td>
<td>Phantom Function Enable</td>
<td>RO</td>
<td>It is not implemented. Hardwired to 0b.</td>
</tr>
<tr>
<td>10</td>
<td>Auxiliary (AUX) Power PM Enable</td>
<td>RO</td>
<td>When set, indicates that the I/O bridge is enabled to draw AUX power independent of PME AUX power. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 0b.</td>
</tr>
<tr>
<td>11</td>
<td>Enable No Snoop</td>
<td>RO</td>
<td>It is not implemented. Hardwired to 0b.</td>
</tr>
<tr>
<td>14:12</td>
<td>Max_Read_Request_Size</td>
<td>RO</td>
<td>Reset to 000b.</td>
</tr>
<tr>
<td>15</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
</tbody>
</table>

#### 7.3.41 DEVICE STATUS REGISTER – OFFSET E8h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>Correctable Error Detected</td>
<td>RWIC</td>
<td>Asserted when correctable error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.</td>
</tr>
<tr>
<td>17</td>
<td>Non-Fatal Error Detected</td>
<td>RWIC</td>
<td>Asserted when non-fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.</td>
</tr>
<tr>
<td>18</td>
<td>Fatal Error Detected</td>
<td>RWIC</td>
<td>Asserted when fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.</td>
</tr>
<tr>
<td>19</td>
<td>Unsupported Request Detected</td>
<td>RWIC</td>
<td>Asserted when unsupported request is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.</td>
</tr>
<tr>
<td>20</td>
<td>AUX Power Detected</td>
<td>RO</td>
<td>Asserted when the AUX power is detected by the I/O bridge Reset to 1b.</td>
</tr>
<tr>
<td>21</td>
<td>Transactions Pending</td>
<td>RO</td>
<td>It is not implemented. Hardwired to 0b.</td>
</tr>
<tr>
<td>31:22</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 000b.</td>
</tr>
</tbody>
</table>

#### 7.3.42 LINK CAPABILITIES REGISTER – OFFSET ECCh

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>3:0</td>
<td>Maximum Link Speed</td>
<td>RO</td>
<td>Indicates the Maximum Link Speed of the given PCIe Link. Defined encodings are: 0001b, which indicates 2.5 Gb/s Link Reset to 1b.</td>
</tr>
</tbody>
</table>
### BIT FUNCTION TYPE DESCRIPTION

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>9:4</td>
<td>Maximum Link Width</td>
<td>RO</td>
<td>Indicates the maximum width of the given PCIe Link. Reset to 000001b (x1).</td>
</tr>
<tr>
<td>11:10</td>
<td>Active State Power Management (ASPM) Support</td>
<td>RO</td>
<td>Indicates the level of ASPM supported on the given PCIe Link. The I/O bridge supports L0s and L1 entry. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 01b.</td>
</tr>
<tr>
<td>14:12</td>
<td>L0s Exit Latency</td>
<td>RO</td>
<td>Indicates the L0s exit latency for the given PCIe Link. The length of time this I/O bridge requires to complete transition from L0s to L0 is in the range of 256ns to less than 512ns. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 011b.</td>
</tr>
<tr>
<td>17:15</td>
<td>L1 Exit Latency</td>
<td>RO</td>
<td>Indicates the L1 exit latency for the given PCIe Link. The length of time this I/O bridge requires to complete transition from L1 to L0 is in the range of 16us to less than 32us. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 00b.</td>
</tr>
<tr>
<td>23:18</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 00000b.</td>
</tr>
<tr>
<td>31:24</td>
<td>Port Number</td>
<td>RO</td>
<td>It is not implemented. Hardwired to 00h.</td>
</tr>
</tbody>
</table>

#### 7.3.43 LINK CONTROL REGISTER – OFFSET F0h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:0</td>
<td>Active State Power Management (ASPM) Control</td>
<td>RW</td>
<td>00b: ASPM is Disabled. 01b: L0s Entry Enabled. 10b: L1 Entry Enabled. 11b: L0s and L1 Entry Enabled. Note that the receiver must be capable of entering L0s even when the field is disabled. Reset to 00b.</td>
</tr>
<tr>
<td>2</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>3</td>
<td>Read Completion Boundary (RCB)</td>
<td>RO</td>
<td>It is not implemented. Hardwired to 0b.</td>
</tr>
<tr>
<td>4</td>
<td>Link Disable</td>
<td>RW</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>5</td>
<td>Retrain Link</td>
<td>RW</td>
<td>Reset to 0b.</td>
</tr>
<tr>
<td>6</td>
<td>Common Clock Configuration</td>
<td>RW</td>
<td>0b: The components at both ends of a link are operating with asynchronous reference clock. 1b: The components at both ends of a link are operating with a distributed common reference clock. Reset to 0b.</td>
</tr>
<tr>
<td>7</td>
<td>Extended Synch</td>
<td>RW</td>
<td>When set, it transmits 4096 FTS ordered sets in the L0s state for entering L0 state and transmits 1024 TS1 ordered sets in the L1 state for entering L0 state. Reset to 0b.</td>
</tr>
<tr>
<td>15:8</td>
<td>RsvdP</td>
<td>RO</td>
<td>Reset to 00h.</td>
</tr>
</tbody>
</table>

#### 7.3.44 LINK STATUS REGISTER – OFFSET F0h

<table>
<thead>
<tr>
<th>BIT</th>
<th>FUNCTION</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>19:16</td>
<td>Link Speed</td>
<td>RO</td>
<td>Indicates the negotiated Link Speed of the given PCIe Link. Defined encodings are: 0001b, which indicates 2.5 Gb/s Link. Reset to 1h.</td>
</tr>
<tr>
<td>BIT</td>
<td>FUNCTION</td>
<td>TYPE</td>
<td>DESCRIPTION</td>
</tr>
<tr>
<td>------</td>
<td>------------------------</td>
<td>------</td>
<td>-------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>25:20</td>
<td>Negotiated Link Width</td>
<td>RO</td>
<td>Indicates the negotiated width of the given PCIe Link, Reset to 000001b.</td>
</tr>
<tr>
<td>26</td>
<td>Training Error</td>
<td>RO</td>
<td>When set, indicates a Link training error occurred. This bit is cleared by hardware upon successful training of the link to the L0 link state. Reset to 0b.</td>
</tr>
<tr>
<td>27</td>
<td>Link Training</td>
<td>RO</td>
<td>When set, indicates the link training is in progress. Hardware clears this bit once link training is complete.</td>
</tr>
<tr>
<td>28</td>
<td>Slot Clock Configuration</td>
<td>RO</td>
<td>It is not implemented. Hardwired to 0b.</td>
</tr>
<tr>
<td>31:29</td>
<td>Reserved</td>
<td>RO</td>
<td>Reset to 000b.</td>
</tr>
</tbody>
</table>
8 CLOCK SCHEME

8.1 PCI EXPRESS INTERFACE

The PCI Express interface of PI7C9X440SL requires 100MHz differential clock inputs through REFCLKP and REFCLKN Pins as shown in the following table.

Table 8-1 Input Clock Requirements for PCI Express Interface

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference Frequency(1)</td>
<td>$\nu_f$</td>
<td>83.3</td>
<td>312.5</td>
<td>MHz</td>
</tr>
<tr>
<td>Accuracy</td>
<td>$A_n$</td>
<td>-300</td>
<td>300</td>
<td>ppm</td>
</tr>
<tr>
<td>Duty Cycle</td>
<td>$DC_c$</td>
<td>45</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td>&gt; 1.5 MHz to Nyquist RMS jitter after</td>
<td>$T_{REFCLK-HF-RMS}$</td>
<td>-</td>
<td>3.1</td>
<td>ps RMS</td>
</tr>
<tr>
<td>applying PCIe filter function</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 KHz – 1.5 MHz RMS jitter</td>
<td>$T_{REFCLK-LP-RMS}$</td>
<td>-</td>
<td>3.0</td>
<td>ps RMS</td>
</tr>
<tr>
<td>Spread Spectrum Clock frequency</td>
<td>$SSC_{freq}$</td>
<td>30</td>
<td>33</td>
<td>KHz</td>
</tr>
</tbody>
</table>

(1) Does not include ±300ppm. Only certain clock frequencies will produce valid PCI Express data.
(2) Specified as per PCI Express Card Electromechanical specification, Rev 1.1.

8.2 USB INTERFACE

PI7C9X440SL requires an external 12 MHz crystal or oscillator of ±60ppm tolerance.

Table 8-2 Input Clock Requirements for USB Interface

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock deviation</td>
<td></td>
<td>-150</td>
<td>150</td>
<td>ppm</td>
<td></td>
</tr>
<tr>
<td>Rise/fall time</td>
<td></td>
<td></td>
<td>200</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>Jitter (peak-to-peak)</td>
<td>&lt;1.2MHz</td>
<td>0</td>
<td>50</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>Jitter (peak-to-peak)</td>
<td>&gt;1.2MHz</td>
<td>0</td>
<td>100</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>Duty-cycle</td>
<td></td>
<td>40</td>
<td>60</td>
<td>%</td>
<td></td>
</tr>
</tbody>
</table>
9 IEEE 1149.1 COMPATIBLE JTAG CONTROLLER

An IEEE 1149.1 compatible Test Access Port (TAP) controller and associated TAP pins are provided to support boundary scan in PI7C9X440SL for board-level continuity test and diagnostics. The TAP pins assigned are TCK, TDI, TDO, TMS and TRST_L. All digital input, output, input/output pins are tested except TAP pins.

9.1 INSTRUCTION REGISTER

The IEEE 1149.1 Test Logic consists of a TAP controller, an instruction register, and a group of test data registers including Bypass and Boundary Scan registers. The TAP controller is a synchronous 16-state machine driven by the Test Clock (TCK) and the Test Mode Select (TMS) pins. An independent power on reset circuit is provided to ensure the machine is in TEST_LOGIC_RESET state at power-up.

PI7C9X440SL implements a 5-bit Instruction register to control the operation of the JTAG logic. The defined instruction codes are shown in the following table. Those bit combinations that are not listed are equivalent to the BYPASS (11111) instruction:

Table 9-1 Instruction Register Codes

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operation Code (binary)</th>
<th>Register Selected</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>EXTEST</td>
<td>00000</td>
<td>Boundary Scan</td>
<td>Drives / receives off-chip test data</td>
</tr>
<tr>
<td>SAMPLE</td>
<td>00001</td>
<td>Boundary Scan</td>
<td>Samples inputs / pre-loads outputs</td>
</tr>
<tr>
<td>HIGHZ</td>
<td>00101</td>
<td>Bypass</td>
<td>Tri-states output and I/O pins except TDO pin</td>
</tr>
<tr>
<td>CLAMP</td>
<td>00100</td>
<td>Bypass</td>
<td>Drives pins from boundary-scan register and selects Bypass register for shifts</td>
</tr>
<tr>
<td>IDCODE</td>
<td>01100</td>
<td>Device ID</td>
<td>Accesses the Device ID register, to read manufacturer ID, part number, and version number</td>
</tr>
<tr>
<td>BYPASS</td>
<td>11111</td>
<td>Bypass</td>
<td>Selected Bypass Register</td>
</tr>
<tr>
<td>INT_SCAN</td>
<td>00010</td>
<td>Internal Scan</td>
<td>Scan test</td>
</tr>
<tr>
<td>MEM_BIST</td>
<td>01010</td>
<td>Memory BIST</td>
<td>Memory BIST test</td>
</tr>
</tbody>
</table>

9.2 BYPASS REGISTER

The required bypass register (one-bit shift register) provides the shortest path between TDI and TDO when a bypass instruction is in effect. This allows rapid movement of test data to and from other components on the board. This path can be selected when no test operation is being performed on the PI7C9X440SL.

9.3 DEVICE ID REGISTER

This register identifies Pericom as the manufacturer of the device and details the part number and revision number for the device.

Table 9-2 JTAG Device ID Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Type</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-28</td>
<td>RO</td>
<td>0001</td>
<td>Version number</td>
</tr>
<tr>
<td>27-12</td>
<td>RO</td>
<td>10010010000000100</td>
<td>Last 4 digits (hex) of the die part number</td>
</tr>
<tr>
<td>11-1</td>
<td>RO</td>
<td>01000111111</td>
<td>Pericom identifier assigned by JEDEC</td>
</tr>
<tr>
<td>0</td>
<td>RO</td>
<td>1</td>
<td>Fixed bit equal to 1'b1</td>
</tr>
</tbody>
</table>
9.4 **BOUNDARY SCAN REGISTER**

The boundary scan register has a set of serial shift-register cells. A chain of boundary scan cells is formed by connected the internal signal of the PI7C9X440SL package pins. The VDD, VSS, and JTAG pins are not in the boundary scan chain. The input to the shift register is TDI and the output from the shift register is TDO. There are 4 different types of boundary scan cells, based on the function of each signal pin.

The boundary scan register cells are dedicated logic and do not have any system function. Data may be loaded into the boundary scan register master cells from the device input pins and output pin-drivers in parallel by the mandatory SAMPLE and EXTEST instructions. Parallel loading takes place on the rising edge of TCK.

9.5 **JTAG BOUNDARY SCAN REGISTER ORDER**

Table 9-3 JTAG Boundary Scan Register Definition

<table>
<thead>
<tr>
<th>Boundary Scan Register Number</th>
<th>Pin Name</th>
<th>Pin No</th>
<th>Type</th>
<th>Tri-state Control Cell</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>TEST5</td>
<td>114</td>
<td>Input</td>
<td>4</td>
</tr>
<tr>
<td>1</td>
<td>IRQ1_I</td>
<td>16</td>
<td>Bidir</td>
<td>4</td>
</tr>
<tr>
<td>2</td>
<td>IRQ12_I</td>
<td>17</td>
<td>Bidir</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>IRQ1_O</td>
<td>18</td>
<td>Bidir</td>
<td>4</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
<td>Control</td>
<td>4</td>
</tr>
<tr>
<td>5</td>
<td>IRQ12_O</td>
<td>19</td>
<td>Bidir</td>
<td>4</td>
</tr>
<tr>
<td>6</td>
<td>LEG_EMU_EN</td>
<td>20</td>
<td>Bidir</td>
<td>4</td>
</tr>
<tr>
<td>7</td>
<td>SMBCLK</td>
<td>21</td>
<td>Bidir</td>
<td>4</td>
</tr>
<tr>
<td>8</td>
<td>SMBDATA</td>
<td>64</td>
<td>Bidir</td>
<td>4</td>
</tr>
<tr>
<td>9</td>
<td>TEST3</td>
<td>65</td>
<td>Bidir</td>
<td>4</td>
</tr>
<tr>
<td>10</td>
<td>TEST6</td>
<td>66</td>
<td>Bidir</td>
<td>4</td>
</tr>
<tr>
<td>11</td>
<td>GPIO[0]</td>
<td>69</td>
<td>Bidir</td>
<td>12</td>
</tr>
<tr>
<td>12</td>
<td></td>
<td></td>
<td>Control</td>
<td>14</td>
</tr>
<tr>
<td>13</td>
<td>GPIO[1]</td>
<td>70</td>
<td>Bidir</td>
<td>16</td>
</tr>
<tr>
<td>14</td>
<td>GPIO[2]</td>
<td>71</td>
<td>Bidir</td>
<td>18</td>
</tr>
<tr>
<td>15</td>
<td>GPIO[3]</td>
<td>72</td>
<td>Bidir</td>
<td>20</td>
</tr>
<tr>
<td>16</td>
<td></td>
<td></td>
<td>Control</td>
<td>22</td>
</tr>
<tr>
<td>17</td>
<td>GPIO[4]</td>
<td>73</td>
<td>Bidir</td>
<td>24</td>
</tr>
<tr>
<td>18</td>
<td>GPIO[5]</td>
<td>74</td>
<td>Bidir</td>
<td>26</td>
</tr>
<tr>
<td>19</td>
<td>GPIO[6]</td>
<td>75</td>
<td>Bidir</td>
<td>28</td>
</tr>
<tr>
<td>20</td>
<td>GPIO[7]</td>
<td>76</td>
<td>Bidir</td>
<td>30</td>
</tr>
<tr>
<td>21</td>
<td>TEST4</td>
<td>77</td>
<td>Bidir</td>
<td>32</td>
</tr>
<tr>
<td>22</td>
<td></td>
<td></td>
<td>Internal</td>
<td>33</td>
</tr>
<tr>
<td>23</td>
<td>EECLK</td>
<td>99</td>
<td>Output2</td>
<td>34</td>
</tr>
<tr>
<td>24</td>
<td>EEYPD</td>
<td>98</td>
<td>Bidir</td>
<td>35</td>
</tr>
<tr>
<td>25</td>
<td>PERST_L</td>
<td>104</td>
<td>Input</td>
<td>36</td>
</tr>
<tr>
<td>26</td>
<td></td>
<td></td>
<td>Internal</td>
<td>37</td>
</tr>
<tr>
<td>27</td>
<td>MAIN_DETECT</td>
<td>24</td>
<td>Input</td>
<td>38</td>
</tr>
<tr>
<td>28</td>
<td></td>
<td></td>
<td>Internal</td>
<td>39</td>
</tr>
<tr>
<td>29</td>
<td></td>
<td></td>
<td>Internal</td>
<td>40</td>
</tr>
<tr>
<td>30</td>
<td></td>
<td></td>
<td>Internal</td>
<td>41</td>
</tr>
<tr>
<td>31</td>
<td></td>
<td></td>
<td>Bidir</td>
<td>4</td>
</tr>
<tr>
<td>Boundary Scan Register Number</td>
<td>Pin Name</td>
<td>Pin No</td>
<td>Type</td>
<td>Tri-state Control Cell</td>
</tr>
<tr>
<td>-------------------------------</td>
<td>-----------</td>
<td>--------</td>
<td>-------</td>
<td>------------------------</td>
</tr>
<tr>
<td>42</td>
<td>Internal</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>43</td>
<td>IO_HIT_I</td>
<td>3</td>
<td>Bidir</td>
<td>4</td>
</tr>
<tr>
<td>44</td>
<td>OCI[1]</td>
<td>4</td>
<td>Input</td>
<td></td>
</tr>
<tr>
<td>45</td>
<td>OCI[2]</td>
<td>5</td>
<td>Input</td>
<td></td>
</tr>
<tr>
<td>46</td>
<td>OCI[3]</td>
<td>6</td>
<td>Input</td>
<td></td>
</tr>
<tr>
<td>47</td>
<td>OCI[4]</td>
<td>7</td>
<td>Input</td>
<td></td>
</tr>
<tr>
<td>48</td>
<td>POE[1]</td>
<td>10</td>
<td>Bidir</td>
<td>4</td>
</tr>
<tr>
<td>49</td>
<td>POE[2]</td>
<td>11</td>
<td>Bidir</td>
<td>4</td>
</tr>
<tr>
<td>50</td>
<td>POE[3]</td>
<td>12</td>
<td>Bidir</td>
<td>4</td>
</tr>
<tr>
<td>51</td>
<td>POE[4]</td>
<td>13</td>
<td>Bidir</td>
<td>4</td>
</tr>
<tr>
<td>52</td>
<td>SMI_O</td>
<td>14</td>
<td>Bidir</td>
<td>4</td>
</tr>
<tr>
<td>53</td>
<td>Internal</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
10 POWER MANAGEMENT

10.1 PCI EXPRESS POWER STATES

The PI7C9X440SL implements a full set of PCI Express power management capabilities including full support for D0, D1, D2, D3-hot, and D3-cold Power States. The PCI Express Physical Link Layer of the PI7C9X440SL device supports the PCI Express Link Power Management with L0, L0s, L1, L2/L3 ready and L3 Power States.

During the transition from D3-hot to D3-cold state, the main power supplies of VDDC and VDDR are turned off to save power. PI7C9X440SL has been designed to have sticky registers that are powered by auxiliary power supplies. PI7C9X440SL forwards power management messages to the upstream Switches or root complex.

PI7C9X440SL also supports ASPM (Active State Power Management) to facilitate the link power saving and PME messaging.

10.2 USB POWER STATES

The EHCI Host Controller implements power management states compliant to PCI Bus Power Management Interface Specification, Revision 1.1 including D0, D1, D2, and D3-hot.

The OHCI Host Controller implements the following power states via the operational registers: USB_Reset, USB_Operational, USB_Suspend and USB_Resume. These states define the Host Controller’s responsibilities relating to USB signaling and bus states. The OHCI Host Controller asserts the Power Management Event signal (PME_L) whenever the power state is resumed to Operational State from Suspend State.
11 ELECTRICAL AND TIMING SPECIFICATIONS

11.1 ABSOLUTE MAXIMUM RATINGS

Table 11-1 Absolute Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

<table>
<thead>
<tr>
<th>Item</th>
<th>Absolute Max. Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Storage Temperature</td>
<td>-65°C to 150°C</td>
</tr>
<tr>
<td>Junction Temperature, TJ</td>
<td>125 °C</td>
</tr>
<tr>
<td>Digital core and analog supply voltage to ground potential (VDDC and AVDD)</td>
<td>-0.3v to 1.2v</td>
</tr>
<tr>
<td>Digital I/O and analog high supply voltage to ground potential (VDDR, VDDA and AVDDH)</td>
<td>-0.3v to 3.8v</td>
</tr>
<tr>
<td>DC input voltage for Digital I/O signals</td>
<td>-0.3v to 3.8v</td>
</tr>
</tbody>
</table>

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

11.2 Operating Ambient Temperature

Table 11-2 Operating Ambient Temperature

(Above which the useful life may be impaired.)

<table>
<thead>
<tr>
<th>Item</th>
<th>Low</th>
<th>High</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ambient Temperature with power applied</td>
<td>-40</td>
<td>85</td>
<td>°C</td>
</tr>
</tbody>
</table>

Note: Exposure to high temperature conditions for extended periods of time may affect reliability.

11.3 POWER CONSUMPTION

Table 11-3 PI7C9X440SL Power Dissipation

<table>
<thead>
<tr>
<th>Mode</th>
<th>Typical Power Dissipation (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>L0 Normal Mode</td>
<td>432</td>
</tr>
</tbody>
</table>

11.4 DC SPECIFICATIONS

Table 11-4 DC Electrical Characteristics

<table>
<thead>
<tr>
<th>Power Pins</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDC</td>
<td>0.9v</td>
<td>1.0v</td>
<td>1.1v</td>
</tr>
<tr>
<td>VDDR</td>
<td>3.0v</td>
<td>3.3v</td>
<td>3.6v</td>
</tr>
<tr>
<td>VDDA</td>
<td>3.0v</td>
<td>3.3v</td>
<td>3.6v</td>
</tr>
<tr>
<td>AVDD</td>
<td>0.95v</td>
<td>1.0v</td>
<td>1.1v</td>
</tr>
<tr>
<td>AVDDH</td>
<td>3.0v</td>
<td>3.3v</td>
<td>3.6v</td>
</tr>
</tbody>
</table>

VDCC: digital power supply for the core
VDDR: digital power supply for 3.3v I/O Interface
VDDA: analog power supply for 3.3v USB Interface
AVDD: analog power supply for 1.0v PCI Express Interface
AVDDH: analog power supply for 3.3v PCI Express Interface
### Table 11-5 DC Electrical Characteristics for Digital I/O

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{IH}</td>
<td>Input High Voltage</td>
<td>2.0V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{IL}</td>
<td>Input Low Voltage</td>
<td></td>
<td></td>
<td>0.8V</td>
</tr>
<tr>
<td>V_T</td>
<td>Threshold Point</td>
<td>1.29V</td>
<td>1.39V</td>
<td>1.49V</td>
</tr>
<tr>
<td>V_{TS}</td>
<td>Schmitt trig. Low to High Threshold Point</td>
<td>1.47V</td>
<td>1.61V</td>
<td>1.75V</td>
</tr>
<tr>
<td>V_{TP}</td>
<td>Schmitt trig. High to Low Threshold Point</td>
<td>0.99V</td>
<td>1.08V</td>
<td>1.18V</td>
</tr>
<tr>
<td>I_C</td>
<td>Input Leakage Current</td>
<td>±1uA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{OL}</td>
<td>Tri-State Output Leakage Current</td>
<td>±1uA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>P_{PU}</td>
<td>Pull-up Resistor</td>
<td>61kohm</td>
<td>75kohm</td>
<td>105kohm</td>
</tr>
<tr>
<td>P_{PD}</td>
<td>Pull-down Resistor</td>
<td>101kohm</td>
<td>199kohm</td>
<td>332kohm</td>
</tr>
<tr>
<td>V_{OL}</td>
<td>Output Low Voltage ( I_{OL} = 2.4 \text{mA} )</td>
<td></td>
<td></td>
<td>2.4V</td>
</tr>
<tr>
<td>V_{OH}</td>
<td>Output High Voltage ( I_{OL} = 2.4 \text{mA} )</td>
<td></td>
<td></td>
<td>2.4V</td>
</tr>
<tr>
<td>I_{OL}</td>
<td>Low Level Output Current ( V_{OL} ) = 0.4V</td>
<td>2.1mA</td>
<td>3.3mA</td>
<td>4.1mA</td>
</tr>
<tr>
<td></td>
<td>( V_{OL} ) = 0.4V</td>
<td>4mA</td>
<td>6.6mA</td>
<td>8.2mA</td>
</tr>
<tr>
<td>I_{OH}</td>
<td>High Level Output Current ( V_{OH} ) = 2.4V</td>
<td>2.8mA</td>
<td>6.1mA</td>
<td>9.9mA</td>
</tr>
<tr>
<td></td>
<td>( V_{OH} ) = 2.4V</td>
<td>4mA</td>
<td>12.2mA</td>
<td>19.8mA</td>
</tr>
</tbody>
</table>

### 11.5 AC SPECIFICATIONS

### Table 11-6 PCI Express Interface - Differential Transmitter (TX) Output Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unit Interval</td>
<td>UI</td>
<td>399.88</td>
<td>400.0</td>
<td>400.12</td>
<td>ps</td>
</tr>
<tr>
<td>Differential p-p TX voltage swing</td>
<td>V_{TX,DIFF-P-P}</td>
<td>800</td>
<td>-</td>
<td>-</td>
<td>mV</td>
</tr>
<tr>
<td>Lower power differential p-p TX voltage swing</td>
<td>V_{TX,DIFF-P-P,LOW}</td>
<td>400</td>
<td>-</td>
<td>-</td>
<td>mV</td>
</tr>
<tr>
<td>TX de-emphasis level ratio</td>
<td>V_{TX,DE-RATIO}</td>
<td>-3.0</td>
<td>-</td>
<td>-4.0</td>
<td>dB</td>
</tr>
<tr>
<td>Minimum TX eye width</td>
<td>T_{TX,EYE}</td>
<td>0.75</td>
<td>-</td>
<td>-</td>
<td>UI</td>
</tr>
<tr>
<td>Maximum time between the jitter median</td>
<td>T_{TX,EYE-MAX-JITTER}</td>
<td>-</td>
<td>-</td>
<td>0.125</td>
<td>UI</td>
</tr>
<tr>
<td>Transmitter rise and fall time</td>
<td>T_{TX,RISE-FALL}</td>
<td>0.125</td>
<td>-</td>
<td>-</td>
<td>UI</td>
</tr>
<tr>
<td>Maximum TX PLL Bandwidth</td>
<td>B_{W,TX,PLL}</td>
<td>-</td>
<td>-</td>
<td>22</td>
<td>MHz</td>
</tr>
<tr>
<td>Maximum TX PLL BW for 3db peaking</td>
<td>B_{W,TX,PLL-3DB}</td>
<td>1.5</td>
<td>-</td>
<td>-</td>
<td>MHz</td>
</tr>
<tr>
<td>Absolute Delta of DC Common Mode Voltage</td>
<td>V_{TX,CM-ACTIVE-IDLE-DELTA}</td>
<td>0</td>
<td>-</td>
<td>-</td>
<td>100</td>
</tr>
<tr>
<td>Absolute Delta of DC Common Mode Voltage</td>
<td>V_{TX,CM-LINE-DELTA}</td>
<td>0</td>
<td>-</td>
<td>-</td>
<td>25</td>
</tr>
<tr>
<td>Electrical Idle Differential Peak Output Voltage</td>
<td>V_{TX,DIFF-IDLE-AC-P}</td>
<td>0</td>
<td>-</td>
<td>-</td>
<td>20</td>
</tr>
<tr>
<td>The Amount of Voltage Change Allowed</td>
<td>V_{TX,VCV-DETECT}</td>
<td>-</td>
<td></td>
<td>-</td>
<td>600</td>
</tr>
<tr>
<td>Transmitter DC Common Mode Voltage</td>
<td>V_{TX,DC}</td>
<td>0</td>
<td>-</td>
<td>-</td>
<td>3.6</td>
</tr>
<tr>
<td>Transmitter Short-Circuit Current Limit</td>
<td>I_{TX,SHORT}</td>
<td>-</td>
<td>-</td>
<td>90</td>
<td>mA</td>
</tr>
<tr>
<td>DC Differential TX Impedance</td>
<td>Z_{TX,DIFF,DC}</td>
<td>80</td>
<td>100</td>
<td>120</td>
<td>Ω</td>
</tr>
<tr>
<td>Lane-to-Lane Output Skew</td>
<td>L_{TX,SKEW}</td>
<td>-</td>
<td>-</td>
<td>500 ps</td>
<td>+ 2 UI</td>
</tr>
</tbody>
</table>

### Table 11-7 PCI Express Interface - Differential Receiver (RX) Input Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unit Interval</td>
<td>UI</td>
<td>399.88</td>
<td>400.0</td>
<td>400.12</td>
<td>ps</td>
</tr>
<tr>
<td>Differential RX Peak-to-Peak Voltage</td>
<td>V_{RX,DIFF-PP-CC}</td>
<td>175</td>
<td>-</td>
<td>-</td>
<td>1200</td>
</tr>
<tr>
<td>Receiver eye time opening</td>
<td>T_{RX,EYE}</td>
<td>0.4</td>
<td>-</td>
<td>-</td>
<td>UI</td>
</tr>
<tr>
<td>Maximum time delta between median and deviation from median</td>
<td>T_{RX,EYE-MEDIAN-JITTER}</td>
<td>-</td>
<td>-</td>
<td>0.3</td>
<td>UI</td>
</tr>
<tr>
<td>Receiver DC common mode impedance</td>
<td>Z_{RX,DC}</td>
<td>40</td>
<td>-</td>
<td>-</td>
<td>60</td>
</tr>
<tr>
<td>DC differential impedance</td>
<td>Z_{RX,DIFF-DC}</td>
<td>80</td>
<td>-</td>
<td>-</td>
<td>120</td>
</tr>
<tr>
<td>RX AC Common Mode Voltage</td>
<td>Z_{RX,CM-AC-P}</td>
<td>-</td>
<td>-</td>
<td>150</td>
<td>mV</td>
</tr>
<tr>
<td>DC input CM input impedance during reset or power down</td>
<td>Z_{RX,HIGH-IMP-DC}</td>
<td>200</td>
<td>-</td>
<td>-</td>
<td>kΩ</td>
</tr>
</tbody>
</table>
### Table 11-8 USB Interface Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrical Idle Detect Threshold</td>
<td>( V_{RX-IDLE-DET-DIFFp-p} )</td>
<td>65</td>
<td>-</td>
<td>175</td>
<td>mV</td>
</tr>
<tr>
<td>Lane to Lane skew</td>
<td>( L_{RX-SKEW} )</td>
<td>-</td>
<td>-</td>
<td>20</td>
<td>ns</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Timing Characteristics</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{rise} )</td>
<td>1.5 Mbps</td>
<td>75</td>
<td>4</td>
<td>300</td>
<td>20 ns</td>
</tr>
<tr>
<td></td>
<td>12 Mbps</td>
<td>4</td>
<td>-</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>480 Mbps</td>
<td>0.5</td>
<td>-</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{fall} )</td>
<td>1.5 Mbps</td>
<td>75</td>
<td>4</td>
<td>300</td>
<td>20 ns</td>
</tr>
<tr>
<td></td>
<td>12 Mbps</td>
<td>0.5</td>
<td>-</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>480 Mbps</td>
<td>-</td>
<td>-</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>Jitter</td>
<td>1.5 Mbps</td>
<td>-</td>
<td>-</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>12 Mbps</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>480 Mbps</td>
<td>-</td>
<td>-</td>
<td>0.2</td>
<td></td>
</tr>
</tbody>
</table>

| **Electrical Characteristics**         |            |       |       |       |      |
| Vcm DC (DC level measured at receiver connector) | HS Mode | -0.05 | -     | 0.5   | V    |
|                                        | LS/FS Mode | 0.8   | 2.5   |       |      |
| Crossover Voltages                     | LS Mode    | 1.3   | -     | 2     | V    |
|                                        | FS Mode    | 1.3   | 2     |       |      |
| Power supply ripple noise              | \(< 1.2\text{MHz}\) | -10   | 0     | 10    | mV   |
| (Analog 3.3V)                          | \(> 1.2\text{MHz}\) | -50   | 0     | 50    | mV   |
| Power supply ripple noise              | All conditions | -50   | 0     | 50    | mV   |
| CORE (Digital Supply)                  |            |       |       |       |      |

| VBUS Comparators Voltage Thresholds    |            |       |       |       |      |
| A-Device Session Valid                | -          | 0.8   | -     | 2.0   | V    |
| B-Device Session Valid                | -          | 0.8   | -     | 4.0   | V    |
| B-Device Session End                  | -          | 0.2   | -     | 0.8   | V    |
| VBUS Valid                            | -          | 4.4   | -     | 4.75  | V    |

| **DC Levels**                          |            |       |       |       |      |
| LS Idle Voltage                        |            | 2.7   | 3.0   | 3.6   | V    |
| FS Idle Voltage                        |            | 2.7   | 3.0   | 3.6   | V    |
| HS Test K                              |            | -10.0 | 0.0   | 10.0  | mV   |
|                                        |            | 360   | 400   | 440   | mV   |
| HS Test J                              |            | -10.0 | 0.0   | 10.0  | mV   |
|                                        |            | 360   | 400   | 440   | mV   |
| HS Test SE0                            |            | -10.0 | 0.0   | 10.0  | mV   |
|                                        |            | 360   | 400   | 440   | mV   |

| **CHIRP Levels**                       |            |       |       |       |      |
| CHIRP 'J'                              |            | 700   | -     | 1100  | mV   |
| CHIRP 'K'                              |            | -900  | -     | -500  | mV   |
12 PACKAGE INFORMATION

The package of PI7C9X440SL is a 14mm x 14mm LQFP (128 Pin) package. The following are the package information and mechanical dimension:

---

**Figure 12-1 Package Outline Drawing**

**Figure 12-2 Part Marking**

---

**DESCRIPTION:** 128-pin Low Profile Quad Flat Package (LQFP)

**PACKAGE CODE:** FDE128

**DATE:** 12/11/14

**DESCRIPTION:** 128-pin Low Profile Quad Flat Package (LQFP)

**PACKAGE CODE:** FDE128

**DOCUMENT CONTROL #:** PD-2193

**REVISION:** --
### ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Temperature Range</th>
<th>Package</th>
<th>Pb-Free &amp; Green</th>
</tr>
</thead>
<tbody>
<tr>
<td>PI7C9X440SL□FDEX</td>
<td>-40° to 85°C (Industrial Temperature Range)</td>
<td>128-pin LQFP 14mm x 14mm</td>
<td>Yes</td>
</tr>
</tbody>
</table>

**Notes:**
1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
2. See http://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, “Green” and Lead-free.
3. Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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**PI 7C 9X440SL □ FD E X**

- **Tape & Reel**
- **Pb-Free and Green**
- **Package Code**
  - Blank=Standard
  - □=Revision
- **Device Type**
- **Device Number**
- **Family**
- **Pericom**