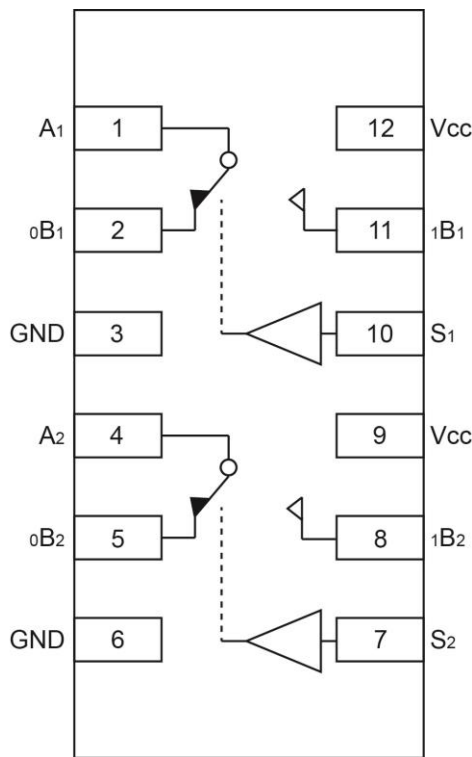


**Low Voltage Dual SPDT Analog Switch 2:1 Mux/Demux Bus Switch**

**Features**

- ➔ CMOS Technology for Bus and Analog Applications
- ➔ Low On-Resistance: 8Ω at 3.0V
- ➔ Wide V<sub>CC</sub> Range: 1.65V to 5.5V
- ➔ Rail-to-Rail Signal Range
- ➔ Control Input Overvoltage Tolerance: 5.5V(Min)
- ➔ Fast Transition Speed: 2ns at 5.0V
- ➔ High Off Isolation: -63dB @ 10MHz
- ➔ Break-Before-Make Switching
- ➔ High Bandwidth: 350MHz
- ➔ Extended Industrial Temperature Range:  
-40°C to 85°C
- ➔ Packaging (Lead Free & Green):
  - -12-pin TDFN, 3mm×1mm

**Pin Assignment**



**12-pin TDFN**

**Description**

The PI5A3158B is a dual high-bandwidth, fast single-pole double-throw (SPDT) CMOS switch. It can be used as an analog switch or as a low-delay bus switch. Specified over a wide operating power supply voltage range, 1.65V to 5.5V, the PI5A3158B has a maximum ON resistance of 12-ohms at 1.65V, 9-ohms at 2.3V & 6-ohms at 4.5V.

Break-before-make switching prevents both switches being enabled simultaneously. This eliminates signal disruption during switching.

The control input, S, is independent of supply voltage.

**Application**

- ➔ Cell Phones
- ➔ PDAs
- ➔ MP3 Players
- ➔ Portable Instrumentation
- ➔ Battery powered Communications
- ➔ Computer Peripherals

**Pin Description**

Pin No	Name	Description
8, 11	<sub>1</sub> B <sub>X</sub>	Data Port (Normally open)
3, 6	GND	Ground
2, 5	<sub>0</sub> B <sub>X</sub>	Data Port (Normally closed)
1, 4	A <sub>X</sub>	Common Output / Data Port
9, 12	V <sub>CC</sub>	Positive Power Supply
7, 10	S <sub>X</sub>	Logic Control

**Logic Function Table**

Logic Input (S <sub>X</sub> )	Function
0	<sub>0</sub> B <sub>X</sub> Connected to A <sub>X</sub>
1	<sub>1</sub> B <sub>X</sub> Connected to A <sub>X</sub>

Note: x = 1 or 2

## Maximum Ratings

Storage Temperature.....	-65°C to +150°C
Ambient Temperature with Power Applied.....	-40°C to +85°C
Supply Voltage $V_{CC}$ .....	-0.5V to +7.0V
DC Switch Voltage $V_{IN}$ .....	-0.5V to $V_{CC}+0.5V$
Control Input Voltage $V_S$ .....	-0.5V to +7.0V
DC Output Current $V_{OUT}$ .....	128mA
DC $V_{CC}$ or Ground Current $I_{CC} / I_{GND}$ .....	$\pm 100mA$
Junction Temperature under Bias ( $T_J$ ) .....	150°C
Junction Lead Temperature (TL) (Soldering, 10 seconds) .....	260°C
Power Dissipation (Pd) @ +85°C .....	180mW
ESD(HBM).....	2000V

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{CC}$	Operating Voltage	-	1.65	-	5.5	V
$V_S$	Control Input Voltage	-	0	-	5.5	V
$V_{IN}$	Switch Input Voltage	-	0	-	$V_{CC}$	V
$V_{OUT}$	Output Voltage	-	0	-	$V_{CC}$	V
$T_A$	Operating Temperature	-	-40	25	85	°C
$t_r, t_f$	Input Rise and Fall Time	Control Input $V_{CC} = 2.3V - 3.6V$	0	-	10	ns/V
		Control Input $V_{CC} = 4.5V - 5.5V$	0	-	5	ns/V

Note: Control input must be held HIGH or LOW; it must not float.

## DC Electrical Characteristics

 (T<sub>A</sub> = -40°C to 85°C, unless otherwise noted.)

Parameter	Description	Test Conditions	Temperature (T <sub>A</sub> :°C)	Min.	Typ.	Max.	Units
V <sub>IAR</sub>	Analog Input Signal Range	V <sub>CC</sub>	-40°C to 85°C	0	-	V <sub>CC</sub>	V
R <sub>ON</sub>	ON Resistance <sup>(1)</sup>	V <sub>CC</sub> =4.5V, I <sub>O</sub> = 30mA, V <sub>IN</sub> = 0V	25°C	-	4	6	Ω
		V <sub>CC</sub> =4.5V, I <sub>O</sub> =-30mA, V <sub>IN</sub> =2.4V		-	5	8	
		V <sub>CC</sub> =4.5V, I <sub>O</sub> =-30mA, V <sub>IN</sub> =4.5V		-	7	11	
		V <sub>CC</sub> =4.5V, I <sub>O</sub> = 30mA, V <sub>IN</sub> = 0V	-40°C to 85°C	-	-	6	
		V <sub>CC</sub> =4.5V, I <sub>O</sub> =-30mA, V <sub>IN</sub> =2.4V		-	-	8	
		V <sub>CC</sub> =4.5V, I <sub>O</sub> =-30mA, V <sub>IN</sub> =4.5V		-	-	11	
		V <sub>CC</sub> =3.0V, I <sub>O</sub> = 24mA, V <sub>IN</sub> = 0V	25°C	-	5	8	
		V <sub>CC</sub> =3.0V, I <sub>O</sub> =-24mA, V <sub>IN</sub> =3.0V		-	10	15	
		V <sub>CC</sub> =3.0V, I <sub>O</sub> = 24mA, V <sub>IN</sub> = 0V		-40°C to 85°C	-	-	
		V <sub>CC</sub> =3.0V, I <sub>O</sub> =-24mA, V <sub>IN</sub> =3.0V	-		-	15	
		V <sub>CC</sub> =2.3V, I <sub>O</sub> = 8mA, V <sub>IN</sub> = 0V	25°C		-	6	
		V <sub>CC</sub> =2.3V, I <sub>O</sub> =-8mA, V <sub>IN</sub> =2.3V		-	13	20	
		V <sub>CC</sub> =2.3V, I <sub>O</sub> = 8mA, V <sub>IN</sub> = 0V		-40°C to 85°C	-	-	
		V <sub>CC</sub> =2.3V, I <sub>O</sub> =-8mA, V <sub>IN</sub> =2.3V	-		-	20	
		V <sub>CC</sub> =1.65V, I <sub>O</sub> = 4mA, V <sub>IN</sub> = 0V	25°C		-	8	
		V <sub>CC</sub> =1.65V, I <sub>O</sub> =-4mA, V <sub>IN</sub> =1.65V		-	20	30	
V <sub>CC</sub> =1.65V, I <sub>O</sub> = 4mA, V <sub>IN</sub> = 0V	-40°C to 85°C	-		-	12		
V <sub>CC</sub> =1.65V, I <sub>O</sub> =-4mA, V <sub>IN</sub> =1.65V		-	-	25			
ΔR <sub>ON</sub>		ON Resistance Match Between Channels <sup>(1,2,3)</sup>	V <sub>CC</sub> =4.5V, I <sub>A</sub> =-30mA, V <sub>Bn</sub> =3.15V	25°C	-	0.15	-
	V <sub>CC</sub> =3.0V, I <sub>A</sub> =-24mA, V <sub>Bn</sub> =2.1V		-		0.2	-	
	V <sub>CC</sub> =2.3V, I <sub>A</sub> =-8mA, V <sub>Bn</sub> =1.6V		-		0.3	-	
	V <sub>CC</sub> =1.65V, I <sub>A</sub> =-4mA, V <sub>Bn</sub> =1.15V		-		0.5	-	
R <sub>ONF</sub>	ON Resistance Flatness (1,2,4)	V <sub>CC</sub> =5.0V, I <sub>A</sub> =-30mA, 0≤V <sub>Bn</sub> ≤V <sub>CC</sub>	25°C	-	6	-	Ω
		V <sub>CC</sub> =3.3V, I <sub>A</sub> =-24mA, 0≤V <sub>Bn</sub> ≤V <sub>CC</sub>		-	12	-	
		V <sub>CC</sub> =2.5V, I <sub>A</sub> =-8mA, 0≤V <sub>Bn</sub> ≤V <sub>CC</sub>		-	22	-	
		V <sub>CC</sub> =1.8V, I <sub>A</sub> =-4mA, 0≤V <sub>Bn</sub> ≤V <sub>CC</sub>		-	90	-	
V <sub>IH</sub>	Input High Voltage (Logic High Level)	V <sub>CC</sub> =1.65V	-40°C to 85°C	1	-	-	V
		V <sub>CC</sub> = 2.3V		1.2	-	-	
		V <sub>CC</sub> = 3V		1.3	-	-	
		V <sub>CC</sub> = 4.2V		1.5	-	-	
		V <sub>CC</sub> = 5.5V		1.8	-	-	
V <sub>IL</sub>	Input Low Voltage (Logic Low Level)	V <sub>CC</sub> =1.65V	-40°C to 85°C	-	-	0.4	V
		V <sub>CC</sub> = 2.3V		-	-	0.6	
		V <sub>CC</sub> = 3V		-	-	0.8	
		V <sub>CC</sub> = 4.2V		-	-	1	
		V <sub>CC</sub> = 5.5V		-	-	1.2	
I <sub>LKC</sub>	Input Leakage Current	0≤V <sub>IN</sub> ≤5.5V, V <sub>CC</sub> =0V to 5.5V	25°C	-	-	±0.1	μA
			-40°C to 85°C	-	-	±1.0	
I <sub>OFF</sub>	OFF State Leakage Current	0≤V <sub>IN</sub> ≤5.5V, V <sub>CC</sub> =1.65V to 5.5V	25°C	-	-	±0.1	μA
			-40°C to 85°C	-	-	±10	
I <sub>CC</sub>	Quiescent Supply Current	All channels ON or OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND, I <sub>OUT</sub> =0, V <sub>CC</sub> = 5.5V	25°C	-	-	1	μA
			-40°C to 85°C	-	-	5	

### Notes:

- Measured by voltage drop between A and B pins at the indicated current through the device. ON resistance is determined by the lower of the voltages on two ports (A or B).
- Parameter is characterized but not tested in production.
- DR<sub>ON</sub> = R<sub>ON</sub> max – R<sub>ON</sub> min. measured at identical V<sub>CC</sub>, temperature and voltage levels.
- Flatness is defined as difference between maximum and minimum value of ON resistance over the specified range of conditions. Guaranteed by design.

## Capacitance <sup>(1)</sup>

(T<sub>A</sub> = 25°C, unless otherwise noted.)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
C <sub>IN</sub>	Control Input	V <sub>CC</sub> = 5.0V	-	2.5	-	pF
C <sub>IO-B</sub>	For B Port, Switch OFF	V <sub>CC</sub> = 5.0V, f = 1 MHz <sup>(1)</sup>	-	5.0	-	
C <sub>IOA-ON</sub>	For A Port, Switch ON		-	15.0	-	

### Notes:

1. Capacitance is characterized but not tested in production

## Switch and AC Characteristics <sup>(1)</sup>

Parameter	Description	Test Conditions	Supply Voltage	Temperature (T <sub>A</sub> : °C)	Min.	Typ.	Max.	Units	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay: A to Bn	See test circuit diagrams 1 and 2. V <sub>I</sub> Open <sup>(2)</sup>	V <sub>CC</sub> = 2.3V to 2.7V V <sub>CC</sub> = 3.0V to 3.6V V <sub>CC</sub> = 4.5V to 5.5V	-40 to 85°C	-	0.7	-	ns	
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Turn ON Time: A to Bn	See test circuit diagrams 1 & 2. V <sub>I</sub> = 2V <sub>CC</sub> for t <sub>PZL</sub> , V <sub>I</sub> = 0V for t <sub>PZH</sub>	V <sub>CC</sub> = 1.65V to 1.95V V <sub>CC</sub> = 2.3V to 2.7V V <sub>CC</sub> = 3.0V to 3.6V V <sub>CC</sub> = 4.5V to 5.5V	-40 to 85°C	-	9	-		
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Turn OFF Time: A to Bn	See test circuit diagrams 1 and 2. V <sub>I</sub> = 2V <sub>CC</sub> for t <sub>PLZ</sub> , V <sub>I</sub> = 0V for t <sub>PHZ</sub>	V <sub>CC</sub> = 1.65V to 1.95V V <sub>CC</sub> = 2.3V to 2.7V V <sub>CC</sub> = 3.0V to 3.6V V <sub>CC</sub> = 4.5V to 5.5V	-40 to 85°C	-	9	-		
t <sub>BM</sub>	Break Before Make Time	See test circuit diagram 3.	V <sub>CC</sub> = 1.65V to 1.95V V <sub>CC</sub> = 2.3V to 2.7V V <sub>CC</sub> = 3.0V to 3.6V V <sub>CC</sub> = 4.5V to 5.5V	-40 to 85°C	0.5	-	-		
Q	Charge Injection	C <sub>L</sub> = 0.1nF, V <sub>GEN</sub> = 0V, R <sub>GEN</sub> = 0Ω See test circuit 4.	V <sub>CC</sub> = 5.0V V <sub>CC</sub> = 3.3V	25°C	-	5	-		pC
OIRR	Off Isolation	R <sub>L</sub> = 50Ω, V <sub>GEN</sub> = 0V, R <sub>GEN</sub> = 0Ω, f = 10MHz. See test circuit 5. <sup>(3)</sup>	V <sub>CC</sub> = 1.65V to 5.5V	25°C	-	-63	-		dB
X <sub>TALK</sub>	Crosstalk Isolation	See test circuit 6. <sup>(4)</sup>	V <sub>CC</sub> = 1.65V to 5.5V	25°C	-	-64	-		
f <sub>3dB</sub>	-3dB Bandwidth	See test circuit 9	V <sub>CC</sub> = 1.65V to 5.5V	25°C	-	350	-		MHz

### Notes:

- Guaranteed by design.
- The device contributes no other propagation delay other than the RC delay of the switch ON resistance and the 50pF load capacitance, when driven by an ideal voltage source with zero output impedance.
- Off Isolation = 20 Log<sub>10</sub> [ V<sub>Bn</sub>/V<sub>A</sub> ] and is measured in dB.
- Crosstalk Isolation = 20 Log<sub>10</sub> [ V<sub>B1</sub>/V<sub>B0</sub> ] and is measured in dB.

**Test Circuits and Timing Diagrams**

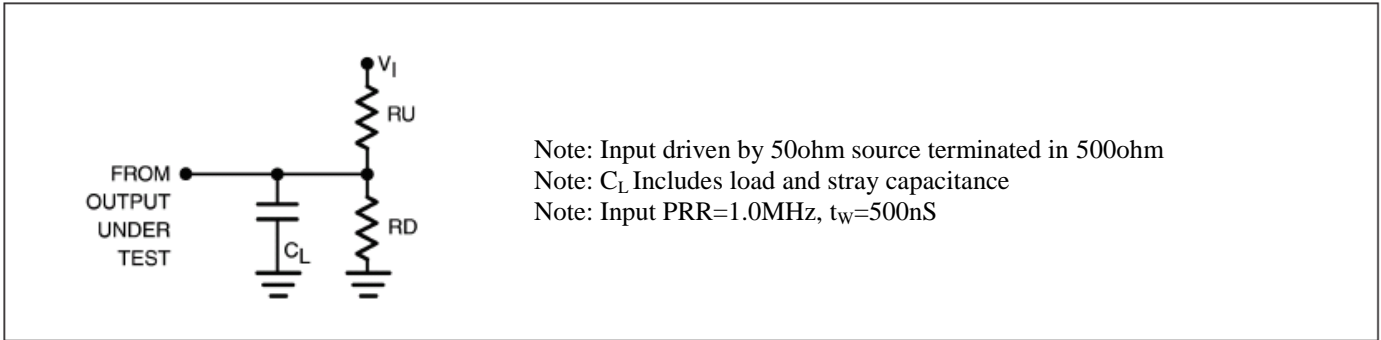


Figure 1. AC Test Circuit

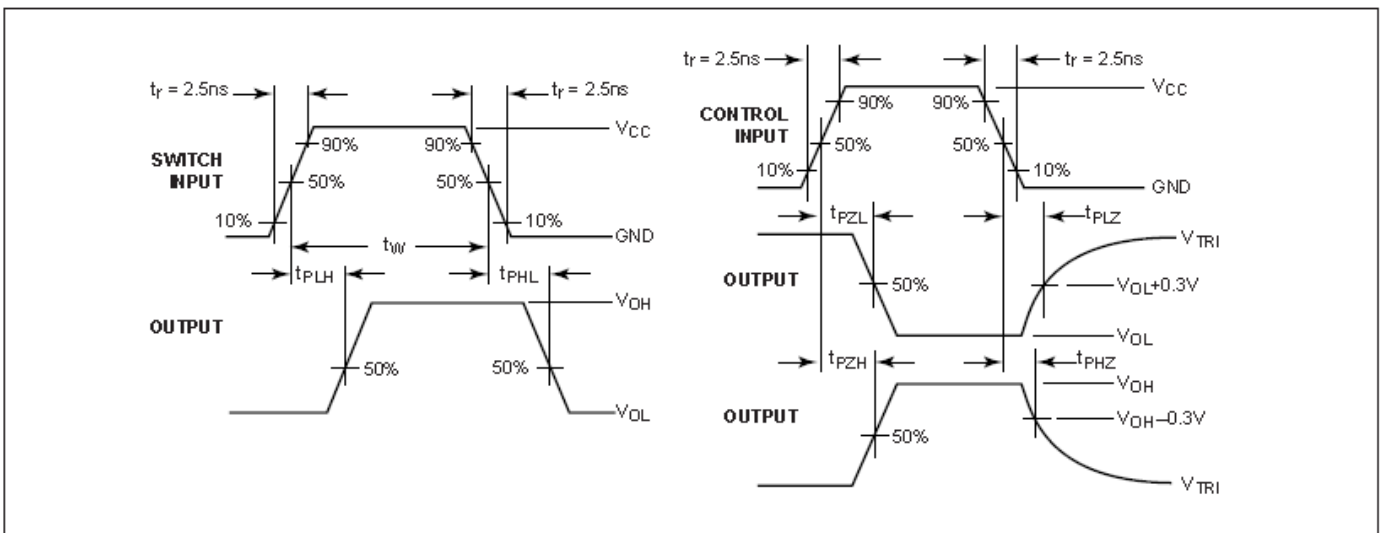


Figure 2. AC Waveforms

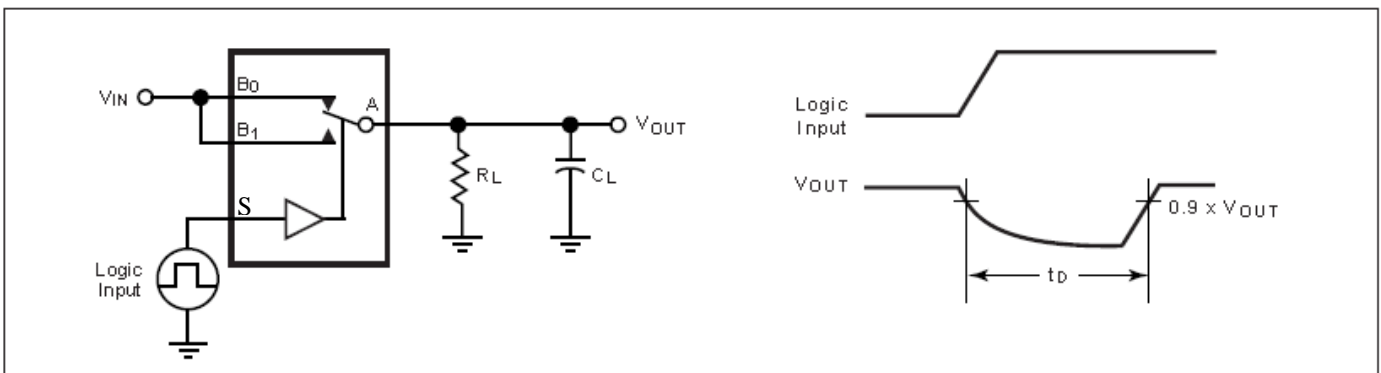
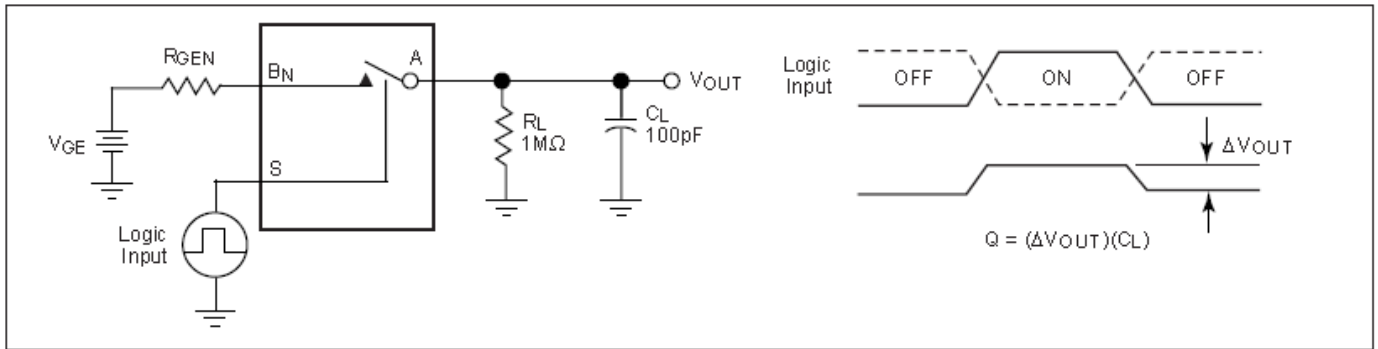
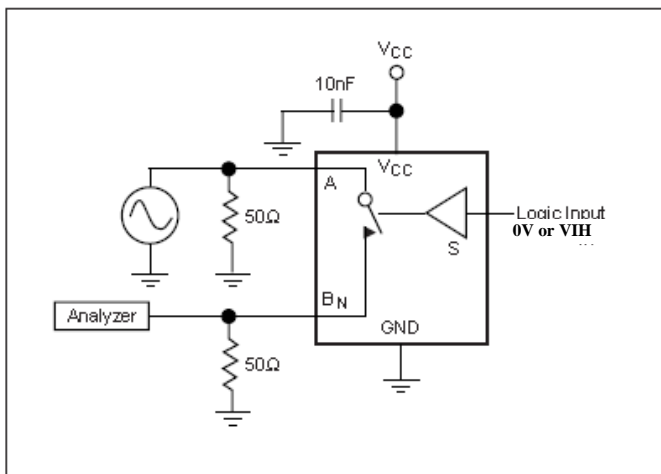


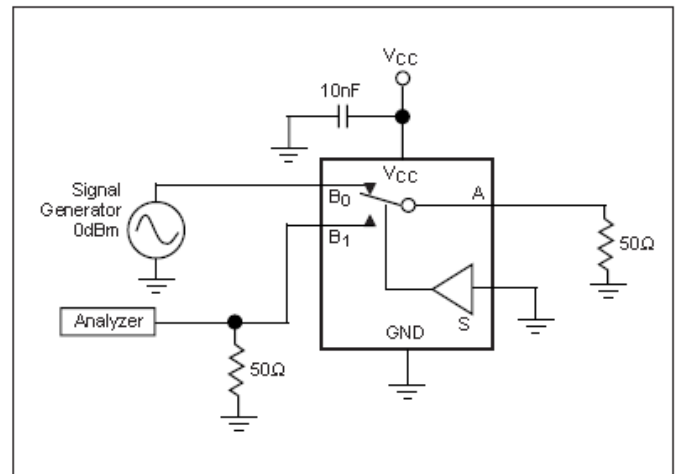
Figure 3. Break Before Make Interval Timing



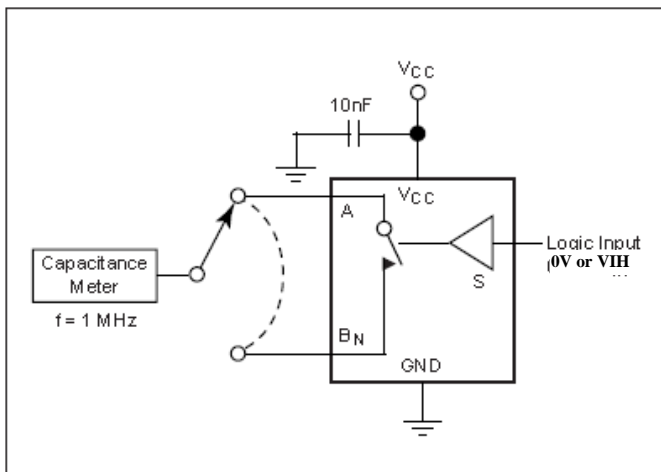
**Figure 4. Charge Injection Test**



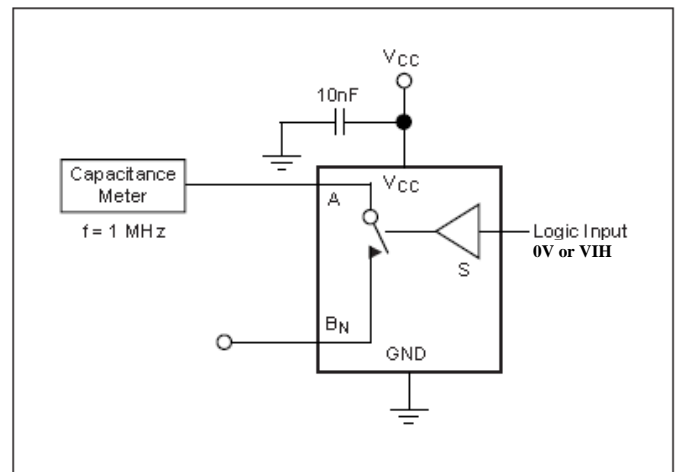
**Figure 5. Off Isolation**



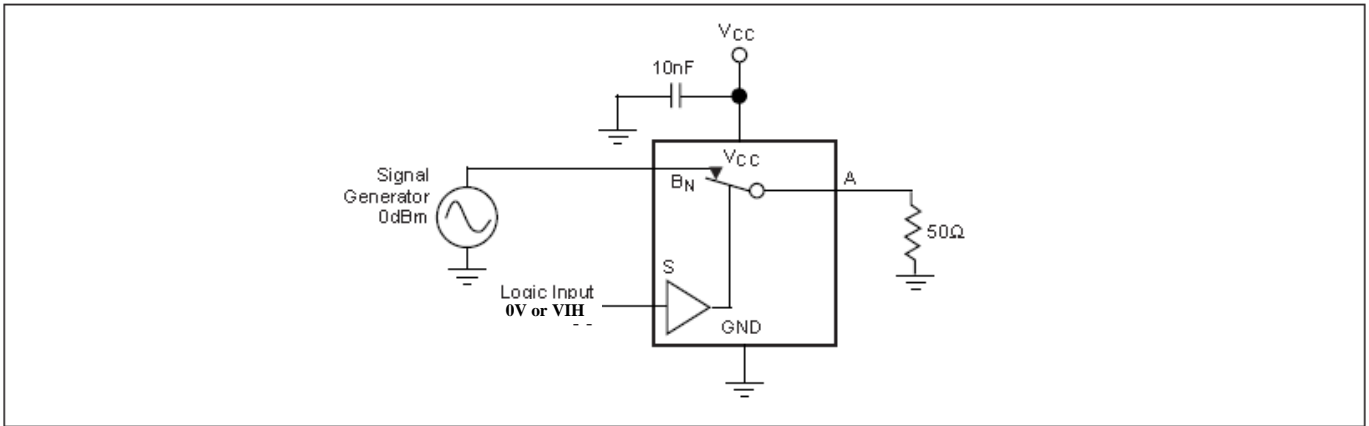
**Figure 6. Crosstalk**



**Figure 7. Channel Off Capacitance**



**Figure 8. Channel On Capacitance**



**Figure 9. Bandwidth**

**Part Marking**

ZA Package

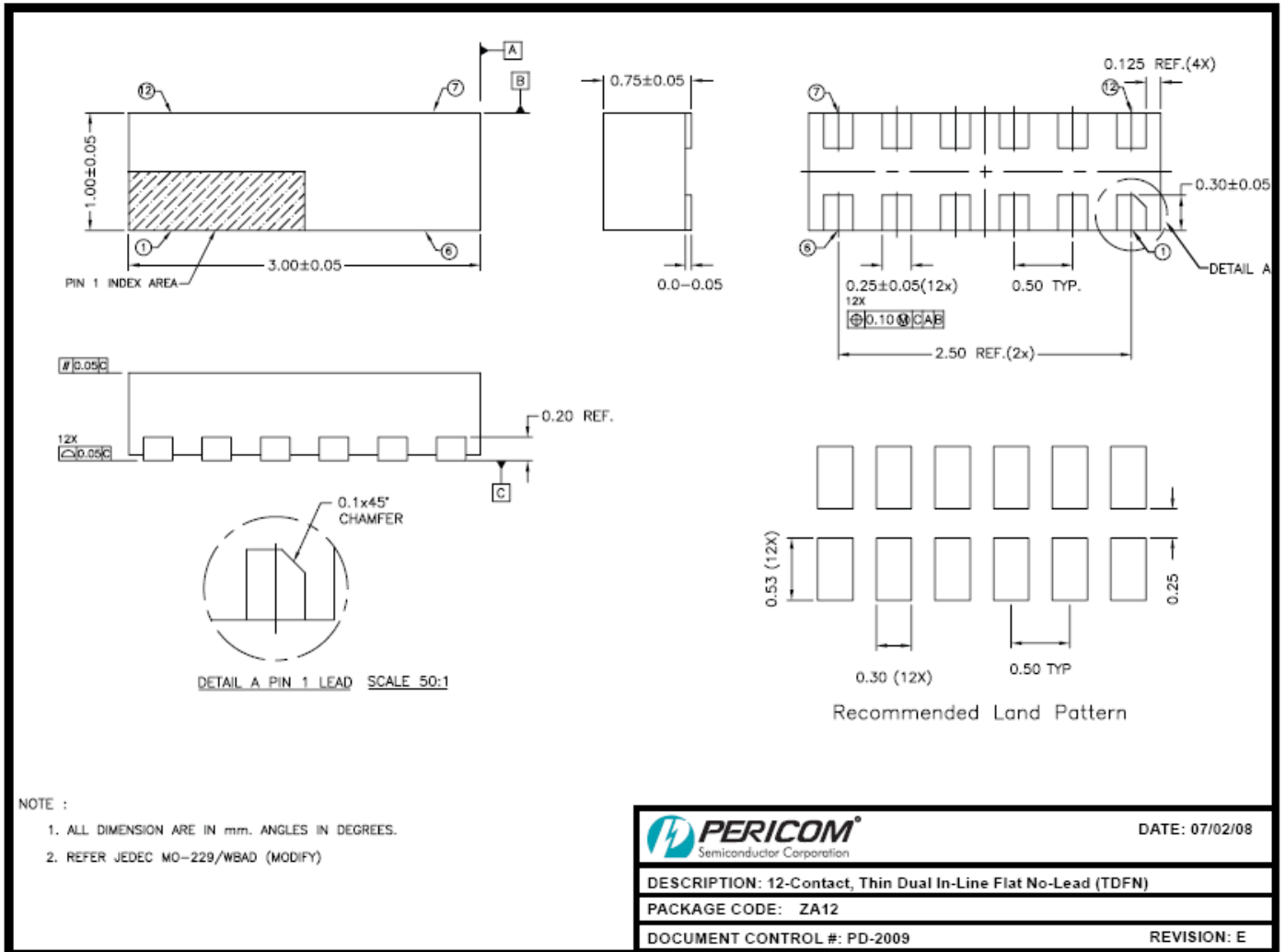


XX: Date Code (Year & Work Week)

kE: PI5A3158BZAE

**Packaging Mechanical**

**12-TDFN (ZA)**



For latest package info.

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**Ordering Information**

Part Number	Package Code	Package	Top Marking
PI5A3158BZAEX	ZA	12-Contact, Thin Dual In-Line Flat No-Lead (TDFN)	kE

**Notes:**

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <http://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Thermal characteristics can be found on the company web site at [www.diodes.com/design/support/packaging/](http://www.diodes.com/design/support/packaging/)
4. E = Pb-free and Green
5. X suffix = Tape/Reel



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