A Product Line of
Diodes Incorporated

PI3HDX231

3:1 HDMI 1.4/2.0 Switch with Linear ReDriver and I2C Control

Description

The DIODES™ PI3HDX231 is the HDMI 2.0 Linear ReDriver™ 3:1 Switch, supporting Data rate 6 Gbps per channel with 4096 x 2160 pixel resolution, color 12-bit YCbCr 4:2:2 format. Diodes Linear ReDriver technology can provide 2 times improved Jitter performance and the component placement flexibility between the source and sink devices. Non-blocking Channel link transparency can provide the mode setting easiness for Signal Integrity adjustment.

It works as a part of the signal conditioning ecosystem, designed to aid in the transmission and Digital Feedback Equalization (DFE) reception of high-speed digital signals.

It has both Pin and I2C programming mode for Ports selection, programmable termination resistors, Squelch detection for idle mode, DDC Switch and input/output voltage level selection.

Features

- HDMI 2.0 standard compliant Linear ReDriver Switch with 6Gbps data rate
- I2C control 3:1 TMDS Ports switching
- Supports DC-coupled TMDS or AC-coupled DP++ Differential input signals for DP++ Level Shifter application
- Supports Input Equalizer, Flat Gain and Voltage Swing control independently to achieve optimized HDMI signal integrity
- Linear ReDriver delivers 2x Improved Additive Jitter than ReDriver CMOS technology
- Improve TMDS Link Margin with receiver-side DFE (Decision Feedback Equalizers) as a part of signal conditioning ecosystem
- Input Clock Detection(squelch) for auto power-down mode
- Selectable Active Buffer or Passive DDC switch with DDC VOL/VIL adjustment
- Programmable Receiver and Driver block termination resistors
- Standby current <50uA when all three ports are off by port selection control or HPD_SINK = 0 condition
- Power supply: 3.3V
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/
- Package (Pb-Free & Green): 72-pin, TQFN (ZL)

Applications

- HDMI Peripheral Switch Box
- TV, Monitor and AIO PCs

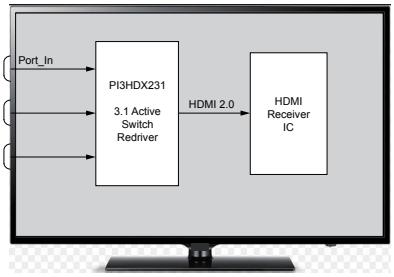


Figure 1. HDMI 2.0 Switching in TV/Monitor

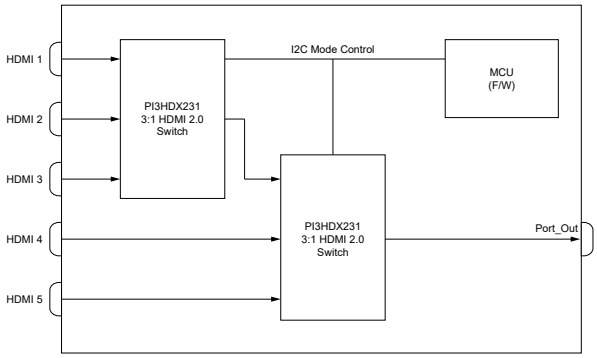


Figure 2. HDMI 2.0 Switch Box

Ordering Information

Ordering Number	Package Code	Package Description
PI3HDX231ZLEX	ZL	72-contact, Very Thin Quad Flat No-Lead (TQFN)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

Revision History

Date	Revision	Description of Changes
July 2016	-	Preliminary DS release
October 2016	-	Pin Description Typo fixed and add SVDD description in the Block Diagram
December 2016	-	Add ES sample Errata
April 2017	-	Changed I2C control registers: Byte 0x00 bit 4 as reserved. bit 2 : Squelch control, Byte 0x06 Bit [7:6] : reserved
June 2017	-	SVDD changed to VDD for reliability improvement. DDC Source channel requires MOSFET for 5V tolerance support, and updated Application Schematics.
August 2017	1	Electrical spec items unrelated for HDMI application were removed. DDC Vilc application added in Application session. Removed ES sample Errata
March 2022	2	Removed Industrial Temperature Removed Section SiGe vs. CMOS Redrivers Jitter performance Removed Section EQ/FG/SW Channel Output Measurement (Informative) Updated Official Diodes' Format Updated Trademark for ReDriver Updated Pin Description Updated Figure HDMI 2.0 Switch Box Updated Figure HDMI 2.0 Switch 5:1 Application Block Diagram Updated Figure HDMI Sink-side Application with I2C mode switching control Updated Figure HDMI Sink Application in Pin mode Updated Figure HDMI Switch Application in I2C mode

Contents

2. Pin Configuration

2.1 Package Pin-out

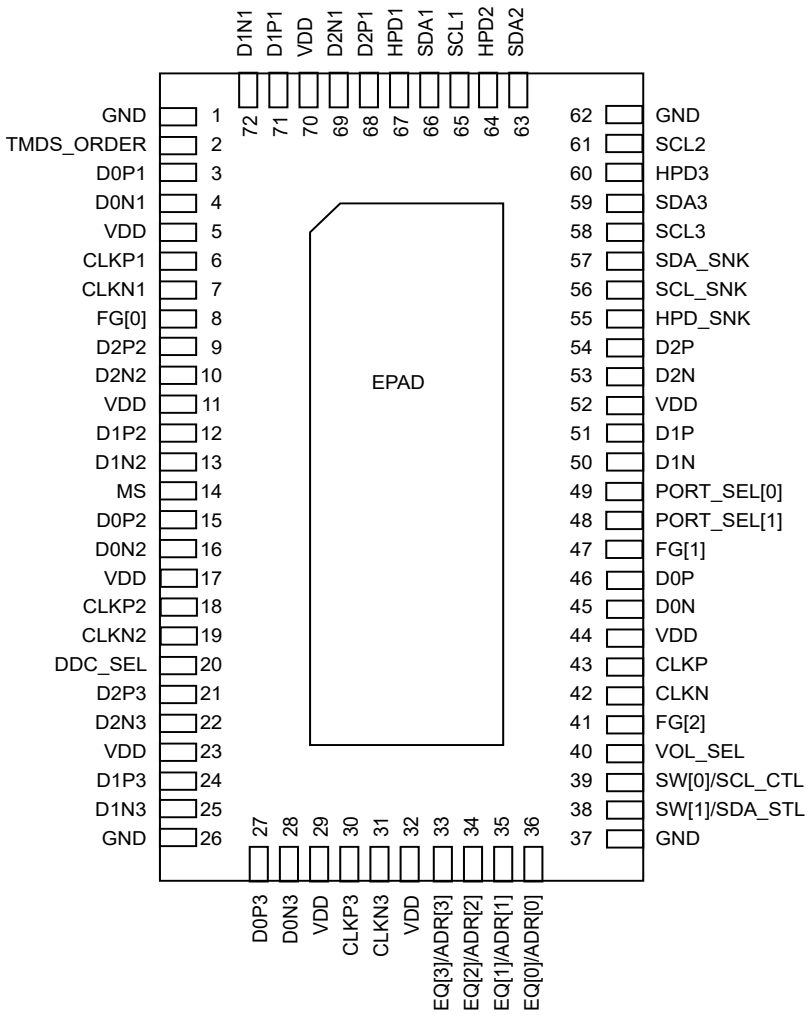


Figure 2-1 72-pin Package Pin-out

Note: In TMDS Data and Clock Differential Pairs of Input and Output, the polarity (+/- or P/N) of each pairs and high-speed data channels A[3:0] can use inter-changeably. Output pins of polarity and data channel will always follow the input polarity and data channel assignment changes.

2.2 Pin Description

Pin Name	Pin #	Type	Description
D[2:0]P1/N1	3, 4, 72, 71, 69, 68	I	Port 1 TMDS Positive/Negative inputs
CLKP1/N1	6, 7	I	Port 1 TMDS Positive/Negative inputs
D[2:0]P2/N2	15, 16, 12, 13, 9, 10	I	Port 2 TMDS Positive/Negative inputs
CLKP2/N2	18, 19	I	Port 2 TMDS Positive/Negative inputs
D[2:0]P/N3	27, 28, 24, 25, 21, 22	I	Port 3 TMDS Positive/Negative inputs
CLKP3/N3	30, 31	I	Port 3 TMDS Positive/Negative inputs
D[2:0]P/N	46, 45, 51, 50, 54, 53	O	TMDS positive outputs
CLKP/N	43, 42	O	TMDS positive outputs
HPD1	67	O	Port 1 HPD output
SDA1	66	I/O	Port 1 DDC Data
SCL1	65	I/O	Port 1 DDC Clock
HPD2	64	O	Port 2 HPD output
SDA2	63	I/O	Port 2 DDC Data
SCL2	61	I/O	Port 2 DDC Clock
HPD3	60	O	Port 3 HPD output
HPD_SNK	55	I	Sink side hot plug detector input. High: 5-V power signal asserted from source to sink and EDID is ready. Low: No 5-V power signal asserted from source to sink, or EDID is not ready.
SDA_SNK	57	I/O	Sink Side DDC Data
SCL_SNK	56	I/O	Sink Side DDC Clock
SDA3	59	I/O	Port 3 DDC Data
SCL3	58	I/O	Port 3 DDC Clock
TMDS_ORDER	2	I	TMDS order selectable control with default pull-high. Tie to VDD or float, they are D2/D1/D0/CLK (default) Tie to GND, they are CLK/D0/D1/D2.
MS	14	I	Mode selection pin. Internal pull-up with 100kΩ. 0: Pin Control Mode 1: I2C Control Mode
DDC_SEL	20	I	DDC buffer or passive switch control with default pull high. When tie to VDD or float, it is passive switch, when tie to GND, it is active buffer.
EQ[3]/ADR[3]	33	I	TMDS input equalization selection in all channels when MS=0. See truth table for EQ setting. I2C address PIN when MS=1
EQ[2]/ADR[2]	34	I	
EQ[1]/ADR[1]	35	I	
EQ[0]/ADR[0]	36	I	
SW[1]/SDA_STL	38	I	TMDS output voltage level selection in all channels when MS=0. See truth table for swing setting. I2C interface when MS=1
SW[0]/SCL_STL	39	I	

Pin Name	Pin #	Type	Description
VOL_SEL	40	I	DDC sink side VOL,VILC value select. Internal pull high to VDD. Low:. VOL=0.525V, VILC=0.425V High: VOL=0.75V, VILC=0.6V
FG[2]	41	I	TMDS output flatten gain level selection in all channels when MS=0. See truth table for FG setting.
FG[1]	47	I	
FG[0]	8	I	
PORT_SEL[1]	48	I	Port selection when MS=0. Port_sel[1:0] 00 port1 select 01 port2 select 10 port3 select 11 shut down all port
PORT_SEL[0]	49		
V_{DD}	5, 11, 17, 23, 29, 32, 44, 52, 70	P	3.3V Power Supply
GND	1, 26, 37, 62	G	Ground
EPAD	EPAD	G	Ground

3. Functional

3.1 Functional Block

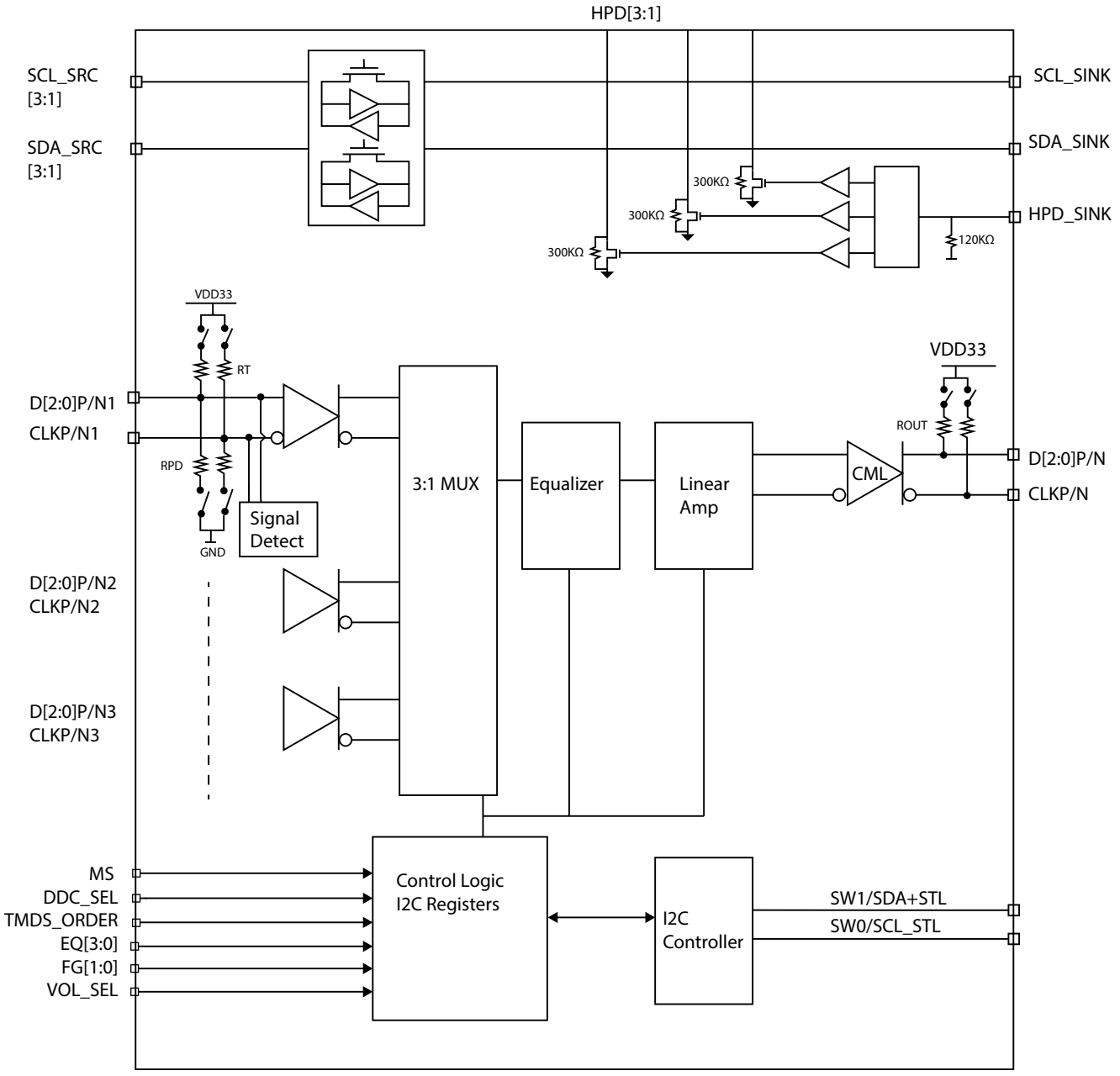


Figure 3-1 Functional Block Diagram

3.2 Control Signal Truth Table

3.2.1 Pin or I2C Control Mode Selection MS Pin

MS	Operation
0	Pin control mode
1	I2C control mode (Default)

Note: Internal pull high

3.2.2 DDC Active Buffer, Switch Selection DDC_SEL Pin

DDC_SEL	Operation
0	Active buffer
1	Passive switch (Default)

Note: internal pull high

3.2.3 DDC Sink-side Output and Input Voltage Selection VOL_SEL Pin

VOL_SEL	VOL	VILC
0	0.525V	0.425V
1	0.75V	0.6V

Note: Intern pull high

3.2.4 TMDS Order Swap Control Pin

TMDS_ORDER	Operation
0	CLK/D0/D1/D2 order
1	D2/D1/D0/CLK order (Default)

Note: internal pull high

3.2.5 Input Equalization Setting

The EQ[3:0] pins are the pin-strap mode for each high-speed channels EQ control. Equalization can be controlled independently, configuration registers programmable by I2C mode.
In pin mode, Equalization setting apply same value for all 3 Data and 1 Clock channels.

Table 3-1. Equalization Setting

EQ3	EQ2	EQ1	EQ0	@ 3GHz	@ 4GHz
0	0	0	0	3.5	4.6
0	0	0	1	4.3	5.8
0	0	1	0	5.1	6.8
0	0	1	1	5.9	7.8
0	1	0	0	7.1	9.1
0	1	0	1	7.8	9.9
0	1	1	0	9.1	11.3
0	1	1	1	10.3	12.6
1	0	0	0	11.7	14.0
1	0	0	1	12.6	14.9
1	0	1	0	13.4	15.7
1	0	1	1	14.5	16.8
1	1	0	0	15.6	17.8
1	1	0	1	16.4	18.5
1	1	1	0	17.1	19.1
1	1	1	1	17.7	19.6

3.2.6 Flat Gain Setting

FG[2:0] pins are the selection of the DC Flat Gain value.

Table 3-2. Flat Gain FG[2:0] Control

FG2	FG1	FG0	dB
0	0	0	-3.5
0	0	1	-2.0
0	1	0	-0.5
0	1	1	0.5
1	0	0	1.5
1	0	1	2.5
1	1	0	4.0
1	1	1	6.0

3.2.7 Voltage Swing Setting

SW[1:0] affects the linearity of the output signal swing when input amplitude changes.

Table 3-3. SW[1:0] Output Swing Setting

SW1	SW0	mVp-p
0	0	800
0	1	900
1	0	1000
1	1	1100

3.3 Function Description

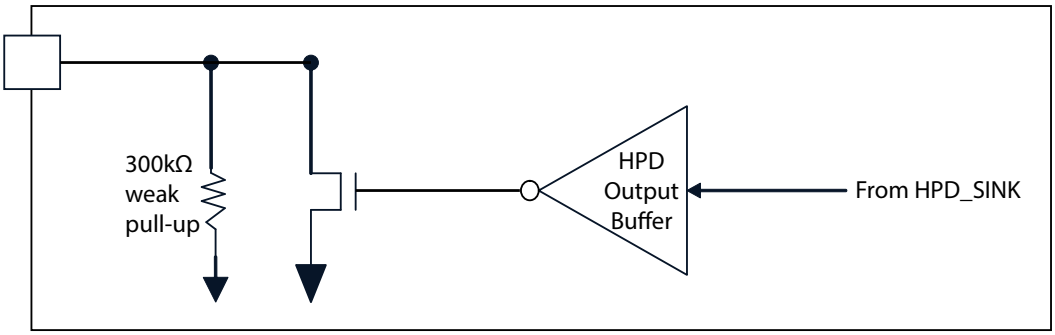
3.3.1 Squelch Function

Squelch is a circuit function to disable the signal outputs when input signal is below ~50mVdiff. Output squelch can shut down TMDS output signals with high impedance or pull-up to VDD in the internal 50Ω resistor.
It can use frequency detection or Voltage threshold method on the TMDS input clock channel. In Frequency detection, the threshold TMDS clock frequency is around 12MHz.
When programming register PORT_SEL[1:0] = 11 or HPD_SINK = 0, all ports shall be shut-down. TMDS Input termination resistor RT switch to power down RPD automatically.

3.3.2 HPD_SRC Output Diagram

External pull-up resistor to 3.3V power supply recommends in open drain output buffer mode.

3.3.3 HPD_SRC Output diagram(open drain only for SINK application)



Note: Open drain buffer is recommended with external pull-up resistor to 3.3V power supply.

3.3.4 Receiver Equalization, Flat Gain and Output Swing Range

Each channel has a programmable equalization network and Flat Gain adjustment. All controls including Equalization, Gain, Output enable/disable can be individually programmed through the on-chip programming register block through pin controls or the I2C serial bus.

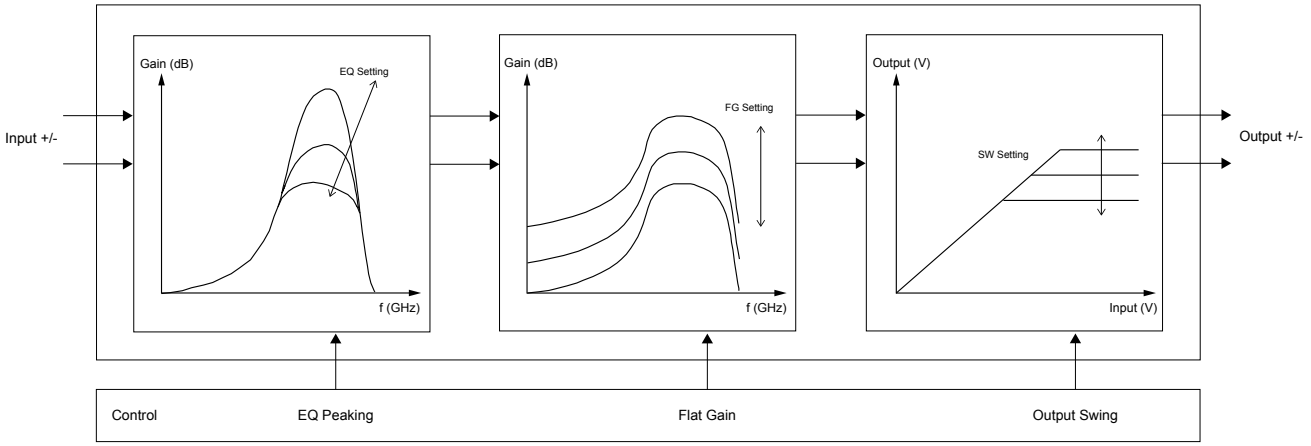


Figure 3-2 Illustration of EQ, Gain and Swing setting

3.4 I2C Register

3.4.1 I²C Address Byte

	b7(MSB)	b6	b5	b4	b3	b2	b1	b0 (R/W)
Address Byte	1	0	1	A3	A2	A1	A0	1/0 *

Note: 1:Read; 0:Write, A[3:0] are four address bits setting in pin-mode

3.4.2 Data Transmission Format

Data is transmitted to the configuration registers using the Write and Read mode as shown in Figure below.

S	Slave Address	R/W=0	A	Start offset	A	Data	A	Data	A	Data	$\overline{A}$/A	P
	7bits	1	1	8	1	8	1	8	1	8	1	

From master to slave A=acknowledge $\overline{A}$=not acknowledge

From slave to master S=start condition P=stop condition

Figure 3-3 I2C Control Register Write Condition

S	Slave address	R/W=0	A	Start offset	A	S	Slave address	R/W=1	A	Data	A	Data	A	Data	$\overline{A}$	P
	7bits	1	1	8	1		7	1	1	8	1	8	1	8	1	

Figure 3-4 I2C Control Register Read Condition

3.5 I2C Control Register

The I2C control register uses index read or write for byte access.

3.5.1 I2C Control Register

Offset	Name	Description	Power Up Condition	Type
0x00	CONFIG[7:0]	[7] Enable Standby. In standby mode. TMDS equalizer and output driver are powered down. 0: normal mode 1: standby mode [6:5] Port selection 00: Port 1 01: Port 2 10: Port 3 11: Disable All ports [4] Source Connection Detector. No sink-connection when HPD_SINK pin is Low. Re-Driver shall not active, and turn off TMDS input termination 50Ω resistors 0: Enable source connection detector (Default) 1: Disable connection detector [3] Squelch Disable 0: Squelch enable (Default) 1: Squelch disable	0x00	R/W
		[2] Squelch result output. 0: No Clock detection in TMDS clock channel 1: Clock detection in TMDS clock channel. When squelch function disable, this bit keep High. This function is available in normal operation mode. In standby or disable all ports, this bit keep Low		R
		[1] RT, RPD control 0: RT active for all 3 ports 1: RT active for selected port, RPD for other non-selected ports	0	R/W
		[0] Reserved	0	R/W

Offset	Name	Description	Power Up Condition	Type
0x01	TERM_SET[7:0]	RX/TX terminal 50 ohm resistor programmable [7:4] Input RX 50 ohm terminal resistor adjust 0000: 50 ohm (default) 0001:+35% 0010:+29% 0011: +22% 0100: +17% 0101: +12% 0110: +8% 0111: +4% 1000: -4% 1001: -7% 1010: -10% 1011:-13% 1100:-16% 1101:-18% 1110:-20% 1111:-22%	0x00	R/W
		[3:1] Output terminal 50 ohm resistor adjust 000: 50 ohm (default) 001:+12% 010:+7.3% 011: +3.4% 100: -3.0% 101: -5.7% 110: -8.1% 111: -10.1% [0] Reserved		

Offset	Name	Description	Power Up Condition	Type
0x02	EQ/FG setting for channel 2	TMDS setting for channel 2 @ 3GHz [7:4] EQ programmable setting for channel 2 0000: 3.5 dB 0001:4.3 dB 0010:5.1 dB 0011:5.9 dB 0100:7.1 dB 0101:7.8 dB 0110:9.1 dB 0111:10.3 dB 1000:11.7 dB 1001:12.6 dB 1010:13.4 dB 1011:14.5dB 1100:15.6 dB 1101:16.4 dB 1110: 17.1 dB 1111: 17.7 dB [3:1] TMDS flat gain setting for channel 2 000: -3.5dB 001: -2.0dB 010: -0.5dB 011: 0.5dB 100: 1.5dB 101: 2.5dB 110: 4.0dB 111: 6.0dB [0] Reserved	0x00	R/W

Offset	Name	Description	Power Up Condition	Type
0x03	EQ/FG setting for channel 1	TMDS setting for channel 1 @ 3GHz [7:4] EQ programmable setting for channel 1 0000: 3.5 dB 0001:4.3 dB 0010:5.1 dB 0011:5.9 dB 0100:7.1 dB 0101:7.8 dB 0110:9.1 dB 0111:10.3 dB 1000:11.7 dB 1001:12.6 dB 1010:13.4 dB 1011:14.5dB 1100:15.6 dB 1101:16.4 dB 1110:17.1 dB 1111:17.7 dB [3:1] TMDS flat gain setting for channel 1 000: -3.5dB 001: -2.0dB 010: -0.5dB 011: 0.5dB 100: 1.5dB 101: 2.5dB 110: 4.0dB 111: 6.0dB [0] Reserved	0x00	R/W
0x04	EQ/FG setting for channel 0	TMDS setting for channel 0 @ 3GHz [7:4] EQ programmable setting for channel 0 0000: 3.5 dB 0001:4.3 dB 0010:5.1 dB 0011:5.9 dB 0100:7.1 dB 0101:7.8 dB 0110:9.1 dB 0111:10.3 dB 1000:11.7 dB 1001:12.6 dB 1010:13.4 dB 1011:14.5dB 1100:15.6 dB 1101:16.4 dB 1110:17.1 dB 1111:17.7 dB	0x00	R/W

Offset	Name	Description	Power Up Condition	Type
		[3:1] TMDS flat gain setting for channel 0 000: -3.5dB 001: -2.0dB 010: -0.5dB 011: 0.5dB 100: 1.5dB 101: 2.5dB 110: 4.0dB 111: 6.0dB [0] Reserved		
0x05	EQ/FG setting for clock channel	TMDS setting for channel CLK @ 3GHz [7:4] EQ programmable setting for channel CLK 0000: 3.5 dB 0001:4.3 dB 0010:5.1 dB 0011:5.9 dB 0100:7.1 dB 0101:7.8 dB 0110:9.1 dB 0111:10.3 dB 1000:11.7 dB 1001:12.6 dB 1010:13.4 dB 1011:14.5dB 1100:15.6 dB 1101:16.4 dB 1110: 17.1 dB 1111: 17.7 dB [3:1] TMDS flat gain setting for channel CLK 000: -3.5dB 001: -2.0dB 010: -0.5dB 011: 0.5dB 100: 1.5dB 101: 2.5dB 110: 4.0dB 111: 6.0dB [0] Reserved	0x00	R/W

Offset	Name	Description	Power Up Condition	Type
0x06	Function[7:0]	[7:6] Reserved [5] DDC switch selection 0: DDC Passive switch(Default) 1: DDC Active buffer [4] TMDS Output Double Termination selection 0: Double termination (Default) 1: Open drain [3:2] DDC VOL, VILC adjustment 00: 0.525 V, 0.425 V 01: 0.603 V, 0.488 V 10: 0.634 V, 0.514 V 11: 0.751 V, 0.608 V [1] Reserved [0] Reserved	0x00	R/W
0x07	SW setting[7:0]	[7:6] TMDS Output Swing setting for channel 2 00: 800 mV 01:900 mV 10: 1000 mV 11: 1100 mV [5:4] TMDS Output Swing setting for channel 1 00: 800 mV 01:900 mV 10: 1000 mV 11: 1100 mV [3:2] TMDS Output Swing setting for channel 0 00: 800 mV 01:900 mV 10: 1000 mV 11: 1100 mV [1:0] TMDS output swing setting for channel CLK 00: 800 mV 01:900 mV 10: 1000 mV 11: 1100 mV	0x00	R/W
0x08	Reserved[7:0]	[7:0] Reserved	0x00	R/W

4. Electrical Specification

4.1 Absolute Maximum Ratings

Supply Voltage to Ground Potential, Vcc . . . . . –0.5 V to +4 V
DC SIG Voltage, Differential between positive and negative inputs. . . . . ± 2.5 V
DC SIG Voltage, at differential inputs . . . . . –0.5 V to 4.0 V
DC SIG Voltage, Control / DDC inputs . . . . . –0.5 V to 4.0 V
Continuous Output Current . . . . . –25 mA to +25 mA
ESD Rating, HBM . . . . . -2 kV to +2 kV
Maximum Junction Temperature . . . . . 125 °C
Storage Temperature . . . . . –65 °C to +150 °C

Note:
(1) Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

4.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max	Units
V_{CC}	Power supply voltage: VDD to GND	3.0	3.3	3.6	V
V_{CC_RAMP}	V_{CC} power supply ramp time (10%V_{CC} to 90%V_{CC})		100		mS
V_{I2C}	I2C Supply that external resistors are pulled up to on SDA and SCL	1.7		3.6	V
T_A	Operation free-air temperature, Commercial	0		70	°C

Note:
(1) Typical parameters in production are tested at VDD = 3.3 ± 0.3V, TA = 25°C.

4.3 Thermal Information

Symbol	Parameter	Value	Units
Theta J_A	Junction-to-ambient resistance	36.70	°C/W
Theta J_C	Junction-to-case (top) thermal resistance	11.80	°C/W

4.4 Power Supply Consumption

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ.	Max	Units
I_{dd}	Main Supply current	Output Enable, Double termination with 50Ω to VDD, PRBS7 pattern, Data rate 6 Gbps, Not included 40mA current to source		180	250	mA
I_{stb1}	Standby Current with MS=0	PORT_SEL[1:0]=11 or HPD_SINK = 0		30	100	uA
I_{stb2}	Standby Current with MS=1	DDC passive switch OFF or HPD_SINK = 0		0.24	0.3	mA
I_{sqlh_sw}	Squelch Current with DDC Switch	No clock input signal: Terminated with 50Ω to Vdd, HPD_SINK =1, DDC Passive switch		12	15	mA
I_{sqlh_buffer}	Squelch Current with Active Buffer	No clock input signal: Terminated with 50Ω to Vdd, HPD_SINK =1, DDC Active Buffer		14	18	mA

4.5 DC Electrical characteristics

Note: Over recommend operating supply and temperature range unless otherwise specified.

4.5.1 Control Pins

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
Control Pins						
V_{IH}	High Level Input Voltage		2		3.6	V
V_{IL}	Low Level Input Voltage		0		0.8	V
I_{IL}	Low Level Digital Input Current	V_{IL} = GND	-15		20	µA
I_{IH}	High Level Digital Input Current	$V_{IH} = V_{CC} = 3.3V$	-15		20	µA
R_{PU}	Internal Pull-up Resistor			11		kΩ

4.5.2 DDC Channel Buffer

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DDC Source Side						
V_{OL}	Low level Output Voltage, Source Side DDC Buffer	External pull-up Rup to VDD from 1.5kΩ to 10kΩ	0		0.2	V
V_{IH}	High level Input Voltage, Source Side DDC Buffer		0.7xV_{CC}		V_{CC}	V
V_{IL}	Low level Input Voltage, Source Side DDC Buffer		0		0.3xV_{CC}	V
I_{input}	Input Current	0.1 x V_{I2C} < Input voltage < 3.3V	-20		20	µA
C_{input}	Input capacitance	$V_{input-pp}$ = 1V, 100 KHz			10	pF
DDC Sink Side						
V_{IH}	High level Input Voltage		2.0			V
V_{IL}	Buffer Input Low Voltage				0.8	V
V_{OL}	Low level Output Voltage	External pull-up Rup to VDD from 1.5kΩ to 10kΩ	0.47	0.52	0.6	V
V_{ILC}	DDC Buffer low-level contention input voltage	I2C register 0x06 bit[3:2] can adjust VILC range. Default is 0x00. [00]: 0.525 V, 0.425 V [01]: 0.603 V, 0.488 V [10]: 0.634 V, 0.514 V [11]: 0.751 V, 0.608 V		0.4		V
I_{input}	Input Current	0.1 x V_{I2C} < Input voltage < 3.3V	-20		20	µA
C_{input}	Input capacitance	V_I peak-peak = 1V, 100 KHz			10	pF
DDC Passive Switch						
I_{IL_DDC}	Low level digital input current	V_{IL} = GND	-20		20	µA
I_{IH_DDC}	High level digital input current	$V_{IH} = V_{CC} = 3.3V$	-20		20	µA
$I_{input-leak}$	Input leakage current	DDC switch is off, V_{IN} = 3.6V	-20		30	µA
C_{IO}	Input/Output capacitance when passive switch on	$V_{input\ p-p}$ = 1V, 100 KHz		10		pF

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R_{ON}	Passive Switch resistance: SCL_SINK to SCL_SRC, SDA_ SINK to SDA_SRC pin sweep	I_{IN} = 3mA, Vin = 0.4V		16	30	Ω
V_{PASS}	Switch Output voltage	V_I = 3.3V, I_{IN} = 100uA, V_{CC} = 3.3V	1.5	2.0	2.5	V

4.5.3 Hot Plug Detect (Open drain output)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Source Side						
V_{OH}	High level output voltage	HPD source, I_{OL} = 4mA	2.4		3.6	V
V_{OL}	Low level output voltage	HPD source, I_{OL} = 4mA	0		0.4	V
Sink Side						
V_{IH}	High level input voltage	HPD sink pin	2.0			V
V_{IL}	Low level input voltage	HPD sink pin			0.8	V
I_{IH}	High level input current	Device powered, V_{IH} = 3.3V. $I_{h\text{-}hpd}$ includes $R_{pd\text{-}hpd}$ resistor current	-20		60	µA
I_{IL}	Low level input current	Device powered, V_{IH} = 3.3V. $I_{h\text{-}hpd}$ includes $R_{pd\text{-}hpd}$ resistor current	-20		20	µA
$R_{pd\text{-}hpd}$	HPD input termination to GND	V_{CC} = 0		120		kΩ

4.6 AC Electrical characteristics

Note: Over recommend operating supply and temperature range unless otherwise specified.

4.6.1 TMDS Differential

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
TMDS Differential Input						
DR_{data}	Data Rate		0.25		6	Gbps
DR_{clk}	Clock Rate		25		340	MHz
$T_{rx\text{-}duty}$	Input clock duty cycle		40	50	60	%
$V_{rx\text{-}cm}$	Input Common-mode voltage (DC)	Output enable		3.0		V
$V_{diff\text{-}pp}$	Differential Input Peak-to-peak Voltage	Operational			1.4	Vppd
$T_{sk\_intra\_in}$	Intra-pair Differential Skew tolerance				0.15	UI
V_{noise_input}	Input-referred noise	100MHz to 6 Gbps, FG<2:0> = 101, EQ<3:0> = 0000		0.5		mV_{RMS}
		100MHz to 6 Gbps, FG<2:0> = 101, EQ<3:0> = 1010		0.4		mV_{RMS}
$V_{DIFFp\text{-}p}$	Peak to peak differential input voltage			400		mV
$R_{diff\text{-}term}$	Differential input termination		45		55	Ω

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
$Z_{rx\text{-}hiz}$	Common mode input impedance during reset or power down			200		kΩ
S_{11}	Input Return loss, SW=1.0	10MHz to 6GHz differential mode		-12		dB
		1GHz to 6GHz common mode		-5		dB
R_{pu}	Internal Pull-up Resistor	Data channel RT/Rout, Double termination		50		Ω
R_{pd}	Internal Pull-down Resistor	Data channel, HPD_SINK=0 (Disable all ports)		1		kΩ
TMDS Differential Output						
$V_{out\text{-}swing}$	Output voltage swing threshold				1300	mVpp
R_{term}	Source termination for HDMI 2.0			50		Ω
C_{tx}	AC coupling capacitors of the driver		75		1220	nF
I_{short}	Short circuit current				50	mA
S_{22}	Output return loss, SW=1.0V	10MHz to 6GHz differential		-17		dB
		1GHz to 6GHz common mode		-7		dB
V_{noise_output}	Output-referred noise(2)	100MHz to 6 Gbps, FG<2:0> = 101, EQ<3:0> = 0000		0.7		mV_{RMS}
	Output-referred noise(2)	100MHz to 6 Gbps, FG<2:0> = 101, EQ<3:0> = 1010		0.8		mV_{RMS}

4.6.2 Timing Characteristic

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_R	Input signal rise time	20-80%		34		ps
T_F	Input signal rise time	20-80%		34		ps
$T_{jit\text{-}clk}$	Peak to peak output jitter, clock channel			5	10	ps
$T_{jit\text{-}data}$	Peak to peak output jitter, data channel			18	50	ps
$T_{sk\_Intra\_In}$	Input Intra-pair Differential Skew tolerance				0.15	UI
R_J	Add-in Random Jitter	at 6 Gbps		0.57		RMS ps
D_J	Add-in Deterministic Jitter	at 6 Gbps		6.57		ps
$T_{sk\_intra\text{-}diff}$	Output Intra-pair Differential Skew			5	10	ps
$T_{skew\_inter\text{-}diff}$	Output Inter-pair Differential Skew			8		ps
T_{enable}	Enable time				10	us
$T_{disable}$	Disable time				1	us

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{PLH}	Low-to-High Propagation Delay			65		ps
T_{PHL}	High-to-Low Propagation Delay			65		ps
T_{sx}	Select to Switch Output				10	ns
T_{PD}	Latency	From input to output		0.5		ns
V_{coup}	Channel isolation, SW=1.0V	3GHz, FG = 0.5dB		-25		dB
$G_{peaking}$	Peaking gain (Compensation at 6Gbps, relative to 100MHz, 100mVp-p sine wave input)	EQ<3:0> = 1111		14.7		dB
		EQ<3:0> = 1000		12		
		EQ<3:0> = 0000		6.8		
		Variation around typical	-3		+3	dB
G_{flat}	Flat gain (100MHz, EQ<3:0> = 1000, SW<1:0> = 10)	FG<2:0>=111		6.0		dB
		FG<2:0>=110		4.0		
		FG<2:0>=101		2.5		
		FG<2:0>=100		1.5		
		FG<2:0>=011		0.5		
		FG<2:0>=010		-0.5		
		FG<2:0>=001		-2.0		
		FG<2:0>=000		-3.5		
		Variation around typical	-3		3	dB
V_{1dB_100M}	-1dB compression point of output swing (at 100MHz)	SW<1:0> = 11		1370		mVpp
		SW<1:0> = 10		1280		
		SW<1:0> = 01		1040		
		SW<1:0> = 00		920		
V_{1dB_6G}	-1dB compression point of output swing (at 6 Gbps)	SW<1:0> = 11		1100		mVpp
		SW<1:0> = 10		1000		
		SW<1:0> = 01		900		
		SW<1:0> = 00		800		

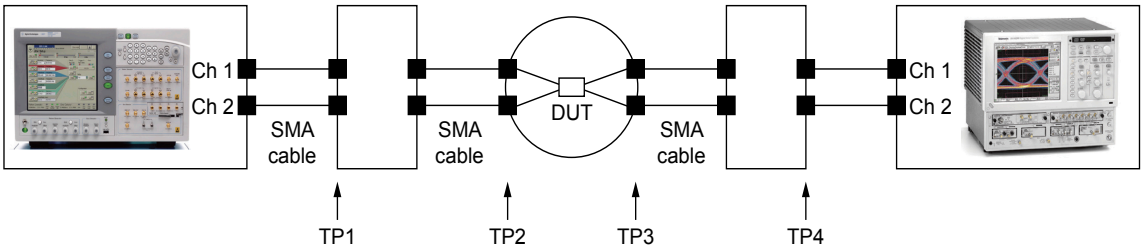
4.6.3 DDC Channels

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Passive Switch mode						
$T_{pd\text{-}ddc}$	Propagation delay	CL = 10pF in passive switch			5	ns
Buffer mode						
T_{pd}	Propagation delay	CL= 10pF, in active switch (1.5kΩ to 5kΩ pull high, 10pf to gnd)			60	ns
T_{plh}	Low-to-High propagation delay	SCL/SDA_sink to SCL/SDAx		169	255	ns
T_{phl}	High-to-Low propagation delay	SCL/SDA_sink to SCL/SDAx	10	103	300	ns
T_{plh}	Low -to- High propagation delay	SCL/SDAx to SCL/SDA_sink	25	67	110	ns

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{phl}	High-to-Low propagation delay	SCL/SDAx to SCL/SDA_sink		118	230	ns

4.6.4 HPD Switching

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{pd-hpd}	Propagation delay from HPD sink to HPD source, rising and falling edge			40	120	ns
$T_{disconnect}$	HPD logical disconnected time-out		2			ms



1) Trace card between TP1 and TP2 is designed to emulate 6-48" of FR4. Trace width -4 mils,100Ω differnetial impedance
2) All jitter is measured at a BER of 10-9
3) Residual jitter reflects the total jitter measured at TP4 jitter minus TP1 jitter
4) VDD = 3.3V, RT = 50Ω
5) The input signal from JBERT does not have any pre-emphasis.

Figure 4-1 Electrical parameter test setup

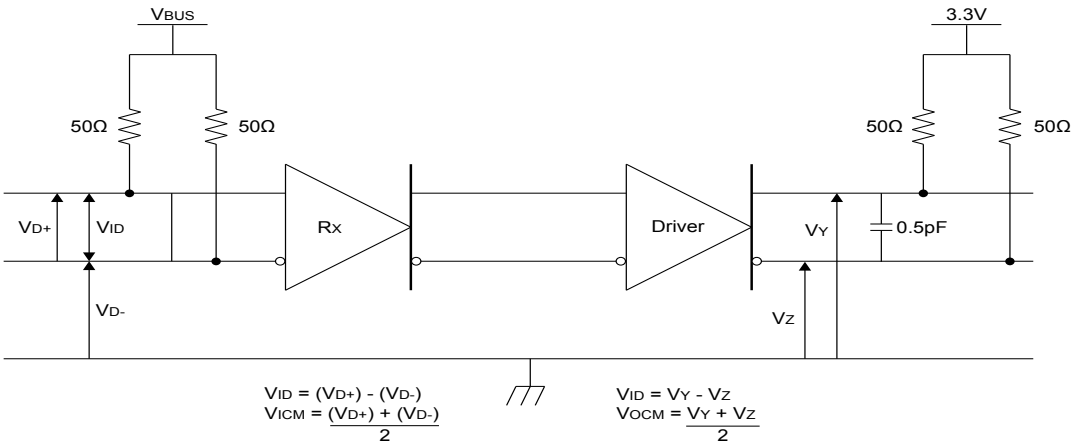


Figure 4-2 Intra and Inter-pair Differential Skew definition

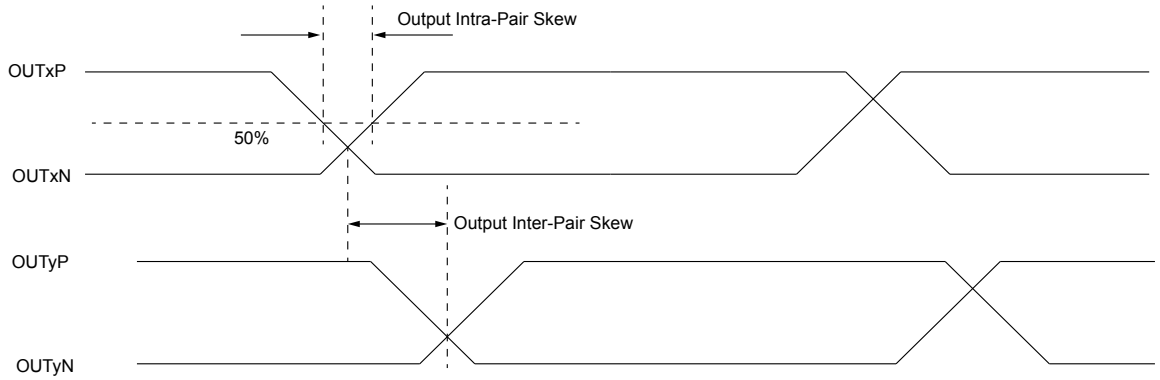


Figure 4-3 Intra and Inter-pair Differential Skew

Common Mode Voltage
$V_{CM} = (|VD+ + VD-| / 2)$
$V_{CMP} = (\max |VD+ + VD-| / 2)$

Symmetric Differential Swing
$V_{DIFFp-p} = (2 * \max |V_{D+} - V_{D-}|)$

Asymmetric Differential Swing
$V_{DIFFp-p} = (\max |V_{D+} - V_{D-}| \{V_{D+} > V_{D-}\}$
$+ \max |V_{D+} - V_{D-}| \{V_{D+} < V_{D-}\})$

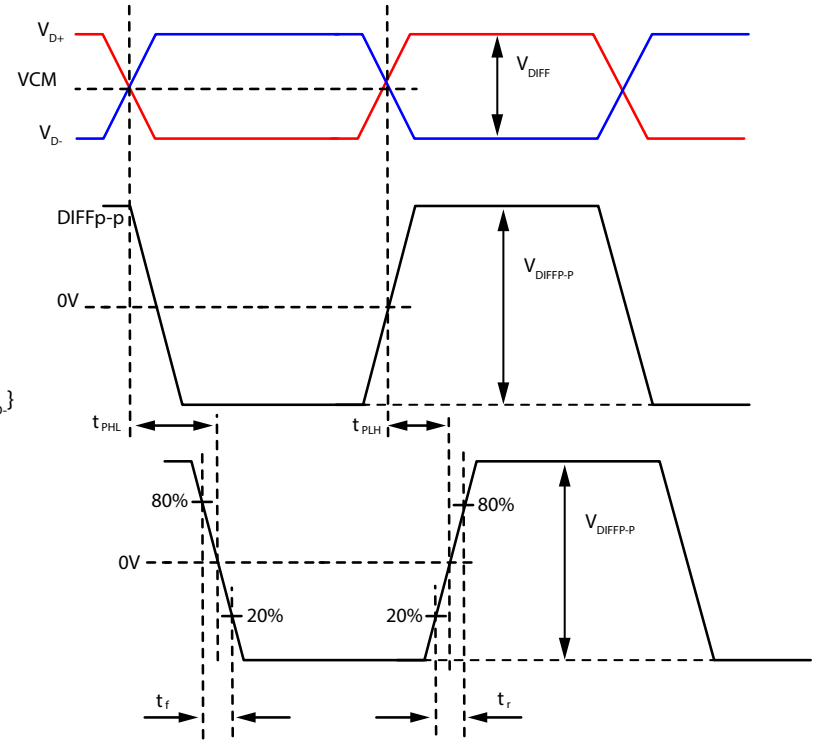


Figure 4-4 Definition of Peak-to-peak Differential voltage

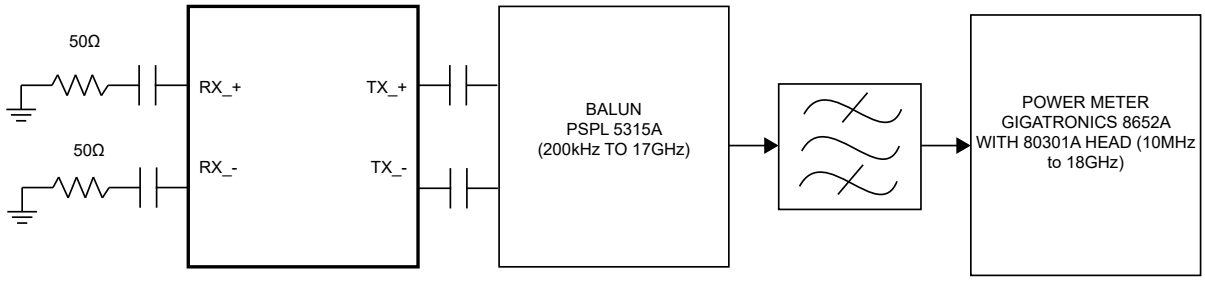


Figure 4-5 Noise test configuration

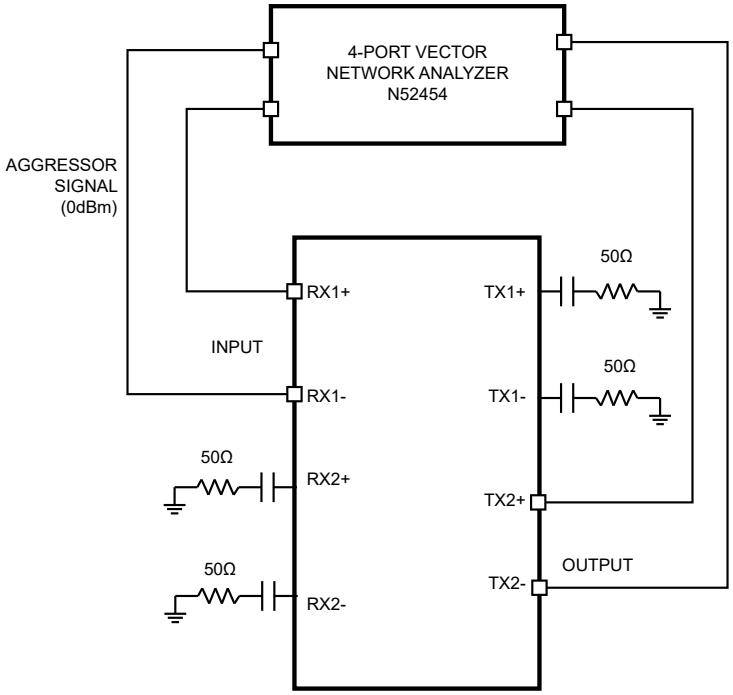
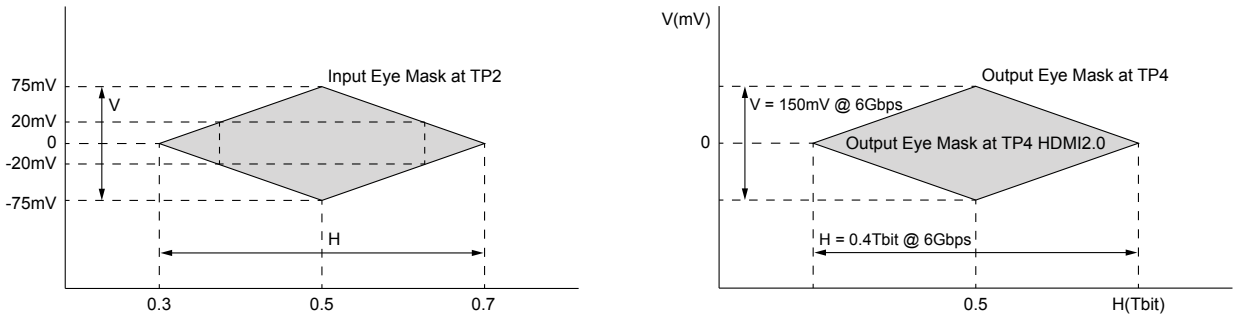
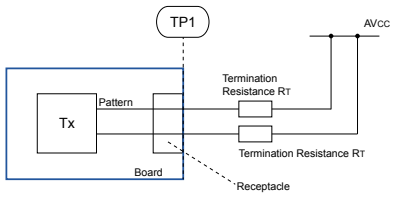


Figure 4-6 Channel-isolation test configuration

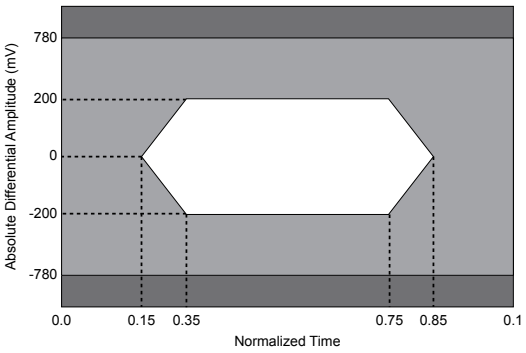


TMDS Data Rate (Gbps)	H (Tbit)	V (mV)	Standard
3.4 < DR < 3.712	0.6	335	HDMI2.0
3.712 < DR < 5.94	-0.0332Rbit2 +0.2312R +0.1998	-19.66Rbit2 +106.74Rbit +209.58	HDMI2.0
5.94 < DR < 6.0	0.4	150	HDMI2.0

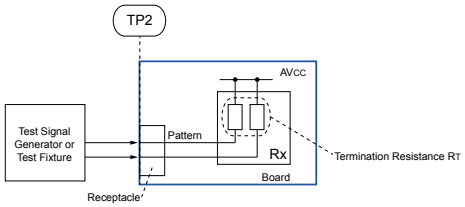
Figure 4-7 Eye mask at TP2 input and TP4 output for HDMI 2.0 standard



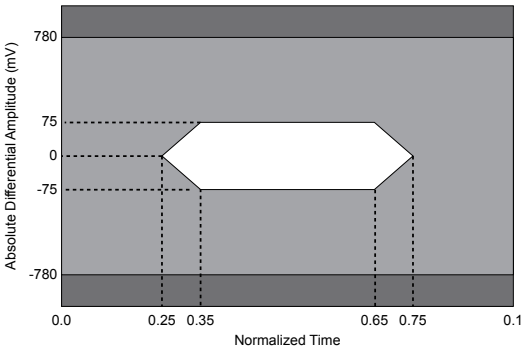
HDMI 1.4 Source Test



HDMI 1.4 Eye Diagram Mask at TP1 for Source Requirements



HDMI 1.4 Sink Test



HDMI 1.4 Eye Diagram Mask at TP1 for Sink Requirements

Figure 4-8 Eye mask at TP2 input and TP4 output for HDMI 1.4 standard

4.7 I2C Interface Bus

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
VDD	Nominal Bus Voltage		3.0		3.6	V
Freq	Bus Operation Frequency				400	kHz
V_{IH}	DC input logic high		$V_{DD}/2$ + 0.7		V_{DD} + 0.3	V
V_{IL}	DC input logic low		-0.3		$V_{DD}/2$ - 0.7	V
V_{OL}	DC output logic low	I_{OL} = 3mA			0.4	V
Ipullup	Current Through Pull-Up Resistor or Current Source	High Power specification	3.0		3.6	mA
Ileak-bus	Input leakage per bus segment		-200		200	uA
Ileak-pin	Input leakage per device pin			-15		uA
CI	Capacitance for SDA/SCL				10	pF
tBUF	Bus Free Time Between Stop and Start condition		1.3			us
tHD:STA	Hold time after (Repeated) Start condition. After this period, the first clock is generated.	At pull-up, Max	0.6			us
TSU:STA	Repeated start condition setup time		0.6			us
TSU:STO	Stop condition setup time		0.6			us
THD:DAT	Data hold time		0			ns
TSU:DAT	Data setup time		100			ns
tLOW	Clock low period		1.3			us
tHIGH	Clock high period		0.6		50	us
tF	Clock/Data fall time				300	ns
tR	Clock/Data rise time				300	ns
tPOR	Time in which a device must be operation after power-on reset				500	ms

Note:
(1) Recommended maximum capacitance load per bus segment is 400pF.
(2) Compliant to I2C physical layer specification.
(3) Ensured by Design. Parameter not tested in production.

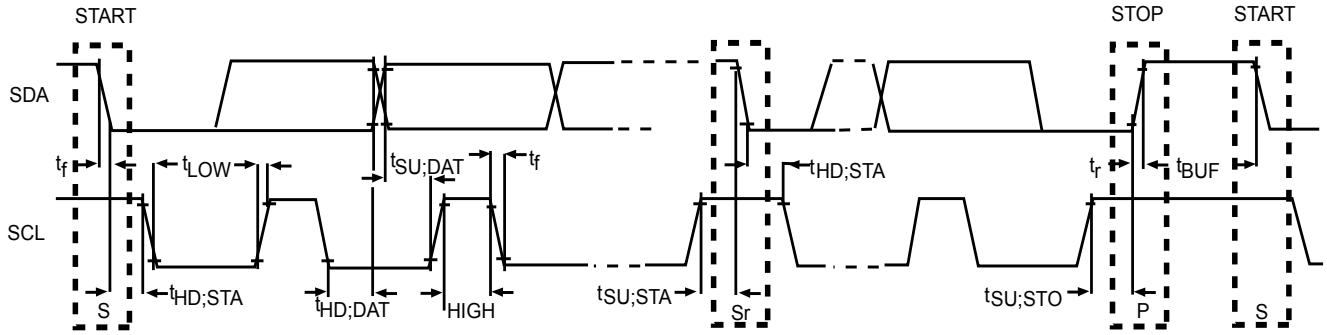
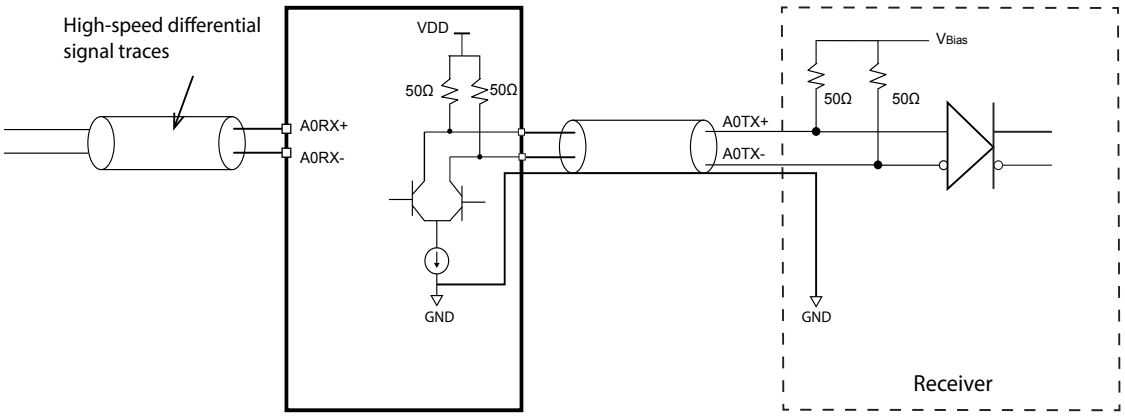


Figure 4-9 Channel-isolation test configuration

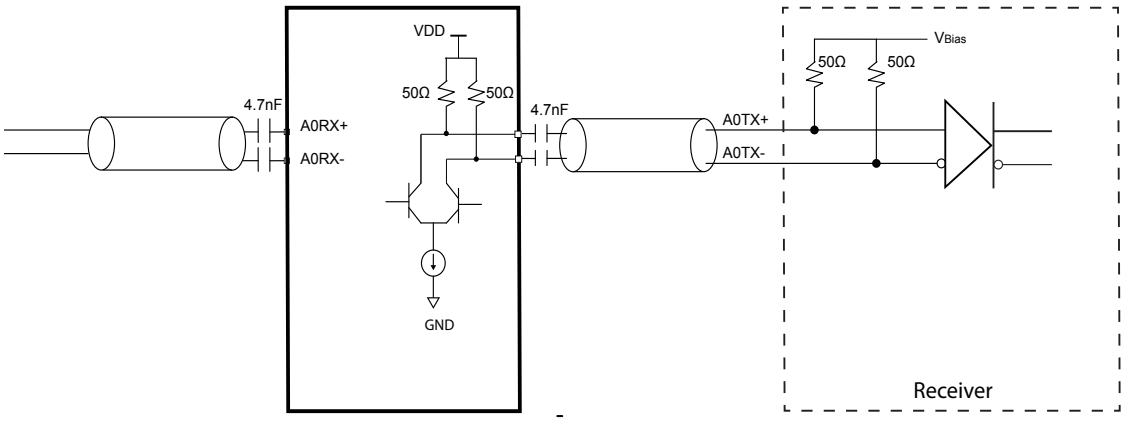
5. Application

Note: Information in the following applications sections is not part of the component specification, and does not warrant its accuracy or completeness. Customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

5.1 DC/AC-coupled Application



DC-Coupled Differential Signaling Application Circuits



AC-Coupled Differential Signaling Application Circuits

Figure 5-1 DC/AC-coupled Application Diagram

5.2 I2C Vilc (input low contention level) and Pullup Resistor Sizing

For Repeater to function correctly, all devices on the B-side must be able to pull the B-side below the voltage input low contention level (V_{ilc}). This means that the Vol of any device on the B-side must be below 0.4 V.
Vol of a device can be adjusted by changing the Iol through the device which is set by the pull-up resistance value. The pull-up resistance on the B-side must be carefully selected to ensure that logic levels will be transferred correctly to the A-side.

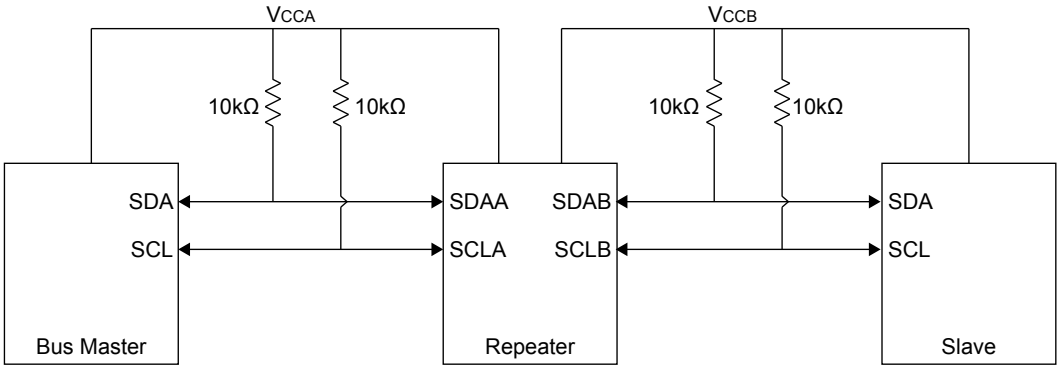


Figure 5-2 Typical DDC repeater connection between Master to Slave

5.3 System Application Block Diagram

- DDC CH inputs requires to add external MOSFET to support 5V tolerance.

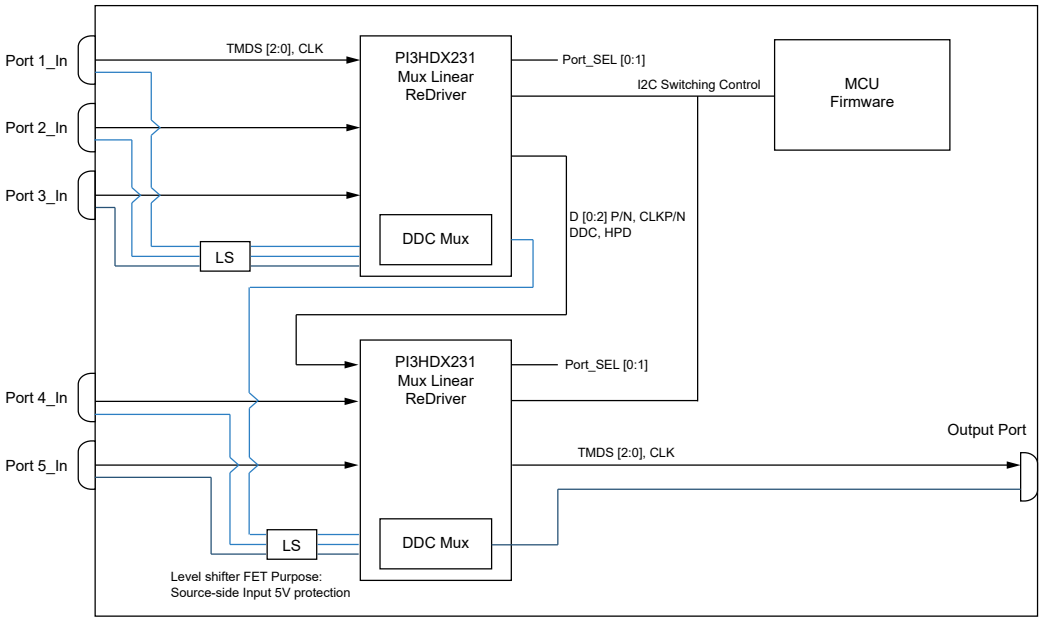


Figure 5-3 HDMI 2.0 Switch 5:1 Application Block Diagram

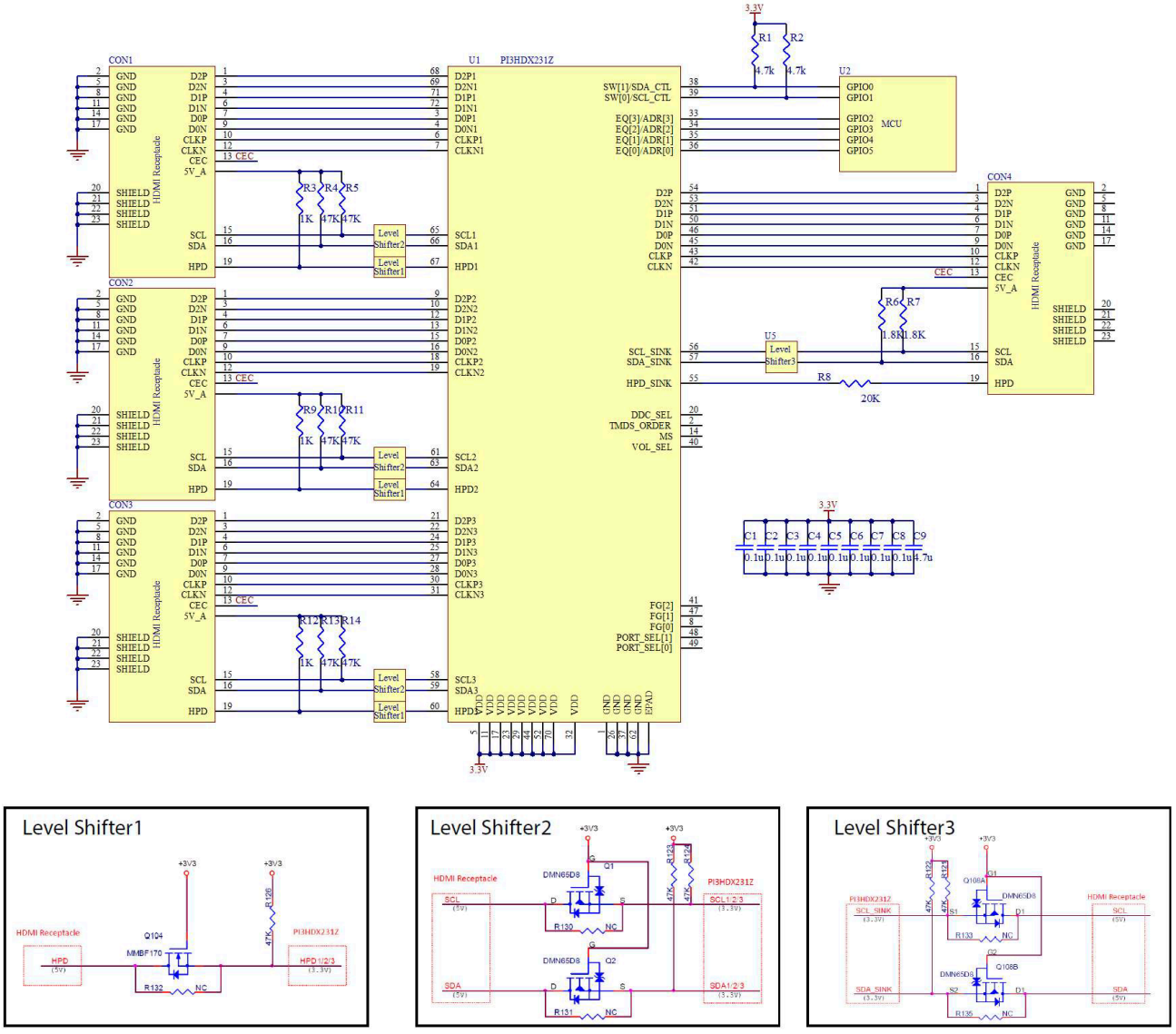


Figure 5-4 HDMI Sink-side Application with I2C mode switching control

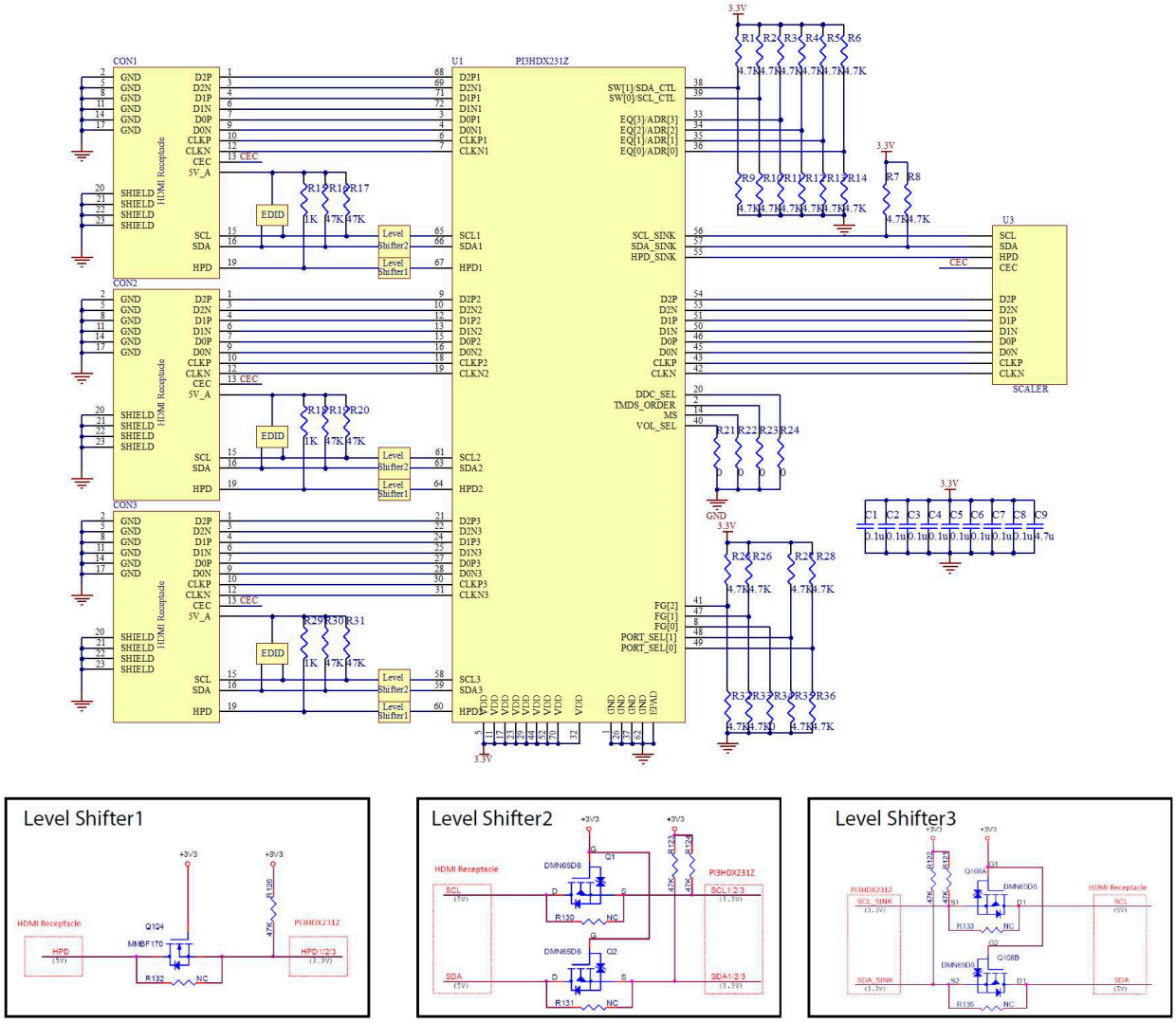


Figure 5-5 HDMI Sink Application in Pin mode

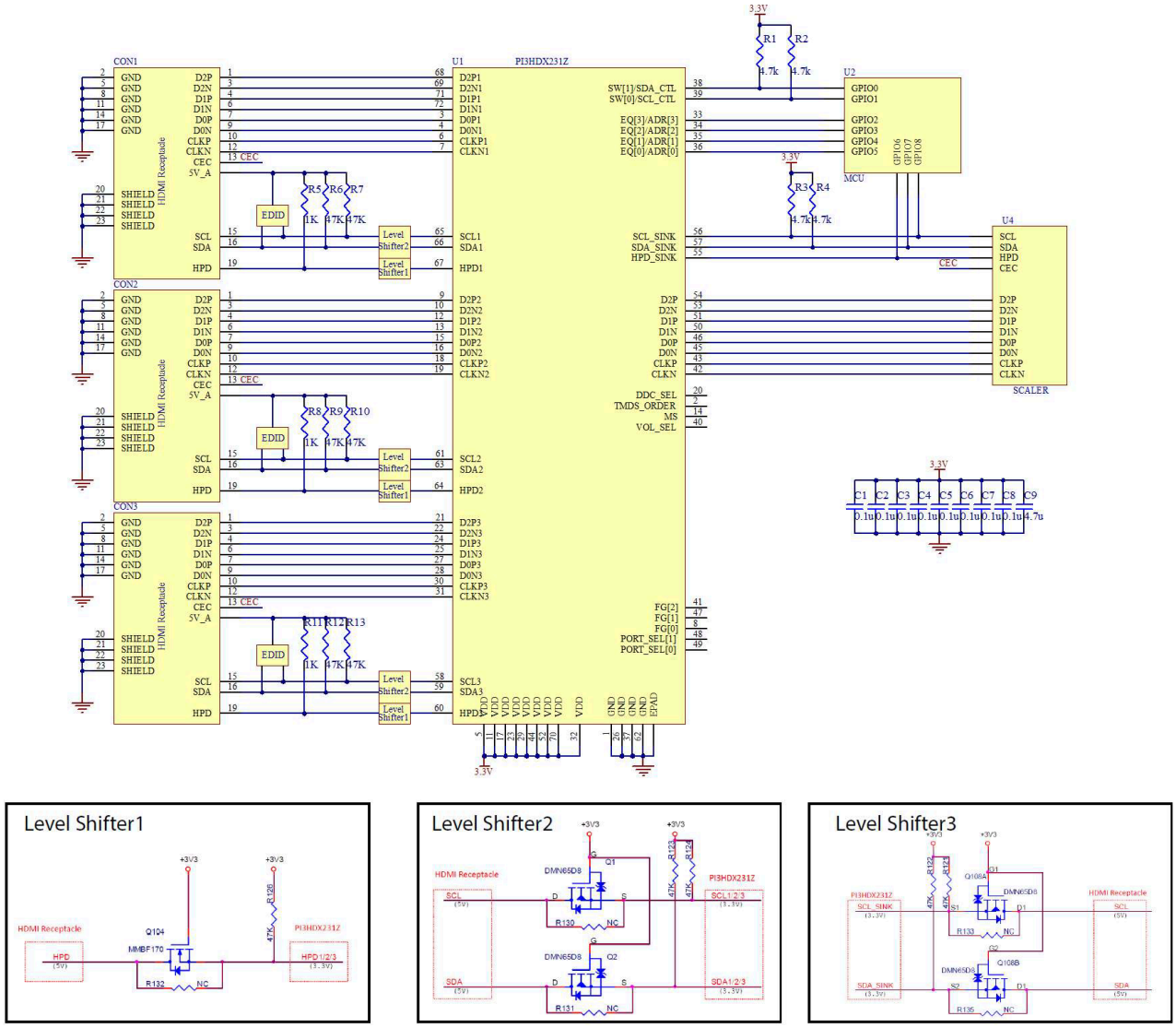


Figure 5-6 HDMI Switch Application in I2C mode

5.4 HDMI 2.0 Compliance Test

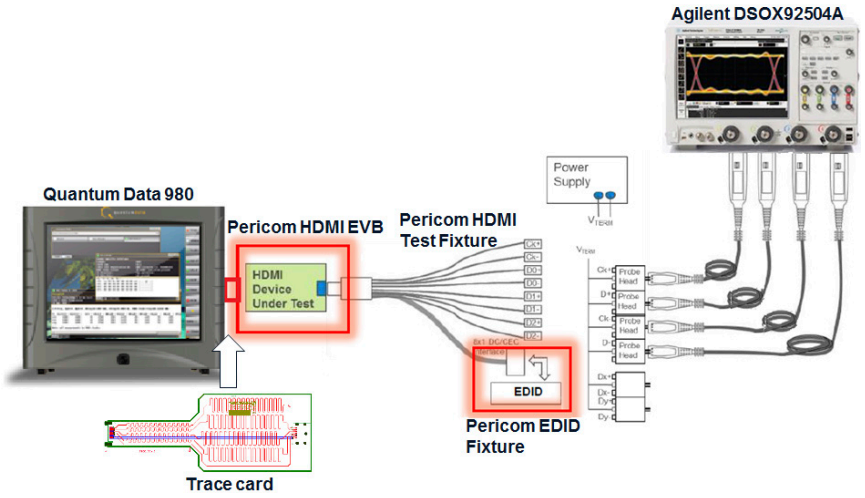


Figure 5-7 HDMI 2.0 CTS test setup*

Note: Application Trace Card Information for CTS test

HDMI FR4 trace	0 in	6 in	12 in	18 in	24 in	30 in	36 in
Insertion loss @ 6Gbps	-5.91 dB	-9.75 dB	-10.47 dB	-13.05 dB	-15.87 dB	-16.97 dB	-21.20 dB

HDMI Test Report

Overall Result: PASS

Test Configuration Details	
Device Description	
Device ID	Transmitter
Fixture Type	Other
Probe Connection	4 Probes
Probe Head Type	N5444A
Lane Connection	1 Data Lane
HDMI Specification	2.0
HDMI Test Type	TMDS Physical Layer Tests
Test Session Details	
Infiniium SW Version	05.60.00603
Infiniium Model Number	DSOX92504A
Infiniium Serial Number	MY54410104
Application SW Version	2.11
Debug Mode Used	No
Probe (Channel 1)	Model: N2801A Serial: US54094067 Head: N5444A Atten: Calibrated (15 NOV 2016 08:41:35), Using Cal Atten (5.6775E+000) Skew: Calibrated (15 NOV 2016 08:41:48), Using Cal Skew
Probe (Channel 2)	Model: N2801A Serial: US54094054 Head: N5444A Atten: Calibrated (15 NOV 2016 08:42:27), Using Cal Atten (5.4765E+000) Skew: Calibrated (15 NOV 2016 08:42:43), Using Cal Skew
Probe (Channel 3)	Model: N2801A Serial: US54094059 Head: N5444A Atten: Calibrated (15 NOV 2016 08:43:31), Using Cal Atten (5.7058E+000) Skew: Calibrated (15 NOV 2016 08:43:50), Using Cal Skew
Probe (Channel 4)	Model: N2801A Serial: US54094057 Head: N5444A Atten: Calibrated (15 NOV 2016 08:45:07), Using Cal Atten (5.5974E+000) Skew: Calibrated (15 NOV 2016 08:45:35), Using Cal Skew
Last Test Date	2016-11-23 11:48:03 UTC +08:00

Figure 5-8 HDMI 2.0 Compliance Report

5.5 Layout Guidelines

As transmission data rate increases rapidly, any flaws and/or mis-matches on PCB layout are amplified in terms of signal integrity

5.5.1 Power and Ground

To provide a clean power supply for Pericom high-speed device, few recommendations are listed below:

- Power (VDD) and ground (GND) pins should be connected to corresponding power planes of the printed circuit board directly without passing through any resistor.
- The thickness of the PCB dielectric layer should be minimized such that the VDD and GND planes create low inductance paths.
- One low-ESR 0.1uF decoupling capacitor should be mounted at each VDD pin or should supply bypassing for at most two VDD pins. Capacitors of smaller body size, i.e. 0402 package, is more preferable as the insertion loss is lower. The capacitor should be placed next to the VDD pin.
- One capacitor with capacitance in the range of 4.7uF to 10uF should be incorporated in the power supply decoupling design as well. It can be either tantalum or an ultra-low ESR ceramic.
- A ferrite bead for isolating the power supply for Pericom high-speed device from the power supplies for other parts on the printed circuit board should be implemented.
- Several thermal ground vias must be required on the thermal pad. 25-mil or less pad size and 14-mil or less finished hole are recommended.

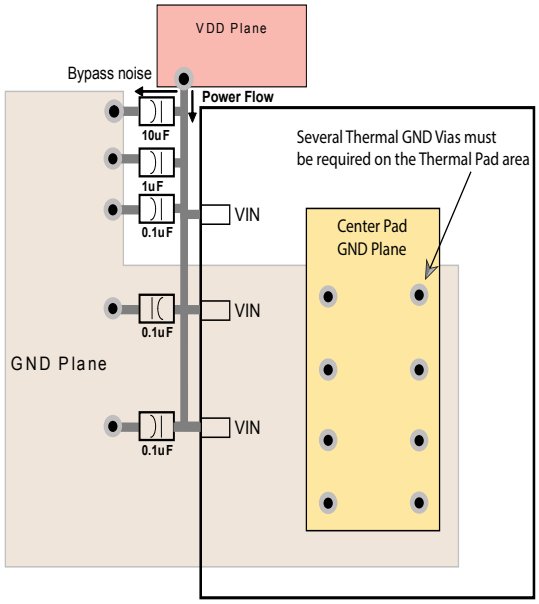


Figure 5-9 Decoupling Capacitor Placement Diagram

5.5.2 High-speed Signal Routing

Well-designed layout is essential to prevent signal reflection:

- For 90Ω differential impedance, width-spacing-width micro-strip of 6-7-6 mils is recommended; for 100Ω differential impedance, width-spacing-width micro-strip of 5-7-5 mils is recommended.
- Differential impedance tolerance is targeted at ±15%.

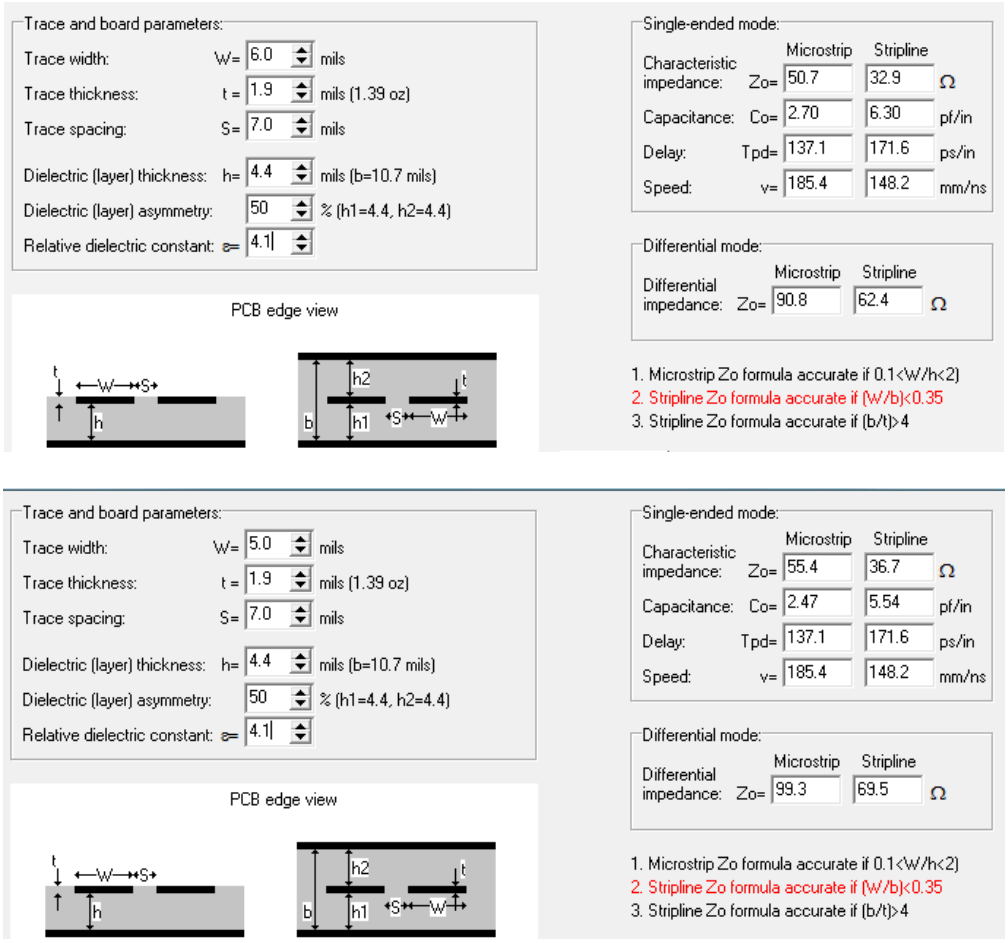


Figure 5-10 Trace Width and Clearance of Micro-strip and Strip-line

- For micro-strip, using 1/2oz Cu is fine. For strip-line in 6+ PCB layers, 1oz Cu is more preferable.

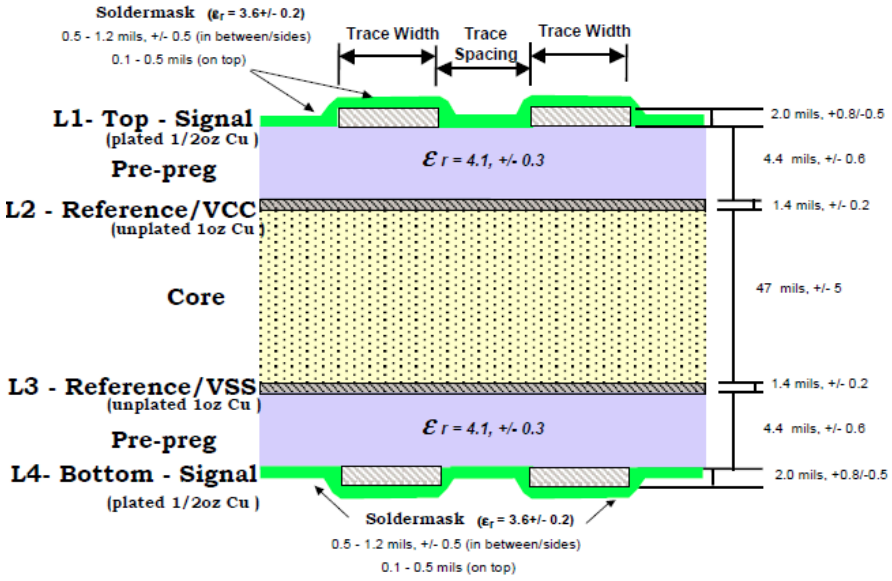


Figure 5-11 4-Layer PCB Stack-up Example

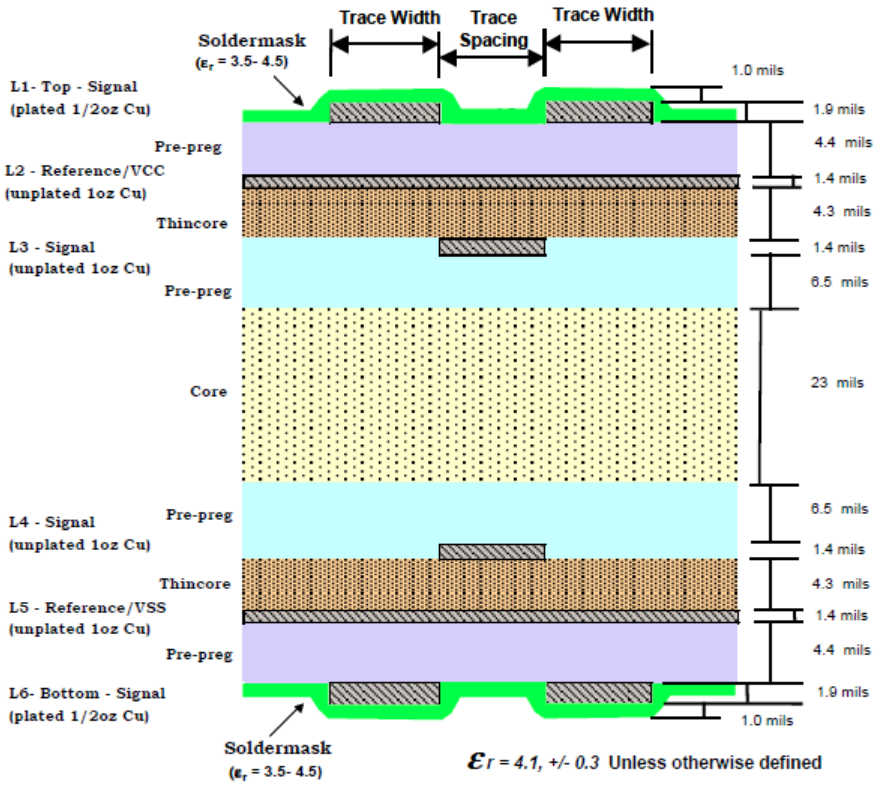


Figure 5-12 6-Layer PCB Stack-up Example

- Ground referencing is highly recommended. If unavoidable, stitching capacitors of 0.1uF should be placed when reference plane is changed.

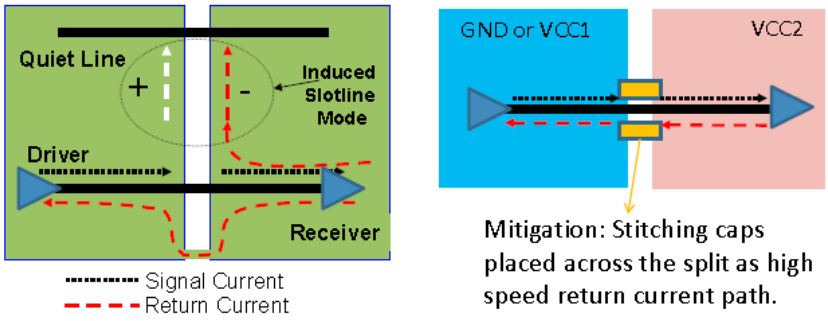


Figure 5-13 Stitching Capacitor Placement

- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.

- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.

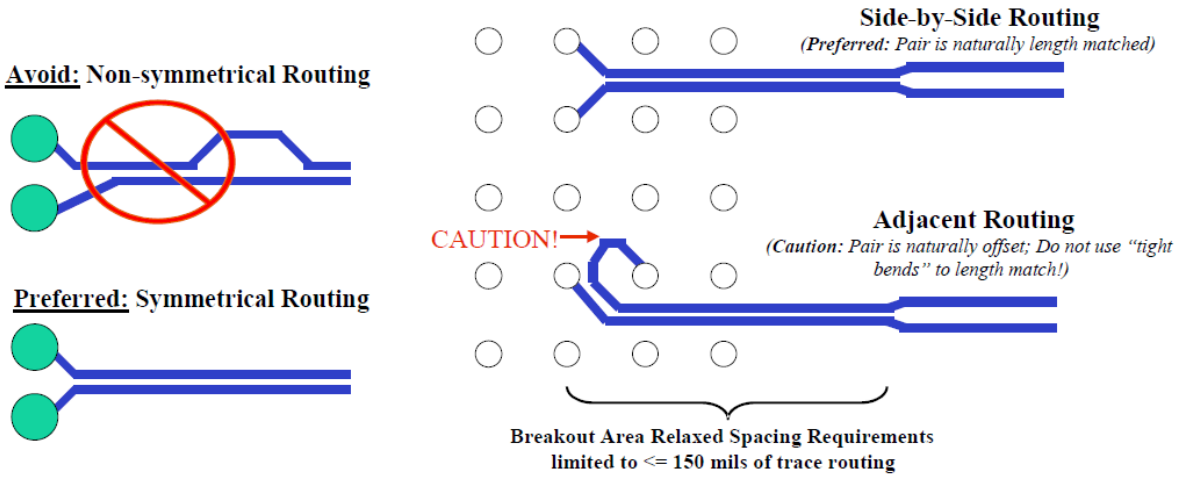


Figure 5-14 Layout Guidance of Matched Differential Pair

- For minimal crosstalk, inter-pair spacing between two differential micro-strip pairs should be at least 20 mils or 4 times the dielectric thickness of the PCB.
- Wider trace width of each differential pair is recommended in order to minimize the loss, especially for long routing. More consistent PCB impedance can be achieved by a PCB vendor if trace is wider.
- Differential signals should be routed away from noise sources and other switching signals on the printed circuit board.
- To minimize signal loss and jitter, tight bend is not recommended. All angles α should be at least 135 degrees. The inner air gap A should be at least 4 times the dielectric thickness of the PCB.

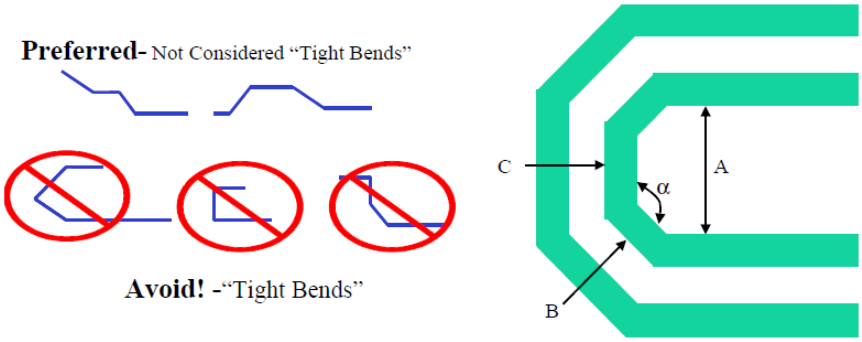


Figure 5-15 Layout Guidance of Bends

- Stub creation should be avoided when placing shunt components on a differential pair.

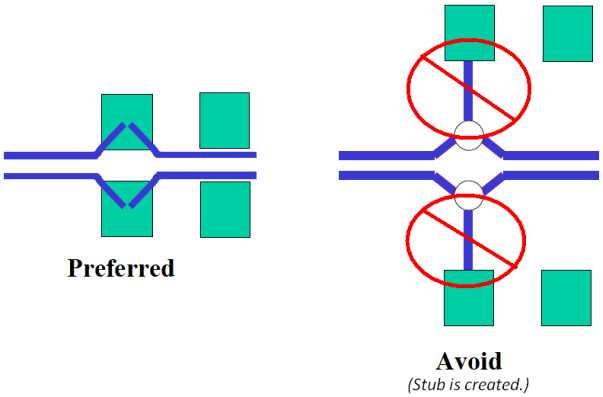


Figure 5-16 Layout Guidance of Shunt Component

- Placement of series components on a differential pair should be symmetrical.

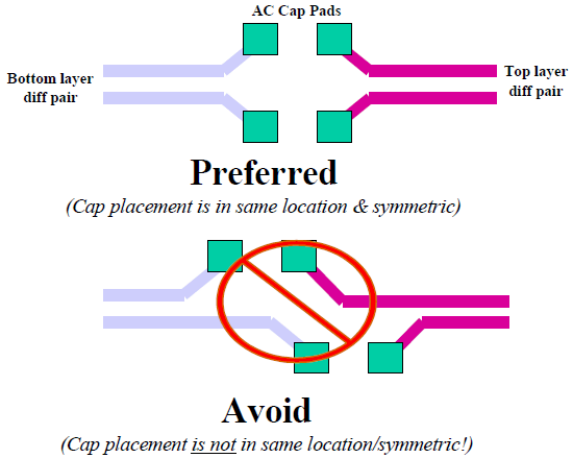


Figure 5-17 Layout Guidance of Series Component

- Stitching vias or test points must be used sparingly and placed symmetrically on a differential pair.

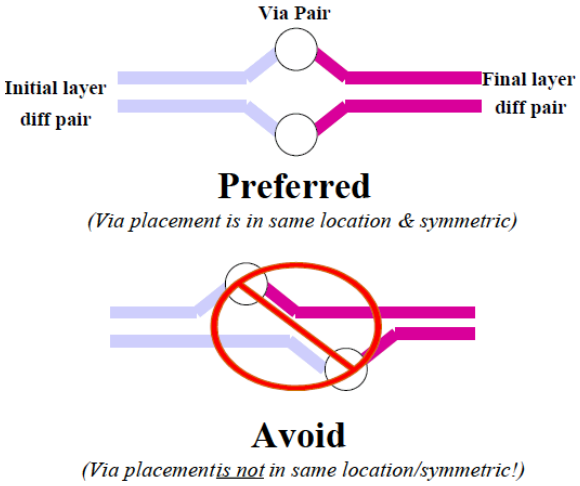
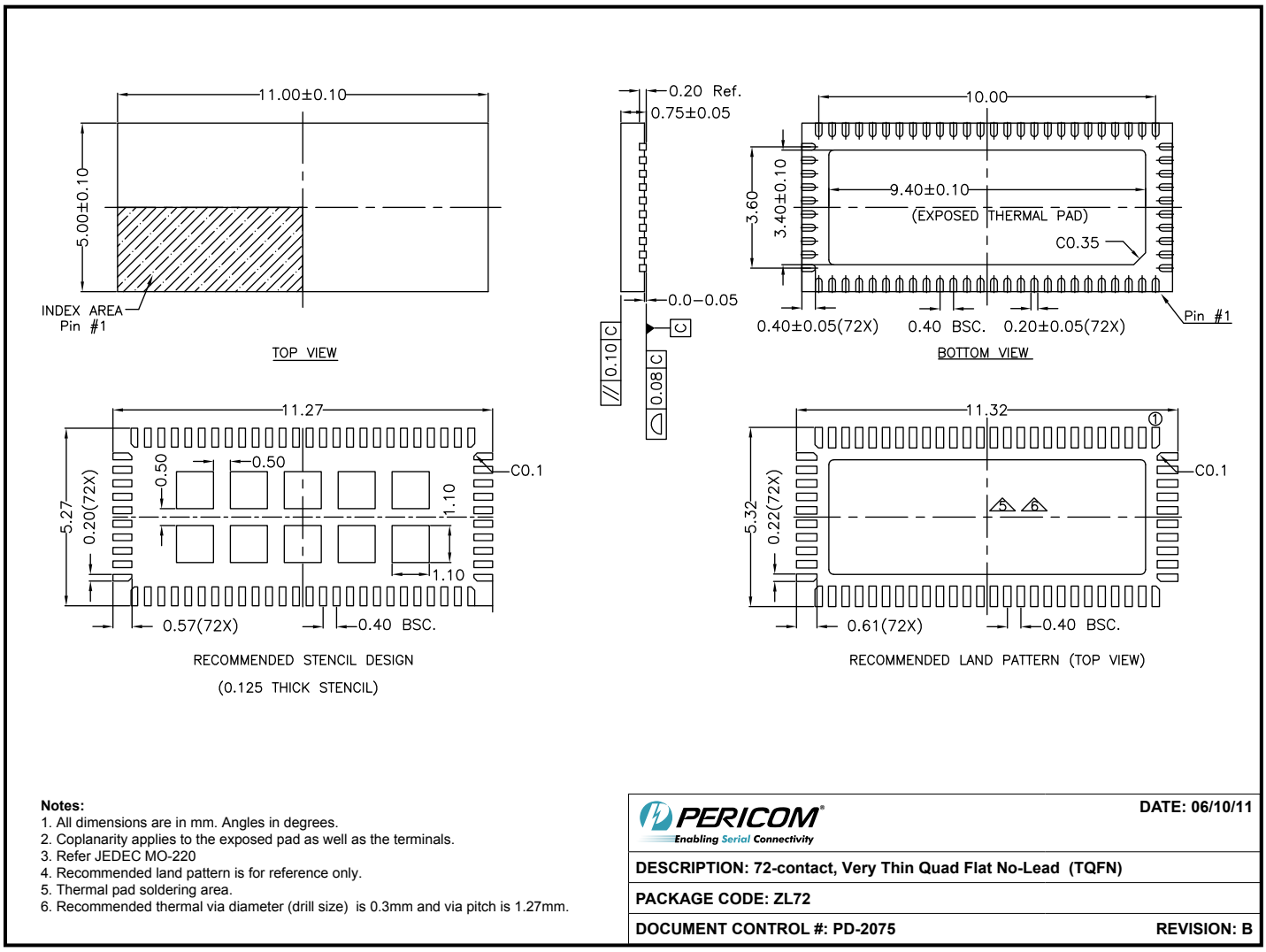


Figure 5-18 Layout Guidance of Stitching Via

6. Mechanical, Packaging, and Orderable Information

6.1 Packaging Mechanical



Notes:
1. All dimensions are in mm. Angles in degrees.
2. Coplanarity applies to the exposed pad as well as the terminals.
3. Refer JEDEC MO-220
4. Recommended land pattern is for reference only.
5. Thermal pad soldering area.
6. Recommended thermal via diameter (drill size) is 0.3mm and via pitch is 1.27mm.

PERICOM Enabling Serial Connectivity	DATE: 06/10/11
DESCRIPTION: 72-contact, Very Thin Quad Flat No-Lead (TQFN)	
PACKAGE CODE: ZL72	
DOCUMENT CONTROL #: PD-2075	REVISION: B

Figure 6-1 72-Pin TQFN Package Mechanical

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

6.2 Part Marking Information

Our standard product mark follows our standard part number ordering information, except for those products with a speed letter code. The speed letter code mark is placed after the package code letter, rather than after the device number as it is ordered. After electrical test screening and speed binning has been completed, we then perform an "add mark" operation which places the speed code letter at the end of the complete part number.

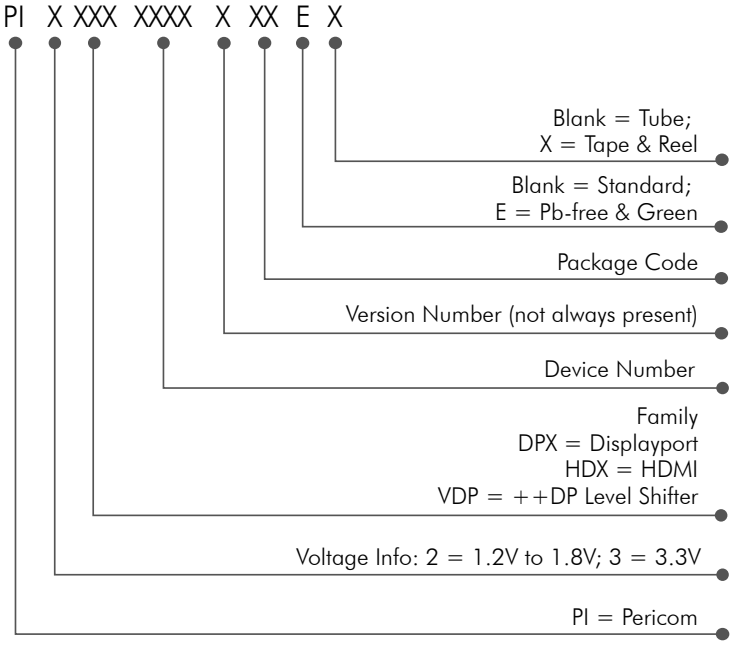


Figure 6-2 Part Marketing Information

6.3 Tape & Reel Materials and Design

Carrier Tape

The Pocketed Carrier Tape is made of Conductive Polystyrene plus Carbon material (or equivalent). The surface resistivity is 10^6Ohm/sq. maximum. Pocket tapes are designed so that the component remains in position for automatic handling after cover tape is removed. Each pocket has a hole in the center for automated sensing if the pocket is occupied or not, thus facilitating device removal. Sprocket holes along the edge of the center tape enable direct feeding into automated board assembly equipment. See Figures 3 and 4 for carrier tape dimensions.

Cover Tape

Cover tape is made of Anti-static Transparent Polyester film.The surface resistivity is 10^7Ohm/Sq. Minimum to 10^{11}Ohm sq. maximum. The cover tape is heat-sealed to the edges of the carrier tape to encase the devices in the pockets. The force to peel back the cover tape from the carrier tape shall be a MEAN value of 20 to 80gm (2N to 0.8N).

Reel

The device loading orientation is in compliance with EIA-481, current version (Figure 2). The loaded carrier tape is wound onto either a 13-inch reel, (Figure 4) or 7-inch reel. The reel is made of Antistatic High-Impact Polystyrene. The surface resistivity 10^7Ohm/sq. minimum to 10^{11}Ohm/sq. max.

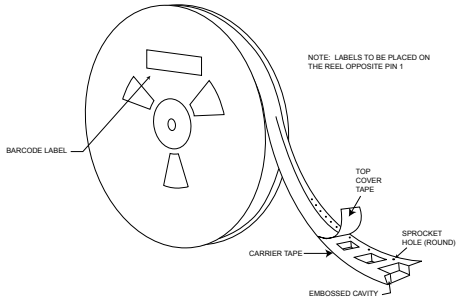


Figure 6-3 Tape & Reel Label Information

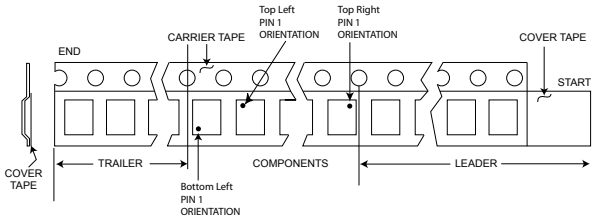


Figure 6-4 Tape Leader and Trailer pin 1 Orientations

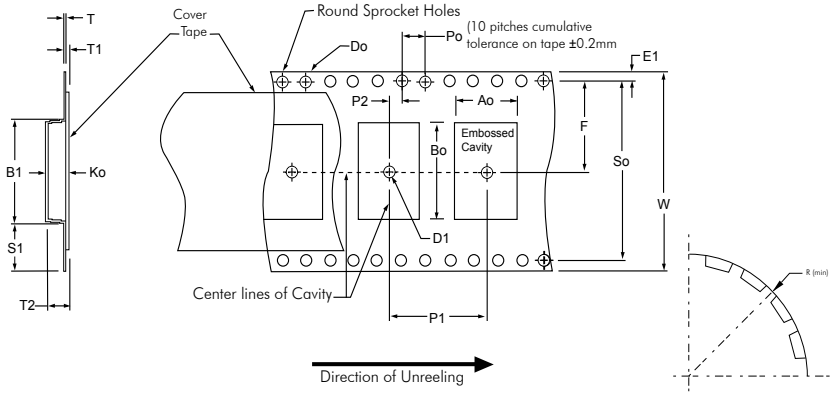


Figure 6-5 Standard Embossed Carrier Tape Dimensions

Constant Dimensions

Tape Size	D0	D1 (Min)	E1	P0	P2	R (See Note 2)	S1 (Min)	T (Max)	T1 (Max)
8mm	1.5 +0.1 -0.0	1.0	1.75 ± 0.1	4.0 ± 0.1	2.0 ± 0.05	25	0.6	0.6	0.1
12mm		1.5				30			
16mm					2.0 ± 0.1				
24mm									
32mm		2.0				50	N/A (See Note 3)		
44mm					2.0 ± 0.15				

Variable Dimensions

Tape Size	P_1	B_1 (Max)	E_2 (Min)	F	So	T_2 (Max.)	W (Max)	A_0, B_0, & K_0
8mm	Specific per package type. Refer to FR-0221 (Tape and Reel Packing Information) or visit www.pericom.com/pdf/gen/tapereel.pdf	4.35	6.25	3.5 ± 0.05	N/A (see note 4)	2.5	8.3	See Note 1
12mm		8.2	10.25	5.5 ± 0.05		6.5	12.3	
16mm		12.1	14.25	7.5 ± 0.1		8.0	16.3	
24mm		20.1	22.25	11.5 ± 0.1		12.0	24.3	
32mm		23.0	N/A	14.2 ± 0.1	28.4± 0.1		32.3	
44mm		35.0	N/A	20.2 ± 0.15	40.4 ± 0.1	16.0	44.3	

NOTES:
1. A0, B0, and K0 are determined by component size. The cavity must restrict lateral movement of component to 0.5mm maximum for 8mm and 12mm wide tape and to 1.0mm maximum for 16,24,32, and 44mm wide carrier. The maximum component rotation within the cavity must be limited to 20o maximum for 8 and 12 mm carrier tapes and 10o maximum for 16 through 44mm.
2. Tape and components will pass around reel with radius "R" without damage.
3. S1 does not apply to carrier width ≥32mm because carrier has sprocket holes on both sides of carrier where Do≥S1.
4. So does not exist for carrier ≤32mm because carrier does not have sprocket hole on both side of carrier.

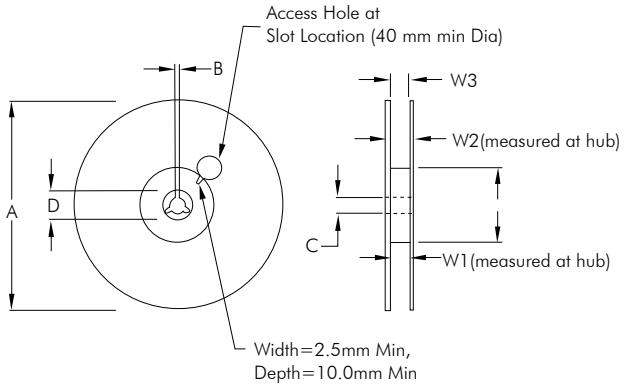


Figure 6-6 Reel dimensions by tape size

Tape Size	A	N (Min) See Note A	W1	W2(Max)	W3	B (Min)	C	D (Min)
8mm	178 ±2.0mm or 330±2.0mm	60 ±2.0mm or 100±2.0mm	8.4 +1.5/-0.0 mm	14.4 mm	Shall Accommodate Tape Width Without Interference	1.5mm	13.0 +0.5/-0.2 mm	20.2mm
12mm			12.4 +2.0/-0.0 mm	18.4 mm				
16mm	330 ±2.0mm	100 ±2.0mm	16.4 +2.0/-0.0 mm	22.4 mm				
24mm			24.4 +2.0/-0.0 mm	30.4 mm				
32mm			32.4 +2.0/-0.0 mm	38.4 mm				
44mm			44.4 +2.0/-0.0 mm	50.4 mm				

NOTE:
A. If reel diameter A=178 ±2.0mm, then the corresponding hub diameter (N(min) will by 60 ±2.0mm. If reel diameter A=330±2.0mm, then the corresponding hub diameter (N(min)) will by 100±2.0mm.

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