

Product Summary

BV _{DSS}	R _{DS(ON)}	I _D T _C = +25°C
40V	5.5mΩ @ V _{GS} = 10V	79A
	7.9mΩ @ V _{GS} = 4.5V	66A

Description and Applications

This MOSFET is designed to meet the stringent requirements of automotive applications. It is qualified to AEC-Q101, supported by a PPAP, and is ideal for use in:

- Wireless charging
- DC-DC converters
- Power management

Features and Benefits

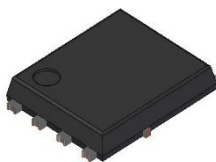
- Rated to +175°C – Ideal for High Ambient Temperature Environments
- 100% Unclamped Inductive Switching (UIS) Test in Production – Ensures More Reliable and Robust End Application
- High Conversion Efficiency
- Low R_{DS(ON)} – Minimizes On-State Losses
- Low Input Capacitance
- Fast Switching Speed
- Wettable Flank for Improved Optical Inspection
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. “Green” Device (Note 3)**
- **The DIODES™ DMTH45M5LPDWQ is suitable for automotive applications requiring specific change control; this part is AEC-Q101 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**

<https://www.diodes.com/quality/product-definitions/>

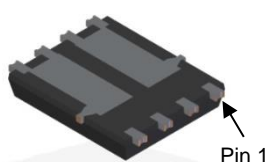
Mechanical Data

- Package: PowerDI®5060-8
- Package Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Finish – Matte Tin Annealed over Copper Leadframe; Solderable per MIL-STD-202, Method 208 (E3)
- Weight: 0.097 grams (Approximate)

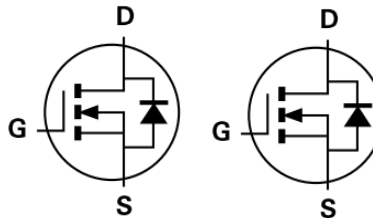
PowerDI5060-8/SWP (Type UXD)



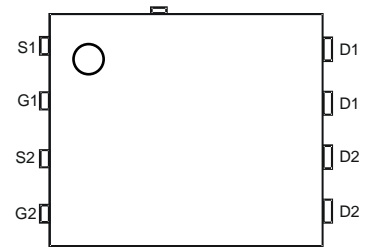
Top View



Bottom View



Internal Schematic



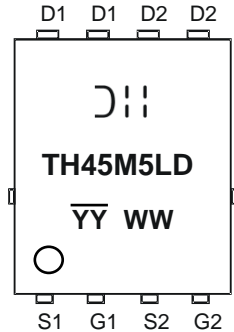
Top View
Pin Configuration

Ordering Information (Note 4)

Part Number	Package	Packing	
		Qty.	Carrier
DMTH45M5LPDWQ-13	PowerDI5060-8/SWP (Type UXD)	2,500	Tape & Reel

- Notes:
1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information



= Manufacturer's Marking
 TH45M5LD = Product Type Marking Code
 $\overline{YY}WW$ = Date Code Marking
 \overline{YY} = Last Two Digits of Year (ex: 22 = 2022)
 WW = Week Code (01 to 53)

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	40	V
Gate-Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current, $V_{GS} = 10\text{V}$ (Note 5)	I_D	$T_C = +25^\circ\text{C}$	79
		$T_C = +100^\circ\text{C}$	55
Pulsed Drain Current (10 μs Pulse, Duty Cycle = 1%)	I_{DM}	316	A
Maximum Continuous Body Diode Forward Current (Note 5)	I_S	79	A
Pulsed Body Diode Forward Current (10 μs Pulse, Duty Cycle = 1%)	I_{SM}	316	A
Avalanche Current $L = 0.1\text{mH}$	I_{AS}	19.8	A
Avalanche Energy $L = 0.1\text{mH}$	E_{AS}	19.6	mJ

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 6)	P_D	3.0	W
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\theta JA}$	50	$^\circ\text{C}/\text{W}$
Total Power Dissipation (Note 5)	P_D	60	W
Thermal Resistance, Junction to Case (Note 5)	$R_{\theta JC}$	2.5	$^\circ\text{C}/\text{W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +175	$^\circ\text{C}$

Notes: 5. Thermal resistance from junction to soldering point (on the exposed drain pad).
 6. Device mounted on FR-4 substrate PC board, 2oz. copper, with thermal bias to bottom layer 1inch square copper plate.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	40	—	—	V	V _{GS} = 0V, I _D = 250μA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	1	μA	V _{DS} = 32V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(TH)}	1.2	—	2.3	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	4.3	5.5	mΩ	V _{GS} = 10V, I _D = 25A
		—	6.1	7.9		V _{GS} = 4.5V, I _D = 15A
Diode Forward Voltage	V _{SD}	—	0.9	1.2	V	V _{GS} = 0V, I _S = 25A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{iss}	—	978	—	pF	V _{DS} = 20V, V _{GS} = 0V f = 1MHz
Output Capacitance	C _{oss}	—	630	—		
Reverse Transfer Capacitance	C _{rss}	—	30	—		
Gate Resistance	R _G	—	1.5	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge (V _{GS} = 4.5V)	Q _g	—	6.3	—	nC	V _{DS} = 20V, I _D = 25A
Total Gate Charge (V _{GS} = 10V)	Q _g	—	13.9	—		
Gate-Source Charge	Q _{gs}	—	3.6	—		
Gate-Drain Charge	Q _{gd}	—	0.9	—		
Turn-On Delay Time	t _{D(ON)}	—	2.8	—	ns	V _{GS} = 10V, V _{DD} = 20V R _G = 3.5Ω, I _D = 25A
Turn-On Rise Time	t _R	—	3.1	—		
Turn-Off Delay Time	t _{D(OFF)}	—	15.6	—		
Turn-Off Fall Time	t _F	—	5.5	—		
Reverse Recovery Time	t _{RR}	—	59	—	ns	I _F = 25A, dI/dt = 100A/μs
Reverse Recovery Charge	Q _{RR}	—	50	—	nC	

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

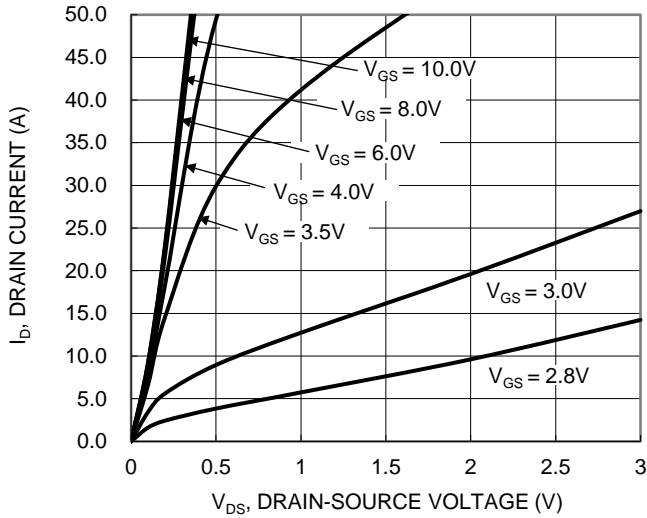


Figure 1. Typical Output Characteristic

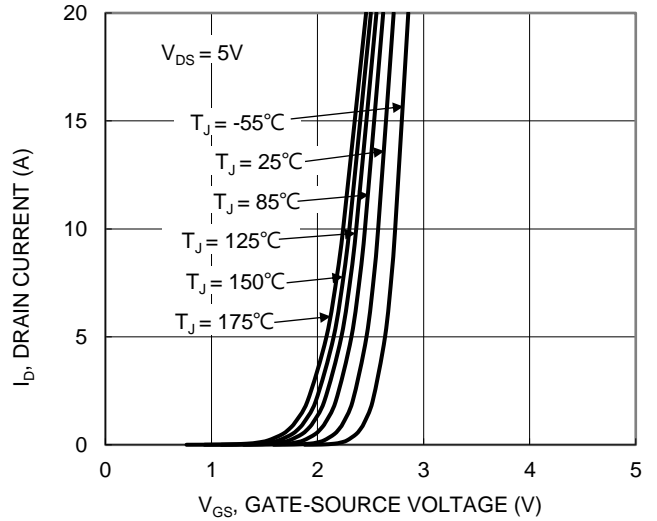


Figure 2. Typical Transfer Characteristic

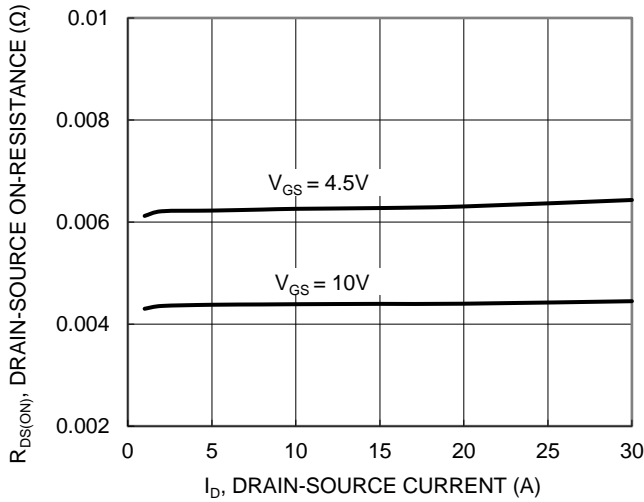


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

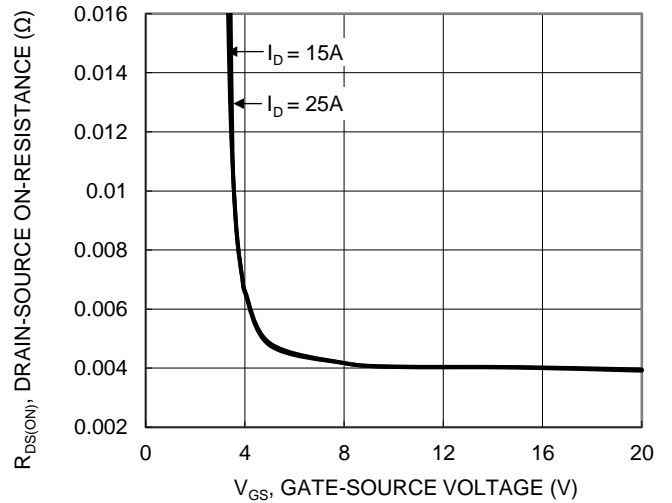


Figure 4. Typical Transfer Characteristic

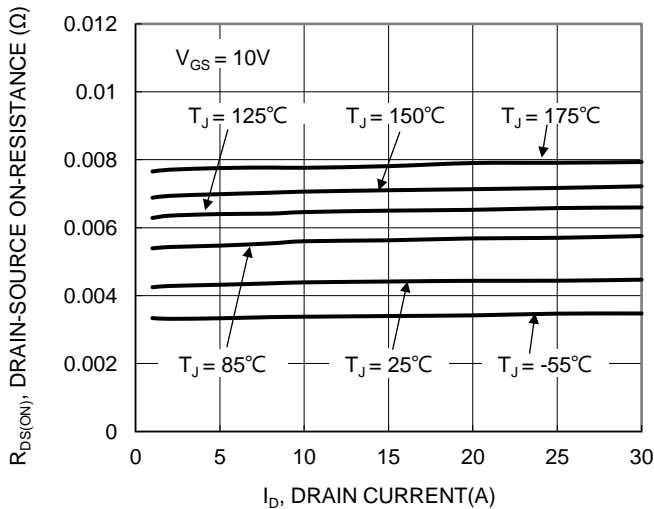


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

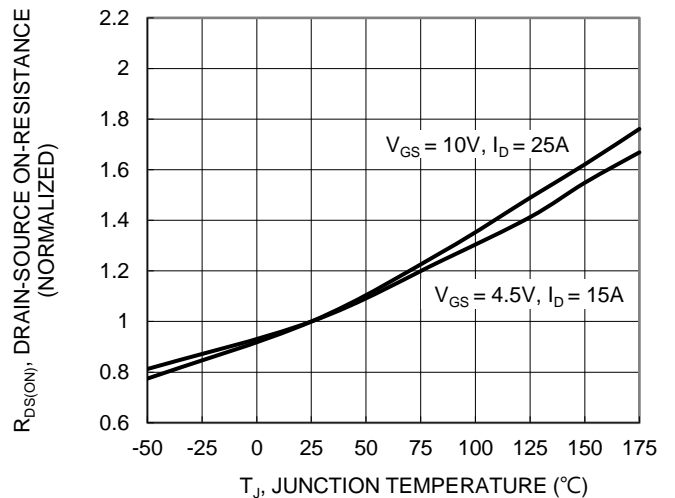


Figure 6. On-Resistance Variation with Junction Temperature

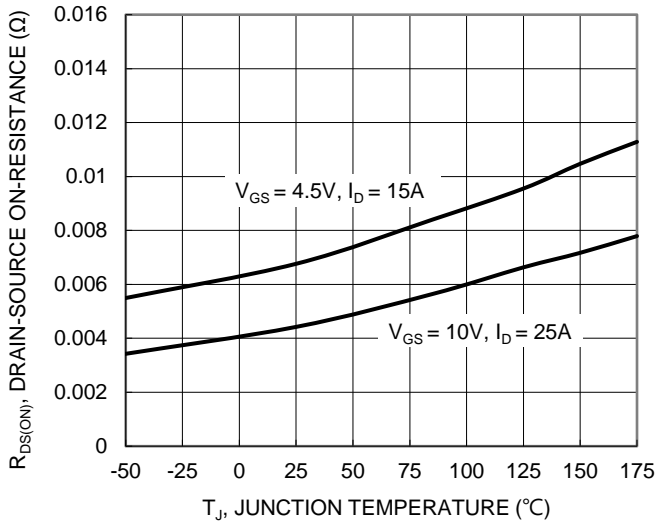


Figure 7. On-Resistance Variation with Junction Temperature

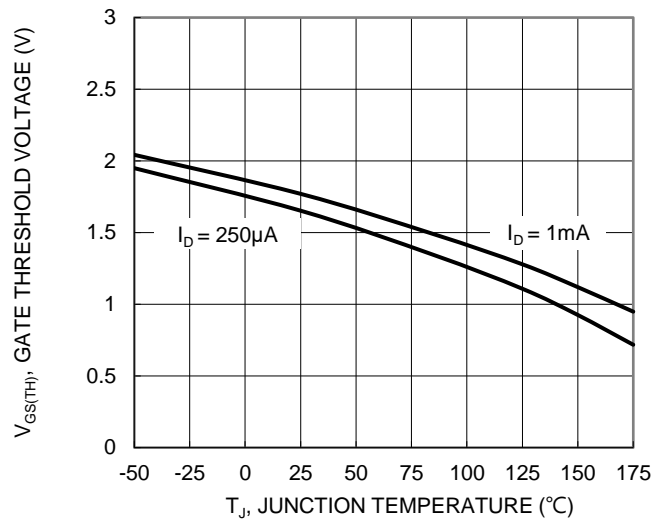


Figure 8. Gate Threshold Variation vs. Junction Temperature

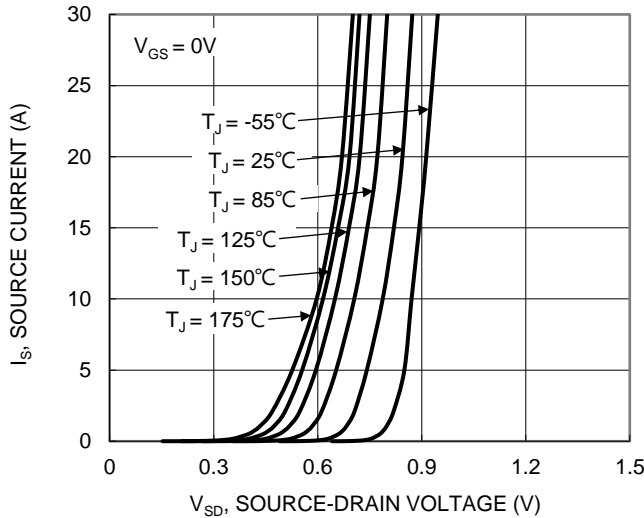


Figure 9. Diode Forward Voltage vs. Current

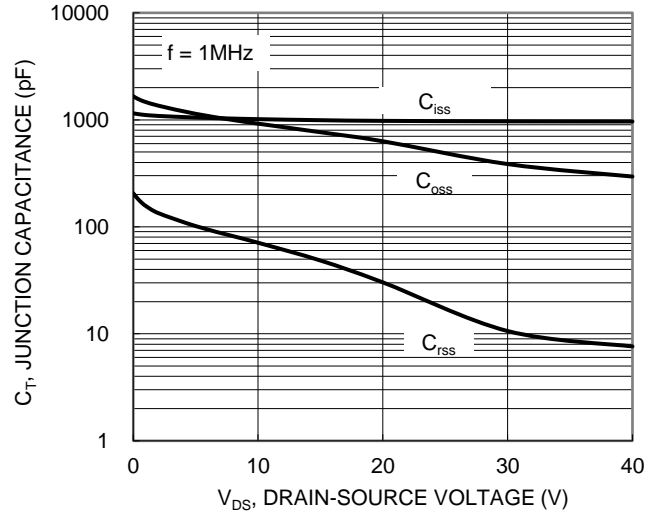


Figure 10. Typical Junction Capacitance

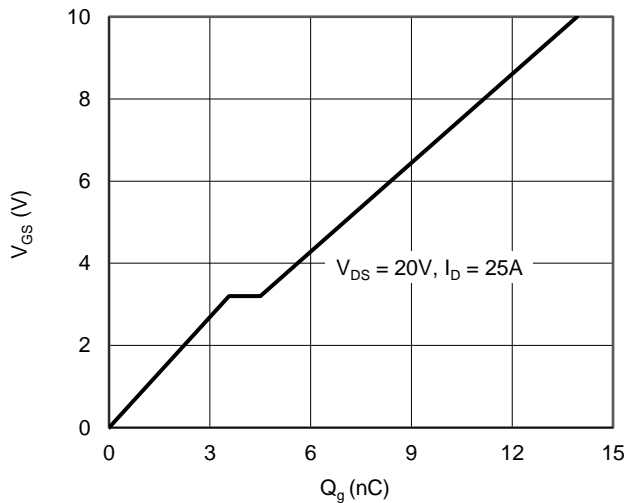


Figure 11. Gate Charge

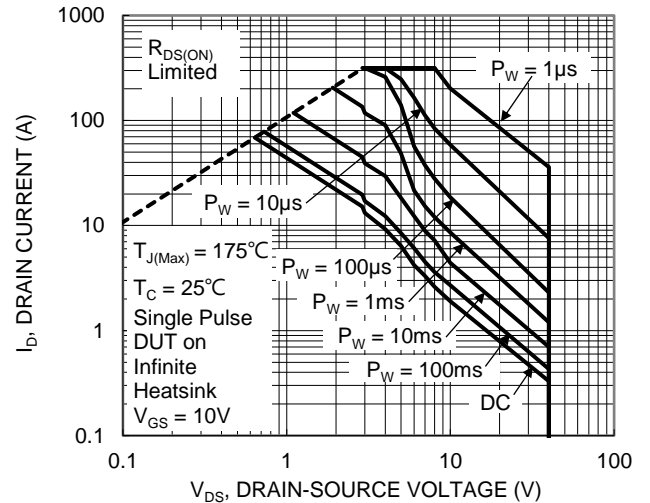


Figure 12. SOA, Safe Operation Area

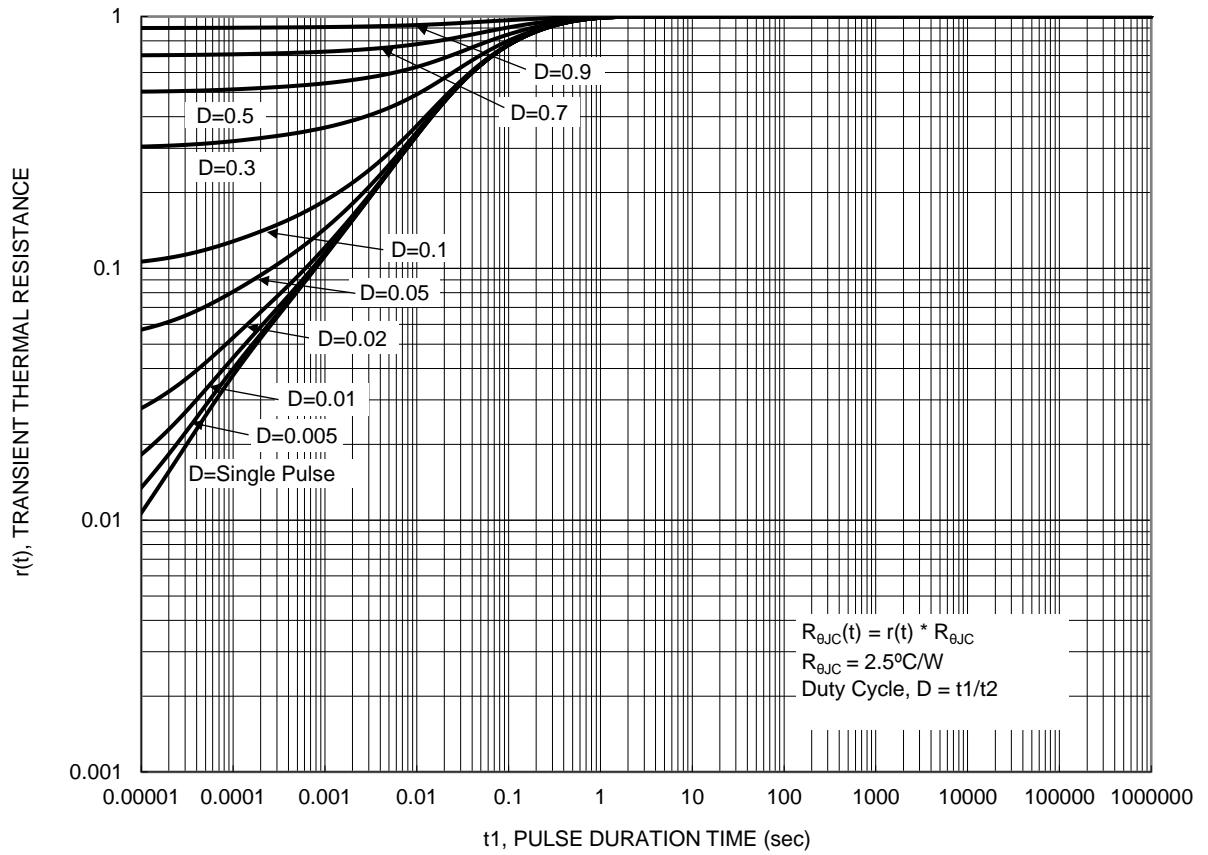
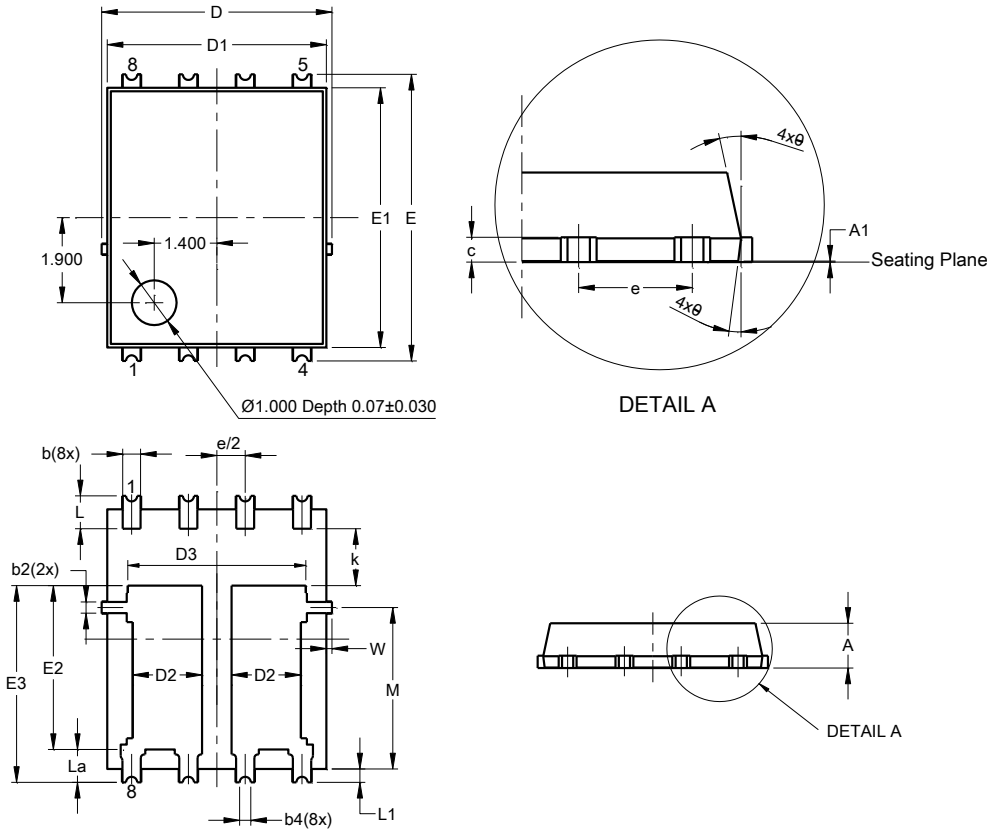


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

PowerDI5060-8/SWP (Type UXD)

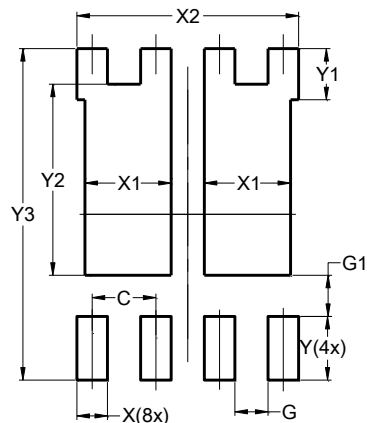


PowerDI5060-8/SWP (Type UXD)			
Dim	Min	Max	Typ
A	0.90	1.10	1.00
A1	0.00	0.05	--
b	0.30	0.50	0.41
b2	0.20	0.35	0.25
b4	0.25REF		
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	1.46	1.66	1.55
D3	3.78	4.18	3.98
E	6.40 BSC		
E1	5.60	6.00	5.80
E2	3.46	3.86	3.66
E2a	4.195	4.595	4.395
e	1.27BSC		
k	1.05	--	--
L	0.635	0.835	0.735
La	0.635	0.835	0.735
L1	0.200	0.400	0.300
M	3.205	4.005	3.605
W	0.025	0.225	0.125
θ	10°	12°	11°
θ1	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

PowerDI5060-8/SWP (Type UXD)



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	1.720
X2	4.420
Y	1.270
Y1	1.020
Y2	3.810
Y3	6.610

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