

### DMTH10H010LPS

### 100V +175°C N-CHANNEL ENHANCEMENT MODE MOSFET PowerDI5060-8

## **Product Summary**

BV <sub>DSS</sub>	R <sub>DS(ON)</sub> Max	I <sub>D</sub> T <sub>C</sub> = +25°C	
100V	8.6mΩ @ V <sub>GS</sub> = 10V	98.4A	

## **Description**

This new generation N-Channel Enhancement Mode MOSFET is designed to minimize  $R_{DS(ON)}$ , yet maintain superior switching performance. This device is ideal for use in notebook battery power management and load switch.

## **Applications**

- Motor Control
- DC-DC Converters
- Power Management

## **Features**

- Rated to +175°C Ideal for High Ambient Temperature Environments
- Thermally Efficient Package-Cooler Running Applications
- High Conversion Efficiency
- Low R<sub>DS(ON)</sub> Minimizes On-State Losses
- Low Input Capacitance
- Fast Switching Speed
- <1.1mm Package Profile Ideal for Thin Applications</li>
- Lead-Free Finish; RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
  - Qualified to AEC-Q101 Standards for High Reliability

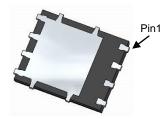
### **Mechanical Data**

- Case: PowerDI<sup>®</sup> 5060-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram Below
- Terminal Finish Matte Tin Annealed over Copper Leadframe.
  Solderable per MIL-STD-202, Method 208 (§3)
- Weight: 0.097 grams (Approximate)

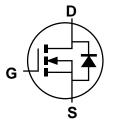
### PowerDI5060-8



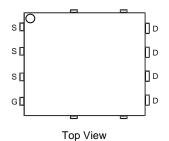
Top View



**Bottom View** 



Internal Schematic



Pin Configuration

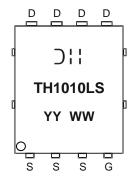
# Ordering Information (Note 4)

Part Number	Case	Packaging
DMTH10H010LPS-13	PowerDI5060-8	2,500 / Tape & Reel

Notes:

- 1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
- See http://www.diodes.com/quality/lead\_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

# Marking Information



| | = Manufacturer's Marking TH1010LS = Product Type Marking Code YYWW = Date Code Marking YY = Last Two Digits of Year (ex: 17= 2017) WW = Week Code (01 to 53)

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# **Maximum Ratings** (@ $T_A = +25^{\circ}C$ , unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			$V_{DSS}$	100	V
Gate-Source Voltage			$V_{GSS}$	±20	V
Continuous Drain Current (/ 40V)	Steady State	$T_A = +25^{\circ}C$ $T_A = +100^{\circ}C$	I <sub>D</sub>	10.8 7.6	А
Continuous Drain Current (V <sub>GS</sub> = 10V)	Steady State	$T_C = +25$ °C $T_C = +100$ °C	I <sub>D</sub>	98.4 69.6	А
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)	I <sub>DM</sub>	250	Α		
Maximum Continuous Body Diode Forward Current			Is	95	Α
Pulsed Body Diode Forward Current (10µs Pulse, Duty Cycle = 1%)			I <sub>SM</sub>	250	Α
Avalanche Current, L=0.3mH			I <sub>AS</sub>	15	Α
Avalanche Energy, L=0.3mH			E <sub>AS</sub>	33.7	mJ

## **Thermal Characteristics**

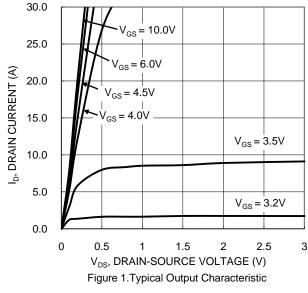
Characteristic	Symbol	Value	Unit	
Total Power Dissipation (Note 5)		$P_{D}$	1.5	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	99	°C/W
Total Power Dissipation	$T_C = +25^{\circ}C$	P <sub>D</sub>	125	W
Thermal Resistance, Junction to Case	$R_{ heta JC}$	1.2	°C/W	
Operating and Storage Temperature Range	T <sub>J,</sub> T <sub>STG</sub>	-55 to +175	°C	

## Electrical Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 6)							
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	100	_	_	V	$V_{GS} = 0V, I_D = 1mA$	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	_	_	1	μA	$V_{DS} = 80V, V_{GS} = 0V$	
Gate-Source Leakage	I <sub>GSS</sub>	_	_	±100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 6)	•						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	1.4	1.9	3	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	
		_	6.9	8.6		$V_{GS} = 10V, I_D = 13A$	
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	_	7.5	12	mΩ	V <sub>GS</sub> = 6V, I <sub>D</sub> = 13A	
		_	10	20		$V_{GS} = 4.5V, I_D = 5A$	
Diode Forward Voltage	$V_{SD}$	_	0.8	1.3	V	$V_{GS} = 0V, I_{S} = 13A$	
DYNAMIC CHARACTERISTICS (Note 7)							
Input Capacitance	Ciss	_	2592	_		V <sub>DS</sub> = 50V, V <sub>GS</sub> = 0V f = 1MHz	
Output Capacitance	Coss	1	792	1	pF		
Reverse Transfer Capacitance	Crss		45			1 - 11/11/12	
Gate Resistance	$R_g$	_	2	_	Ω	$V_{DS} = 0V$ , $V_{GS} = 0V$ , $f = 1MHz$	
Total Gate Charge	Qg	_	53.7	_			
Gate-Source Charge	$Q_{gs}$	_	10.6	_	nC	$V_{DD} = 50V, I_D = 13A,$	
Gate-Drain Charge	Q <sub>gd</sub>	_	8.2	_		$V_{GS} = 10V$	
Turn-On Delay Time	t <sub>D(ON)</sub>	_	11.6	_			
Turn-On Rise Time	t <sub>R</sub>	_	14.1	_		$V_{DD} = 50V, V_{GS} = 10V,$	
Turn-Off Delay Time	t <sub>D(OFF)</sub>	_	42.9	_	ns	$I_D = 13A$ , $R_g = 6\Omega$	
Turn-Off Fall Time	t <sub>F</sub>	_	22	_			
Reverse Recovery Time	t <sub>RR</sub>	_	49.8	_	ns	100 11/14 1000//	
Reverse Recovery Charge	Q <sub>RR</sub>	_	85.1	_	nC	$I_F = 13A$ , di/dt = 100A/ $\mu$ s	

5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.6. Short duration pulse test used to minimize self-heating effect.7. Guaranteed by design. Not subject to product testing.





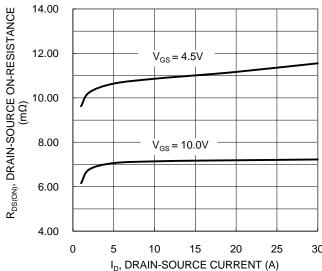


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

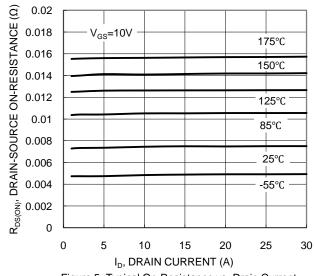
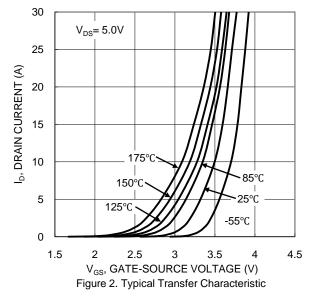
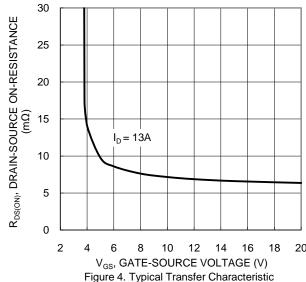


Figure 5. Typical On-Resistance vs. Drain Current and Temperature





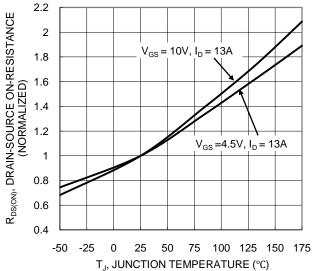


Figure 6. On-Resistance Variation with Temperature



75 100 125 150 175



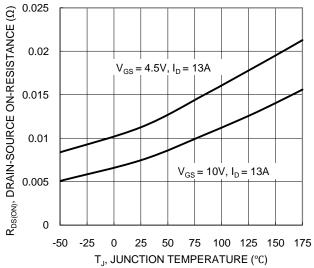


Figure 7. On-Resistance Variation with Temperature

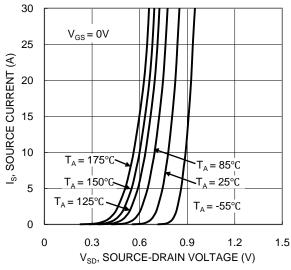
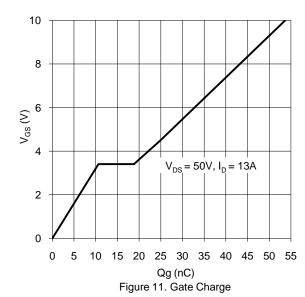


Figure 9. Diode Forward Voltage vs. Current



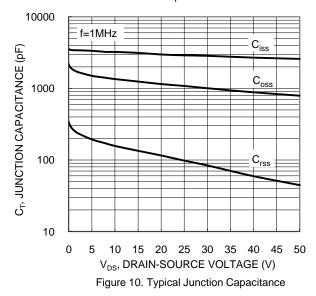
3 GATE THRESHOLD VOLTAGE (V) 2.8 2.6 2.4 2.2  $I_D = 1mA$ 2 1.8 1.6  $I_{D} = 250 \mu A$ 1.4 1.2 V<sub>GS(ТН)</sub>, (

8.0 0.6

-25

T<sub>J</sub>, JUNCTION TEMPERATURE (°C) Figure 8. Gate Threshold Variation vs. Junction Temperature

25 50



1000  $R_{DS(ON)}$  LIMITED 100 l<sub>D</sub>, DRAIN CURRENT (A) T<sub>J(MAX)</sub>=150°C T<sub>C</sub>=25°C =10ms P<sub>w</sub>=100ms Single Pulse DUT on infinite heatsink V<sub>GS</sub>=10V 0.01 0.1 1000 10 100 V<sub>DS</sub>, DRAIN-SOURCE VOLTAGE (V) Figure 12. SOA, Safe Operation Area



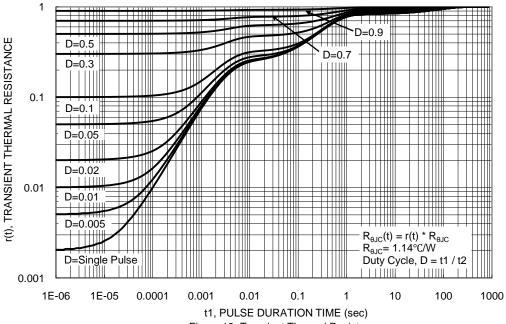


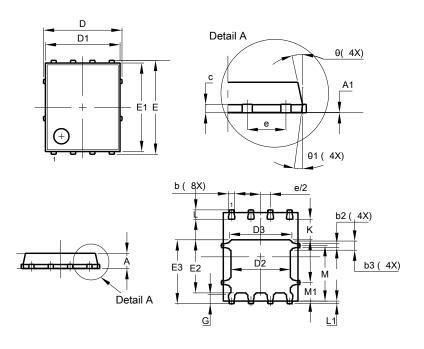
Figure 13. Transient Thermal Resistance



## **Package Outline Dimensions**

Please see http://www.diodes.com/package-outlines.html for the latest version.

### PowerDI5060-8

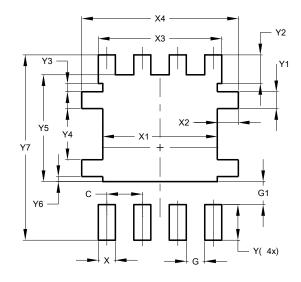


PowerDI5060-8					
Dim	Min	Max	Тур		
Α	0.90	1.10	1.00		
A1	0.00	0.05	_		
b	0.33	0.51	0.41		
b2	0.200	0.350	0.273		
b3	0.40	0.80	0.60		
С	0.230	0.330	0.277		
D	į,	5.15 BSC			
D1	4.70	5.10	4.90		
D2	3.70	4.10	3.90		
D3	3.90	4.30	4.10		
Е	(	6.15 BSC			
E1	5.60	6.00	5.80		
E2	3.28	3.68	3.48		
E3	3.99	4.39	4.19		
е	•	1.27 BSC	•		
G	0.51	0.71	0.61		
K	0.51	-	-		
L	0.51	0.71	0.61		
L1	0.100	0.200	0.175		
М	3.235	4.035	3.635		
M1	1.00	1.40	1.21		
θ	10°	12º	11º		
θ1	6º	8°	7º		
All	All Dimensions in mm				

# **Suggested Pad Layout**

Please see http://www.diodes.com/package-outlines.html for the latest version.

### PowerDI5060-8



Dimensions	Value (in mm)				
C	1.270				
G	0.660				
G1	0.820				
Х	0.610				
X1	4.100				
X2	0.755				
Х3	4.420				
X4	5.610				
Υ	1.270				
Y1	0.600				
Y2	1.020				
Y3	0.295				
Y4	1.825				
Y5	3.810				
Y6	0.180				
Y7	6.610				



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