

60V N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV _{DSS}	R _{DS(ON)} Max	I _D T _C = +25°C
60V	8.3mΩ @ V _{GS} = 10V	52.1A
607	12.5m Ω @ V _{GS} = 4.5V	42.4A

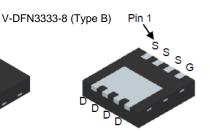
Features and Benefits

- 100% Unclamped Inductive Switching (UIS) Test in Production Ensures More Reliable and Robust End Application
- High Conversion Efficiency
- Low R_{DS(ON)} Minimizes On State Losses
- Low Input Capacitance
- Fast Switching Speed
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/

Description and Applications

This new generation N-channel enhancement mode MOSFET is designed to minimize $R_{DS(ON)}$ yet maintain superior switching performance. This device is ideal for use in notebook battery power management and load switch.

- Synchronous Rectifier
- Power Management Functions
- DC-DC Converters

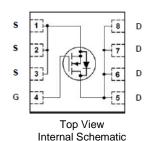


Top View

Bottom View

Mechanical Data

- Case: V-DFN3333-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Below Diagram
- Terminals: Finish—NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 (e4)
- Weight: 0.027 grams (Approximate)



G S Equivalent Circuit

D

Ordering Information (Note 4)

Part Number	Case	Packaging
DMT69M5LCG-7	V-DFN3333-8 (Type B)	2,000/Tape & Reel
DMT69M5LCG -13	V-DFN3333-8 (Type B)	3,000/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/

Marking Information



695 = Product Type Marking Code YWX = Date Code Marking Y = Year (ex: 0 = 2020)

W = Week (ex: a = week 27; z represents week 52 and 53)

X = Internal Code (ex: U = Monday)

Date Code Key

Date Code Rey												
Year	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
Code	0	1	2	3	4	5	6	7	8	9	0	1
Week		1-	26			27	-52			5	3	
Code	A-Z			A-Z a-z					7	Z		
Internal Code	Sur	n	Mon		Tue	W	ed	Thu		Fri		Sat
Code	Т		IJ		V	\	N	X		Υ		7



Maximum Ratings (@TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit		
Drain-Source Voltage	VDSS	60	V		
Gate-Source Voltage			V _{GSS}	±20	V
Continuous Drain Current, $V_{GS} = 10V$ (Note 6) Steady $T_A = +25^{\circ}C$ State $T_A = +70^{\circ}C$			lο	14.6 11.7	А
Continuous Drain Current, Vgs = 10V (Note 7)	lο	52.1 41.7	А		
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%	l _{DM}	208	Α		
Maximum Continuous Body Diode Forward Current	Is	52	Α		
Pulsed Body Diode Forward Current (10µs Pulse, D	I _{SM}	208	Α		
Avalanche Current, L = 0.1mH	las	27.4	Α		
Avalanche Energy, L = 0.1mH			Eas	37.5	mJ

Thermal Characteristics (@TA = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	T _A = +25°C	PD	1.37	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	RθJA	91	°C/W
Total Power Dissipation (Note 6)	T _A = +25°C	P _D	2.64	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	47.3	°C/W
Thermal Resistance, Junction to Case (Note 7)		R _θ JC	3.7	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C	

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 8)							
Drain-Source Breakdown Voltage	BV _{DSS}	60	_	_	V	$V_{GS} = 0V, I_D = 250\mu A$	
Zero Gate Voltage Drain Current	I _{DSS}	_	_	1	μΑ	$V_{DS} = 48V, V_{GS} = 0V$	
Gate-Source Leakage	Igss	_	_	±100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$	
ON CHARACTERISTICS (Note 8)							
Gate Threshold Voltage	V _{GS(TH)}	1.4	_	2.5	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	
Static Drain-Source On-Resistance	0	_	6.1	8.3	mΩ	V _{GS} = 10V, I _D = 13.5A	
Static Drain-Source On-Resistance	RDS(ON)	_	8.7	12.5	11177	V _{GS} = 4.5V, I _D = 11.5A	
Diode Forward Voltage	V_{SD}	_	0.7	1.2	V	V _G S = 0V, I _S = 1A	
DYNAMIC CHARACTERISTICS (Note 9)					•		
Input Capacitance	Ciss		1406	_		$V_{DS} = 30V, V_{GS} = 0V,$ f = 1MHz	
Output Capacitance	Coss	_	540	_	pF		
Reverse Transfer Capacitance	Crss	_	52	_		1 = 11011 12	
Gate Resistance	Rg	_	1.85	_	Ω	$V_{DS} = 0V$, $V_{GS} = 0V$, $f = 1MHz$	
Total Gate Charge (V _{GS} = 10V)	Qg	_	28.4	_			
Total Gate Charge (V _{GS} = 4.5V)	Qg	_	15.4	_	nC	V 00V I 40.5A	
Gate-Source Charge	Qgs	_	2.4	_	nc nc	V _{DS} = 30V, I _D = 13.5A	
Gate-Drain Charge	Qgd	_	9.0	_			
Turn-On Delay Time	tD(ON)	_	10.5	_			
Turn-On Rise Time	t _R	_	49.0	_		$V_{DD} = 30V, V_{GS} = 10V,$	
Turn-Off Delay Time	tD(OFF)		30.9	_	ns	$I_D = 13.5A, R_G = 6\Omega$	
Turn-Off Fall Time	tr	_	79.5	_			
Reverse Recovery Time	t _{RR}	_	26.7	_	ns	1 10 54 11/11 0004/	
Reverse Recovery Charge	Qrr	_	44.8	_	nC	IF = 13.5A, di/dt = 300A/μs	

5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

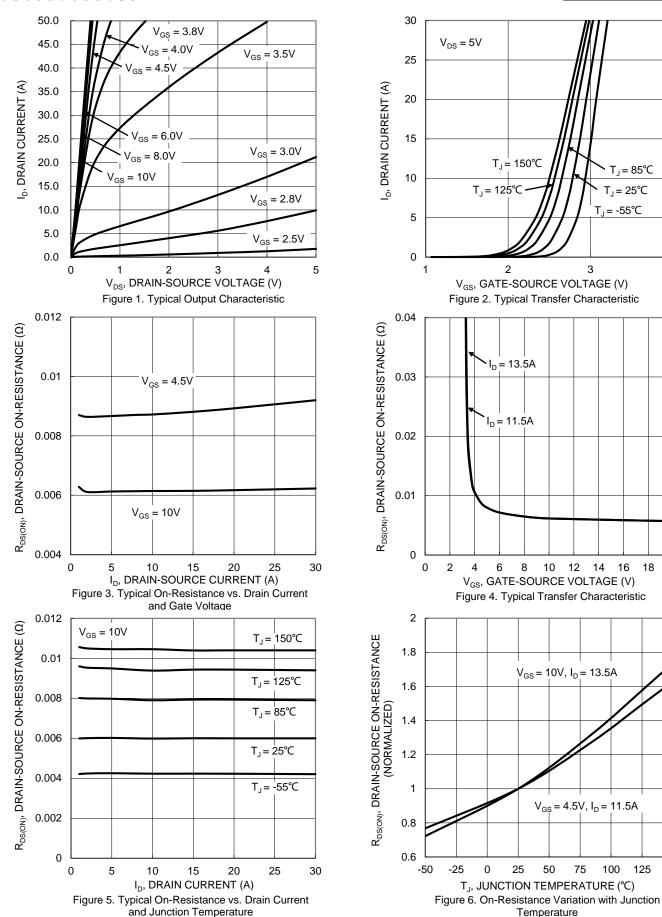
^{6.} Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

^{7.} Thermal resistance from junction to soldering point (on the exposed drain pad).
8. Short duration pulse test used to minimize self-heating effect.

^{9.} Guaranteed by design. Not subject to product testing.







125

150



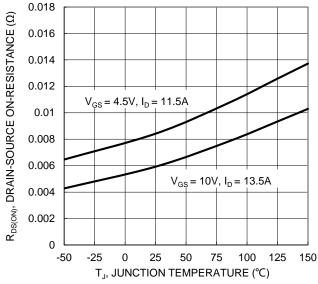


Figure 7. On-Resistance Variation with Junction Temperature

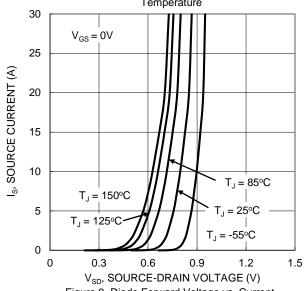


Figure 9. Diode Forward Voltage vs. Current

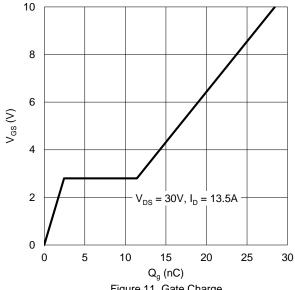


Figure 11. Gate Charge

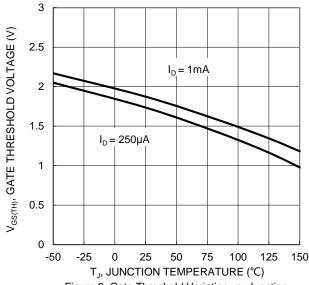


Figure 8. Gate Threshold Variation vs. Junction Temperature

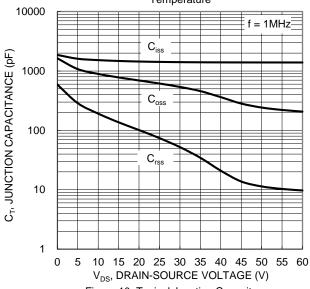


Figure 10. Typical Junction Capacitance

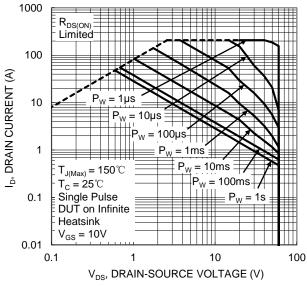


Figure 12. SOA, Safe Operation Area



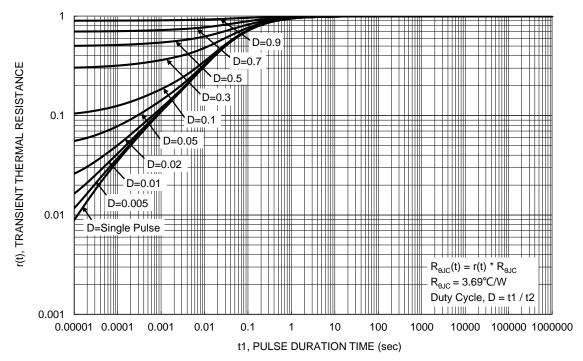


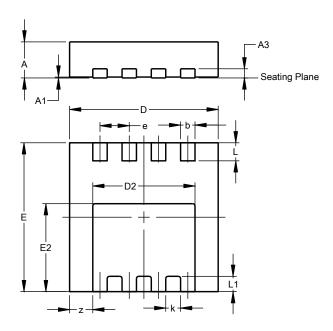
Figure 13. Transient Thermal Resistance



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

V-DFN3333-8 (Type B)

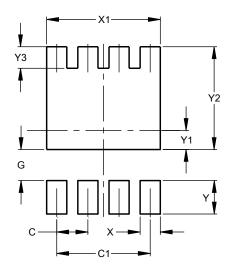


V-DFN3333-8 (Type B)							
Dim	Min Max Typ						
Α	0.75	0.85	0.80				
A1	0.00	0.05	0.02				
A3	-		0.203				
b	0.27	0.37	0.32				
D	3.25	3.35	3.30				
D2	2.17	2.37	2.27				
Е	3.25	3.35	3.30				
E2	1.85	2.05	1.95				
е			0.65				
k	-		0.33				
L	0.35	0.45	0.40				
L1			0.34				
Z			0.515				
All Dimensions in mm							

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

V-DFN3333-8 (Type B)



Dimensions	Value (in mm)
С	0.650
C1	1.950
G	0.650
X	0.420
X1	2.370
Y	0.700
Y1	0.400
Y2	2.150
Y3	0.450



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