



### P-CHANNEL ENHANCEMENT MODE MOSFET

## **Product Summary**

BV <sub>DSS</sub>	RDS(ON) Max	I <sub>D</sub> T <sub>A</sub> = +25°C
-25V	40mΩ @ V <sub>GS</sub> = -4.5V	-5.2

## **Description and Applications**

This new generation MOSFET is designed to minimize the on-state resistance (RDS(ON)) yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Battery management
- Load switches
- Battery protections

## **Features and Benefits**

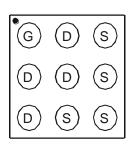
- Low Q<sub>q</sub> & Q<sub>qd</sub>
- Small Footprint 1.5mm x 1.5mm
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.

https://www.diodes.com/quality/product-definitions/

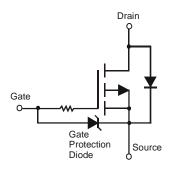
### **Mechanical Data**

- Package: X2-DSN1515-9 (Note 4)
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal: Finish SnAg over Cu Pillar @1
- Solder Cap Material: SnAg (Ag: 2.0+/-0.5%)
- Terminal Connections: See Diagram Below
- UBM Size: 320µm
- Weight: 0.0015 grams (Approximate)





Top View Pin Configuration



**Equivalent Circuit** 

## **Ordering Information (Note 5)**

Part Number	Backago	Packing		
Fait Number	Package	Qty. Carrier		
DMP2541UCP9-7	X2-DSN1515-9 (Type B)	3,000	Tape & Reel	

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. Device with exposed silicon sidewall is non-isolated area.
- 5. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

# **Marking Information**



3M = Product Type Marking Code YW = Date Code Marking Y or Y = Year (ex: 2 = 2022)

W or  $\overline{W}$  = Week (ex: a = week 27; z represents week 52 and 53)

Date Code Key

Year	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033
Code	2	3	4	5	6	7	8	9	0	1	2	3
Week	Week 1-26			ek 1-26 27-52					5	i3		
Code	de A-Z			a-	-Z				Z			



# **Maximum Ratings** (@ $T_A = +25^{\circ}C$ , unless otherwise specified.)

Characteristic		Symbol	Value	Unit	
Drain-Source Voltage		VDSS	-25	V	
Gate-Source Voltage	V <sub>GSS</sub>	-6	V		
Continuous Drain Current (Note 6) V <sub>GS</sub> = -4.5V	Steady State	T <sub>A</sub> = +25°C T <sub>A</sub> = +70°C	l <sub>D</sub>	-3.8 -3.0	А
Continuous Drain Current (Note 7) Vos = -4 5V		T <sub>A</sub> = +25°C T <sub>A</sub> = +70°C	lo	-5.2 -4.2	А
Pulsed Drain Current (Pulse Duration 10µs, Duty C	ycle ≤ 1%	)	I <sub>DM</sub>	-35	Α
Continuous Source Pin Current (Note 7)		Is	-1.5	Α	
Pulsed Source Pin Current (Pulse Duration 10µs, D	Outy Cycle	≤ 1%)	Ism	-35	A

# Thermal Characteristics (@ $T_A = +25$ °C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 6)	P <sub>D</sub>	0.9	W
Total Power Dissipation (Note 7)	PD	1.67	W
Thermal Resistance, Junction to Ambient (Note 6)	$R_{ heta JA}$	139	°C/W
Thermal Resistance, Junction to Ambient (Note 7)	RθJA	75	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

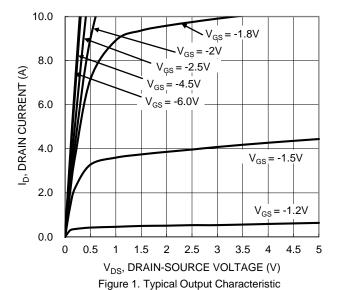
# **Electrical Characteristics** (@TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-25	_	_	V	$V_{GS} = 0V, I_{D} = -250\mu A$
Zero Gate Voltage Drain Current @Tc = +25°C	IDSS		_	-1	μA	V <sub>DS</sub> = -20V, V <sub>GS</sub> = 0V
Gate-Source Leakage	Igss		_	-100	nA	$V_{GS} = -6V$ , $V_{DS} = 0V$
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	-0.4	-0.78	-1.1	V	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$
			28	40		$V_{GS} = -4.5V$ , $I_{D} = -2A$
Static Drain-Source On-Resistance	RDS(ON)	_	36	50	mΩ	$V_{GS} = -2.5V, I_{D} = -2A$
			51	60		$V_{GS} = -1.8V, I_{D} = -2A$
Diode Forward Voltage (Note 6)	VsD	_	-0.74	-1	V	V <sub>G</sub> S = 0V, I <sub>S</sub> = -2A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	Ciss		566	_	pF	101/11/ 01/
Output Capacitance	Coss		343	_	pF	V <sub>DS</sub> = -10V, V <sub>GS</sub> = 0V, -f = 1.0MHz
Reverse Transfer Capacitance	Crss		20	_	pF	1 – 1.01/11/12
Series Gate Resistance	Rg		12.1	_	Ω	$V_{DS} = 0V$ , $V_{GS} = 0V$ , $f = 1.0MHz$
Total Gate Charge	Qg		4.7	_	nC	\\ 45\\\\ 40\\
Gate-Source Charge	Qgs		0.6	_	nC	Vgs = -4.5V, Vps = -10V, -In = -2A
Gate-Drain Charge	$Q_{gd}$		1.0	_	nC	ID = -2A
Turn-On Delay Time	td(ON)		3.4	_	ns	
Turn-On Rise Time	t <sub>R</sub>		6.5	_	ns	$V_{DD} = -10V$ , $V_{GS} = -4.5V$ ,
Turn-Off Delay Time	t <sub>D(OFF)</sub>	_	55	_	ns	$I_{DS} = -2A$ , $R_g = 2\Omega$
Turn-Off Fall Time	tF		43	_	ns	

Notes:

- Device mounted on FR-4 PCB with minimum recommended pad layout.
   Device mounted on FR-4 material with 1inch² (6.45cm²), 2oz. (0.071mm thick) Cu.
   Short duration pulse test used to minimize self-heating effect.







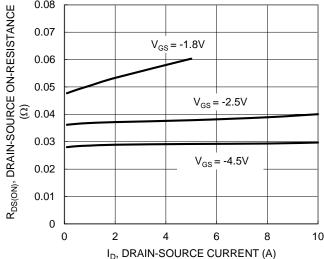


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

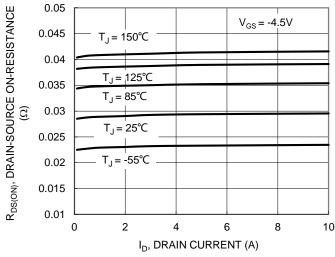


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

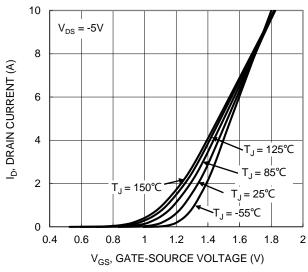


Figure 2. Typical Transfer Characteristic

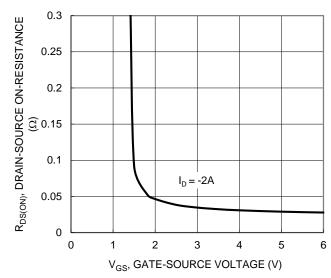


Figure 4. Typical Transfer Characteristic

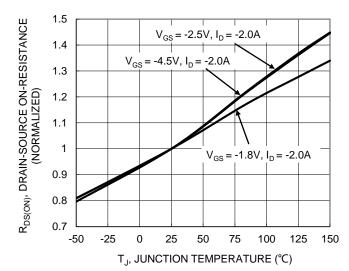


Figure 6. On-Resistance Variation with Junction Temperature



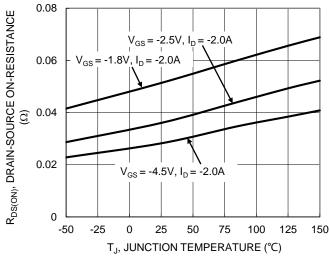


Figure 7. On-Resistance Variation with Junction Temperature

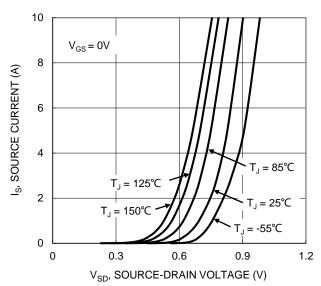


Figure 9. Diode Forward Voltage vs. Current

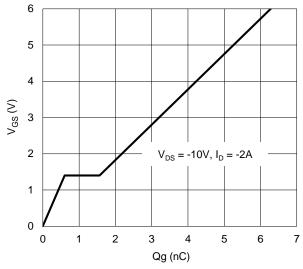


Figure 11. Gate Charge

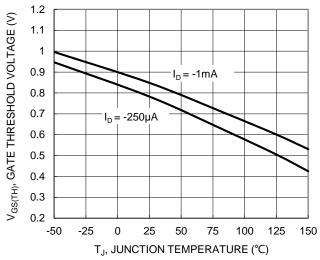


Figure 8. Gate Threshold Variation vs. Junction Temperature

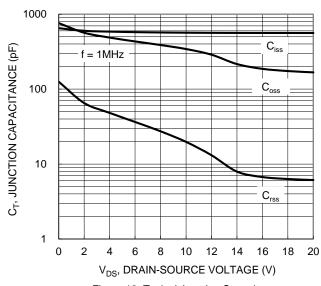


Figure 10. Typical Junction Capacitance

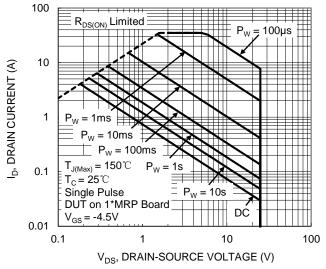


Figure 12. SOA, Safe Operation Area



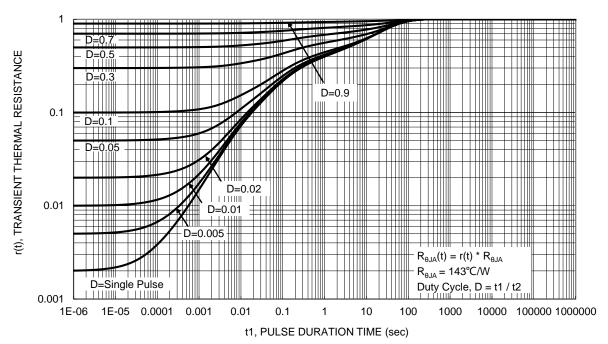


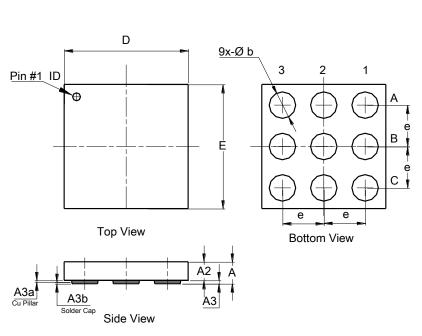
Figure 13. Transient Thermal Resistance

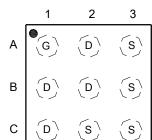


## **Package Outline Dimensions**

Please see http://www.diodes.com/package-outlines.html for the latest version.

### X2-DSN1515-9 (Type B)





Pin Assignment					
A1	G				
A2, B1, B2, C1	D				
A3, B3, C2, C3	S				
A3, B3, C2, C3	J				

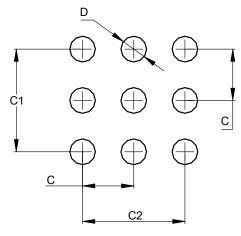
Top View

X2-DSN1515-9 (Type B)							
Dim	Min	Max	Тур				
Α	-	0.32	0.265				
A2	1		0.225				
A3	0.034	0.046	0.040				
A3a	0.015	0.025	0.020				
A3b	0.017	0.023	0.02				
p	0.27	0.37	0.32				
D	1.45	1.53	1.50				
Е	1.45	1.53	1.50				
е	1		0.50				
Co- planarity	<u>&lt;</u> 0.005						
All Dimensions in mm							

## **Suggested Pad Layout**

Please see http://www.diodes.com/package-outlines.html for the latest version.

### X2-DSN1515-9 (Type B)



Dimensions	Value (in mm)
С	0.50
C1	1.00
C2	1.00
ח	0.25



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