



#### **DUAL P-CHANNEL ENHANCEMENT MODE MOSFET**

### **Product Summary**

BV <sub>DSS</sub>	RDS(ON) Max	ID MAX TA = +25°C
-20V	$75m\Omega$ @ V <sub>GS</sub> = -4.5V	-3.2A
-200	110m $\Omega$ @ V <sub>GS</sub> = -2.5V	-2.9A

### **Description and Applications**

This MOSFET is designed to minimize the on-state resistance (RDS(ON)) yet maintain superior switching performance, which makes it ideal for high-efficiency power management applications.

- Load switches
- Power management functions
- Portable power adaptors

#### **Features**

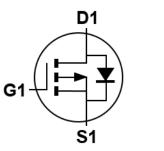
- PCB Footprint of 4mm<sup>2</sup>
- Low On-Resistance
- Low Input Capacitance
- Low Profile, 0.6mm Maximum Height
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- An automotive-compliant part is available under separate datasheet (DMP2110UFDBQ)

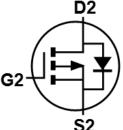
#### Mechanical Data

- Package: U-DFN2020-6
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208@4
- Terminals Connections: See Diagram Below
- Weight: 0.0065 grams (Approximate)



**Bottom View** 





Internal Schematic

### Ordering Information (Note 4)

Part Number	Pankaga	Packing			
Fait Number	Package	Qty.	Carrier		
DMP2110UFDB-7	U-DFN2020-6 (Type B)	3,000	Tape & Reel		
DMP2110UFDB-13	U-DFN2020-6 (Type B)	10,000	Tape & Reel		

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + CI) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

## **Marking Information**



H6 = Product Type Marking Code YWX = Date Code Marking Y = Year (ex: 3 = 2023)W = Week (ex: a = Week 27; z Represents Week 52 and 53)

X = Internal Code (ex: U = Monday)

Date Code Key

Year	2019	-	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032
Code	9	-	3	4	5	6	7	8	9	0	1	2

Week	1-26	27-52	53
Code	A-Z	a-z	z

Ī	Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat
Ī	Code	Т	U	V	W	X	Y	Z



### **Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit		
Drain-Source Voltage	VDSS	-20	V		
Gate-Source Voltage	Vgss	±12	V		
Continuous Drain Current (Note 6) Vgs = -4.5V	Steady State	$T_A = +25$ °C $T_A = +70$ °C	ID	-3.2 -2.6	А
Maximum Continuous Body Diode Forward Current (N	Is	-1.05	А		
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)	I <sub>DM</sub>	-15	А		

# **Thermal Characteristics**

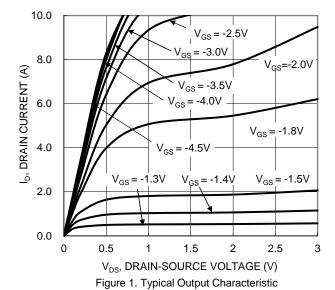
Characteristic	Symbol	Value	Unit	
Total Power Dissipation (Note 5)	$T_A = +25$ °C	PD	0.82	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	Rөja	153	°C/W
Total Power Dissipation (Note 6)	$T_A = +25^{\circ}C$	P <sub>D</sub>	1.14	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	Rөja	110	°C/W
Operating and Storage Temperature Range		TJ, TSTG	-55 to +150	°C

### Electrical Characteristics (@ TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)					•	
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-20	_	_	V	$V_{GS} = 0V, I_{D} = -250\mu A$
Zero Gate Voltage Drain Current T <sub>J</sub> = +25°C	IDSS	_	_	-1.0	μΑ	V <sub>DS</sub> = -16V, V <sub>GS</sub> = 0V
Gate-Source Leakage	lgss	_	_	±100	nA	V <sub>G</sub> S = ±8V, V <sub>D</sub> S = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	Vgs(TH)	-0.45	_	-1.0	V	$V_{DS} = V_{GS}$ , $I_D = -250\mu A$
		_	_	75		Vgs = -4.5V, ID = -2.8A
Static Drain-Source On-Resistance	RDS(ON)	_	_	110	mΩ	Vgs = -2.5V, ID = -2.0A
		_	_	168		V <sub>G</sub> S = -1.8V, I <sub>D</sub> = -1.0A
Diode Forward Voltage	V <sub>SD</sub>	_	_	-1.0	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = -1.0A
DYNAMIC CHARACTERISTICS (Note 8)					•	
Input Capacitance	C <sub>iss</sub>	_	443	_	pF	
Output Capacitance	Coss	_	59	_	pF	V <sub>DS</sub> = -10V, V <sub>GS</sub> = 0V, f = 1.0MHz
Reverse Transfer Capacitance	Crss	_	47	_	pF	1 - 1.0001112
Gate Resistance	Rg	_	8.5	_	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1MHz
Total Gate Charge (V <sub>GS</sub> = -4.5V)	0	_	6.0	_	nC	
Total Gate Charge (VGS = -8V)	$Q_g$	_	12.7	_	nC	157 1 000
Gate-Source Charge	Qgs	_	0.6	_	nC	$V_{DS} = -4.5V, I_{D} = -3.0A$
Gate-Drain Charge	Qgd	_	1.8	_	nC	]
Turn-On Delay Time	td(ON)	_	4.0	_	ns	
Turn-On Rise Time	t <sub>R</sub>	_	3.7	_	ns	V <sub>DS</sub> = -10V, V <sub>GS</sub> = -4.5V,
Turn-Off Delay Time	tD(OFF)	_	24.5	_	ns	$R_L = 10\Omega$ , $R_g = 6\Omega$
Turn-Off Fall Time	tF	_	9.5		ns	]
Body Diode Reverse Recovery Time	trr	_	8.3	_	ns	Is = -1.0A, dI/dt = 100A/µs
Body Diode Reverse Recovery Charge	Q <sub>RR</sub>	_	2.0	_	nC	I <sub>S</sub> = -1.0A, dI/dt = 100A/µs

 Device mounted on FR-4 substrate PCB, 2oz copper, with minimum recommended pad layout.
Device mounted on FR-4 substrate PCB, 2oz copper, with 1inch square copper plate.
Short duration pulse test used to minimize self-heating effect.
Guaranteed by design. Not subject to product testing. Notes:





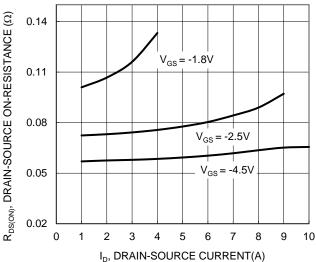


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

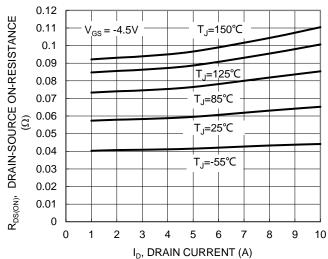


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

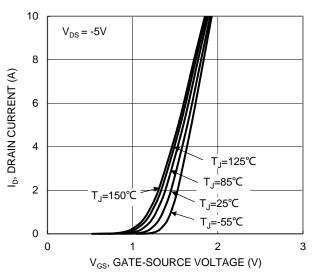


Figure 2. Typical Transfer Characteristic

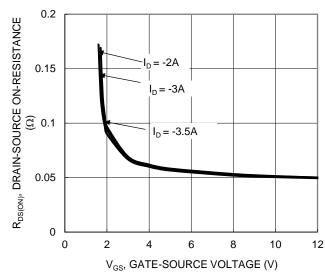


Figure 4. Typical Transfer Characteristic

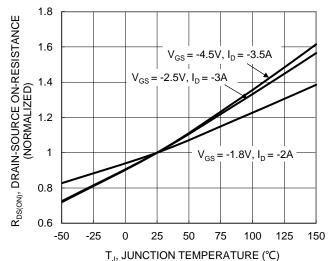


Figure 6. On-Resistance Variation with Junction Temperature



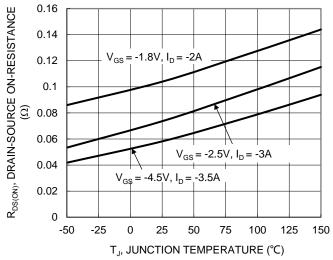


Figure 7. On-Resistance Variation with Junction Temperature

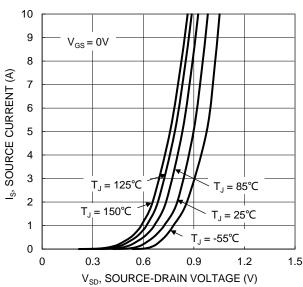
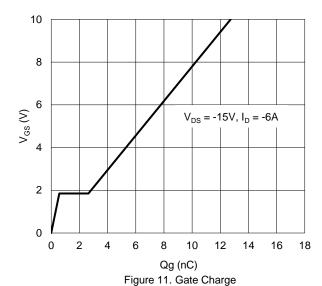
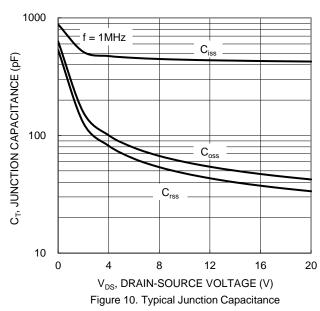


Figure 9. Diode Forward Voltage vs. Current



1.5  $V_{GS(TH)}, \, GATE \, THRESHOLD \, VOLTAGE \, (V)$ 1  $I_D = -1mA$  $I_{D} = -250 \mu A$ 0.5 0 125 150 -50 -25 25 50 75 100  $T_J$ , JUNCTION TEMPERATURE (°C)

Figure 8. Gate Threshold Variation vs. Junction Temperature



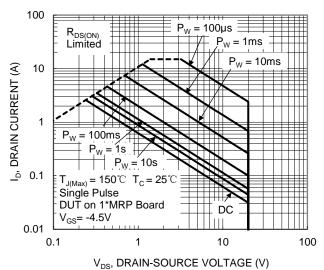


Figure 12. SOA, Safe Operation Area



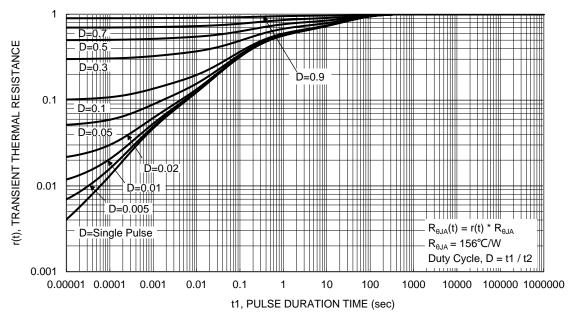
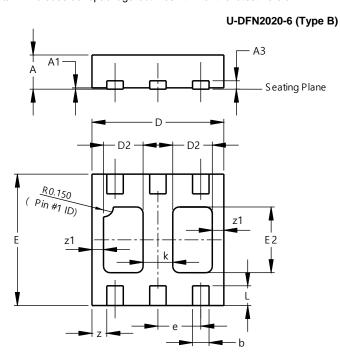


Figure 13. Transient Thermal Resistance



# **Package Outline Dimensions**

Please see http://www.diodes.com/package-outlines.html for the latest version.

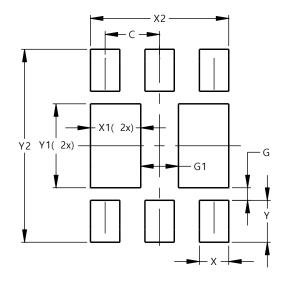


U-DFN2020-6 Type B						
Dim	Min	Min Max Ty				
Α	0.545	0.605	0.575			
A1	0.00	0.05	0.02			
A3	-	-	0.13			
b	0.20	0.30	0.25			
D	1.95	2.075	2.00			
D2	0.50	0.70	0.60			
e	-	-	0.65			
Е	1.95	2.075	2.00			
E2	0.90	1.10	1.00			
k	-	-	0.45			
L	0.25	0.35	0.30			
Z	-	-	0.225			
<b>z1</b> 0.1						
All	Dimens	ions in	mm			

# **Suggested Pad Layout**

Please see http://www.diodes.com/package-outlines.html for the latest version.

### U-DFN2020-6 (Type B)



Dimensions	Value
Dillielisions	(in mm)
С	0.650
G	0.150
G1	0.450
Х	0.350
X1	0.600
X2	1.650
Y	0.500
Y1	1.000
Y2	2 300

March 2023



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