



DUAL P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV _{DSS}	R _{D1D2 max}	I _D T _A = +25°C
001/	90mΩ @ V _{GS} = -4.5V	-3.2A
-20V	120mΩ @ V _{GS} = -2.5V	-2.7A

Features

- PCB Footprint of 4mm²
- Low On-Resistance
- Low Input Capacitance
- Low Profile, 0.6mm Maximum Height
- ESD Protected Gate
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/

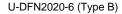
Description and Applications

This MOSFET is designed to minimize the on-state resistance (RDS(ON)) yet maintain superior switching performance, which makes it ideal for high-efficiency power management applications.

- Load Switch
- Power Management Functions
- Portable Power Adaptors

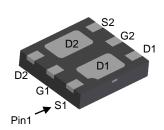
Mechanical Data

- Case: U-DFN2020-6
- Case Material: Molded Plastic, "Green" Molding Compound.
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 64
- Terminals Connections: See Diagram Below
- Weight: 0.0065 grams (Approximate)

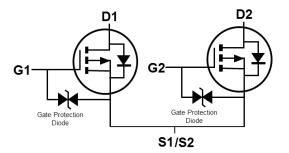




LOD proteoted oute



Bottom View



Internal Schematic

Ordering Information (Note 4)

Part Number	Case	Packaging
DMP2090UFDB-7	U-DFN2020-6 (Type B)	3000/Tape & Reel
DMP2090UFDB-13	U-DFN2020-6 (Type B)	10,000/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.



Marking Information

Site 1:



E4 = Product Type Marking Code YM = Date Code Marking Y = Year (ex: G = 2019) M = Month (ex: 9 = September)

Date Code Key

Year	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
Code	G	Н		J	K	L	М	N	0	Р	R	S
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec

Site 2:



E4 = Product Type Marking Code YWX = Date Code Marking Y = Year (ex: 9 = 2019) W = Week (ex: a = week 27; z represents week 52 and 53) X = Internal Code (ex: U = Monday)

Date Code Kev

Year	2019	2020	2021	2022	2023	2024	2025	2026	2027
Code	9	0	1	2	3	4	5	6	7
Week	1-26			27-52			53		
Code		A-Z	A-Z		a-z		Z		
Internal Code	Sun	Mon	1	Tue	Wed	Thu		Fri	Sat
Code	T	U		V	W	Х		Υ	Z



Maximum Ratings (@ $T_A = +25^{\circ}C$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit		
Drain-Source Voltage	V _{DSS}	-20	V		
Gate-Source Voltage	Vgss	±8	V		
Continuous Drain Current (Note 6) V _{GS} = -4.5V	lo	-3.2 -2.5	А		
Maximum Continuous Body Diode Forward Current (No	te 6)		Is	-1.9	Α
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)	Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)				
Avalanche Current (Note 7) L = 0.1mH	I _{AS}	-11	Α		
Avalanche Energy (Note 7) L = 0.1mH			Eas	7	mJ

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	T _A = +25°C	PD	0.79	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	Reja	159	°C/W
Total Power Dissipation (Note 6)	$T_A = +25$ °C	P _D	1.39	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	Rөja	90	°C/W
Operating and Storage Temperature Range		TJ, TSTG	-55 to +150	°C

Electrical Characteristics (@ T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 8)	·			I.			
Drain-Source Breakdown Voltage	BV _{DSS}	-20	_	_	V	V _G S = 0V, I _D = -250μA	
Zero Gate Voltage Drain Current TJ = +25°C	IDSS	_	_	-1.0	μΑ	V _{DS} = -20V, V _{GS} = 0V	
Gate-Source Leakage	Igss	_	_	±10	μΑ	V _G S = ±8V, V _D S = 0V	
ON CHARACTERISTICS (Note 8)							
Gate Threshold Voltage	VGS(TH)	-0.3	_	-1.0	V	$V_{DS} = V_{GS}$, $I_D = -250\mu A$	
Static Drain1-Drain2 On-Resistance	D	_	37	90		Vgs = -4.5V, ID = -4A	
Static Drain 1-Drain2 On-Resistance	R _{D1D2}	_	50	120	mΩ	V _G S = -2.5V, I _D = -3.5A	
Diode Forward Voltage	VsD	_	-0.7	-1.2	V	V _G S = 0V, I _S = -1.0A	
DYNAMIC CHARACTERISTICS (Note 9)			•	•			
Input Capacitance	Ciss	_	634	_	pF		
Output Capacitance	Coss	_	81	_	pF	$V_{DS} = -10V, V_{GS} = 0V,$ - f = 1.0MHz	
Reverse Transfer Capacitance	Crss	_	66	_	pF	1 = 1.001112	
Gate Resistance	Rg	_	20	_	Ω	$V_{DS} = 0V$, $V_{GS} = 0V$, $f = 1MHz$	
Total Gate Charge (VGS = -4.5V)	Qg	_	6.8	_	nC		
Gate-Source Charge	Qgs	_	0.7	_	nC	V _{DS} = -4.5V, I _D = -4A, - V _{DS} = -10V	
Gate-Drain Charge	Qgd	_	1.6	_	nC	VDS = -10V	
Turn-On Delay Time	t _{D(ON)}	_	4.2	_	ns		
Turn-On Rise Time	t _R	_	3.4	_	ns	V _{DS} = -10V, V _{GS} = -4.5V,	
Turn-Off Delay Time	tD(OFF)	_	23	_	ns	$R_L = 3.3\Omega$, $R_g = 1\Omega$	
Turn-Off Fall Time	t⊧	_	9.6	_	ns		
Body Diode Reverse Recovery Time	t _{RR}	_	1.8	_	ns	$I_S = -1.0A$, $dI/dt = 100A/\mu s$	
Body Diode Reverse Recovery Charge	Q _{RR}	_	9.4	_	nC	I _S = -1.0A, dI/dt = 100A/μs	

5. Device mounted on FR-4 substrate PCB, 2oz copper, with minimum recommended pad layout. 6. Device mounted on FR-4 substrate PCB, 2oz copper, with 1inch square copper plate. 7. I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep T_J = +25°C. Notes:

- Short duration pulse test used to minimize self-heating effect.
 Guaranteed by design. Not subject to product testing.



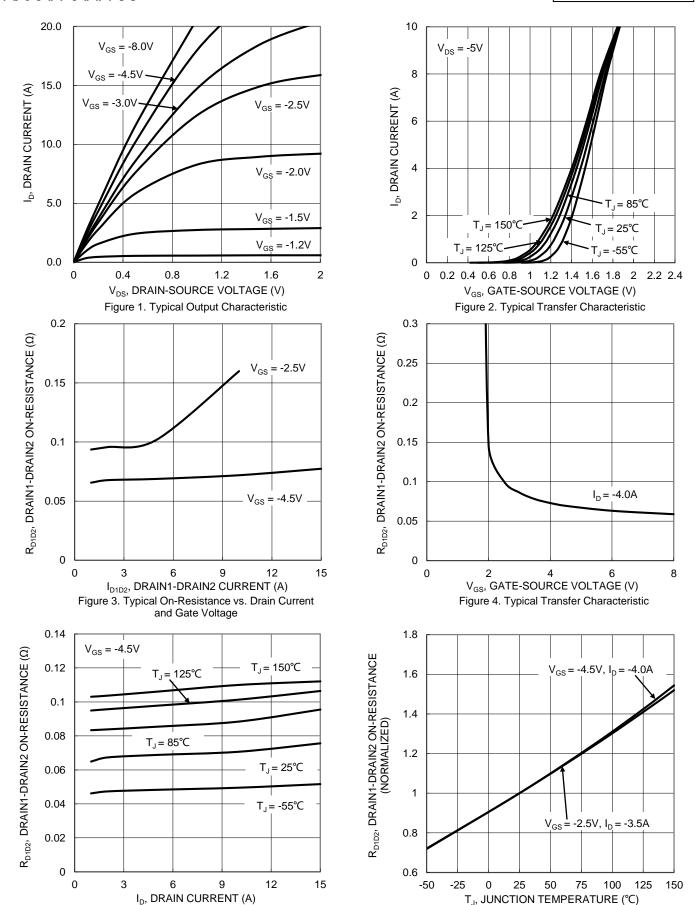


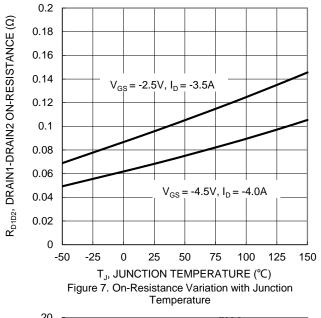
Figure 5. Typical On-Resistance vs. Drain Current and

Junction Temperature

Figure 6. On-Resistance Variation with Junction

Temperature





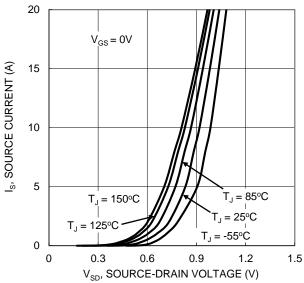


Figure 9. Diode Forward Voltage vs. Current

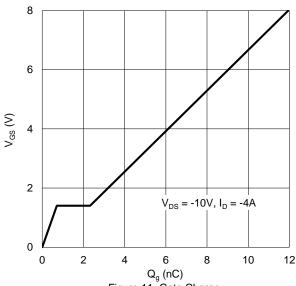


Figure 11. Gate Charge

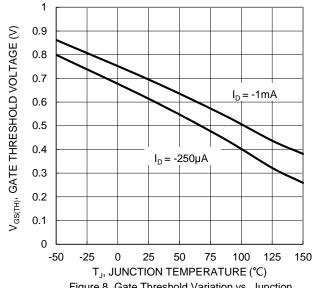
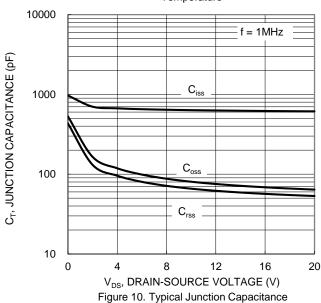
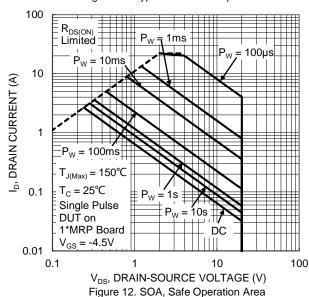


Figure 8. Gate Threshold Variation vs. Junction Temperature







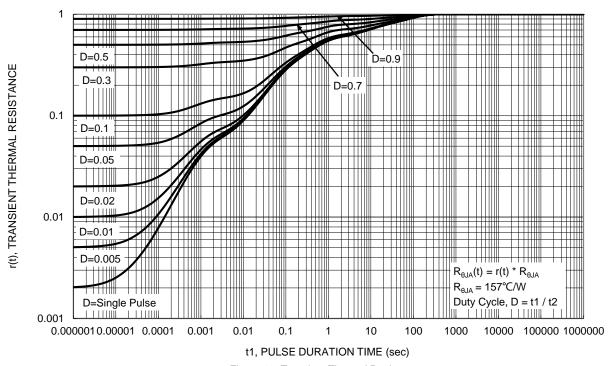


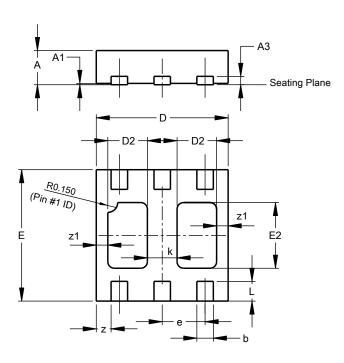
Figure 13. Transient Thermal Resistance



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2020-6 (Type B)

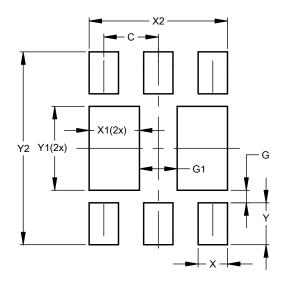


U-DFN2020-6 Type B						
Dim	Min	Max	Тур			
Α	0.545	0.605	0.575			
A1	0.00	0.05	0.02			
A3	-	-	0.13			
b	0.20	0.30	0.25			
D	1.95	2.075	2.00			
D2	0.50	0.70	0.60			
е	-	-	0.65			
E	1.95	2.075	2.00			
E2	0.90	1.10	1.00			
k	-	-	0.45			
L	0.25	0.35	0.30			
Z	-	-	0.225			
z1	-	-	0.175			
All	Dimens	ions in	mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2020-6 (Type B)



Dimensions	Value
Dillielisions	(in mm)
С	0.650
G	0.150
G1	0.450
Х	0.350
X1	0.600
X2	1.650
Y	0.500
Y1	1.000
Y2	2.300



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