



#### P-CHANNEL ENHANCEMENT MODE MOSFET

### **Product Summary**

BV <sub>DSS</sub>	R <sub>DS(ON)</sub> Typ.	I <sub>D</sub> T <sub>A</sub> = +25°C
001/	37mΩ @ V <sub>GS</sub> = -4.5V	-3.4A
-20V	49mΩ @ V <sub>GS</sub> = -2.5V	-2.9A

### **Description and Applications**

This new generation MOSFET has been designed to minimize the onstate resistance (R<sub>DS(ON)</sub>) yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Battery managements
- Load switches
- Battery protections

## **Features and Benefits**

- Low Q<sub>q</sub> & Q<sub>qd</sub>
- Small Footprint
- Low Profile 0.45mm Height
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.

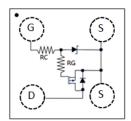
https://www.diodes.com/quality/product-definitions/

#### **Mechanical Data**

- Package: X1-DSN1010-4
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal: Finish SnAg over Cu Pillar
  Solder Cap Material: SnAg (Ag: 2.0+/-0.5%) (a)
- Terminal Connections: See Diagram Below
- UBM Size:320μm
- Weight: 0.0012 grams (Approximate)

#### X1-DSN1010-4 (Type C)





Top View Equivalent Circuit

## **Ordering Information (Note 4)**

Part Number	Backago	Packing			
Part Number	Part Number Package		Carrier		
DMP2042UCP4-7	X1-DSN1010-4 (Type C)	3000	Tape & Reel		

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

## **Marking Information**



2M= Product Type Marking Code YW = Date Code Marking Y or  $\overline{Y}$  = Year (ex: 2 = 2022) W or  $\overline{W}$  = Week (ex: a = week 27; z represents week 52 and 53)

### Date Code Key

Year	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033
Code	2	3	4	5	6	7	8	9	0	1	2	3
Week		1.	-26		27-52				53			
Code		А	ı-Z		a-z				Z			



# **Maximum Ratings** (@ $T_A = +25$ °C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	VDSS	-20	V
Gate-Source Voltage	V <sub>GSS</sub>	-6	V
Continuous Drain Current (Note 6) V <sub>GS</sub> = -4.5V	lD	-3.4	Α
Continuous Drain Current (Note 6) V <sub>GS</sub> = -2.5V	I <sub>D</sub>	-2.9	Α
Pulsed Drain Current (Note 5)	I <sub>DM</sub>	-16	Α

## **Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 6)	PD	0.86	W
Thermal Resistance, Junction to Ambient @T <sub>A</sub> = +25°C (Note 6)	R <sub>0JA</sub>	145.7	°C/W
Operating and Storage Temperature Range	TJ, TSTG	-55 to +150	°C

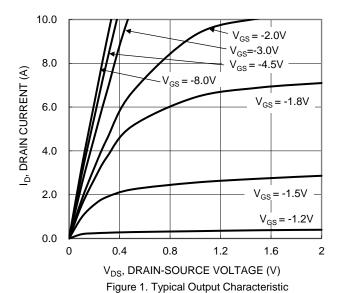
# **Electrical Characteristics** (@TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage	BVDSS	-20	_	_	V	$V_{GS} = 0V, I_{D} = -250\mu A$	
Zero Gate Voltage Drain Current T <sub>J</sub> = +25°C	I <sub>DSS</sub>	_	_	-1	μΑ	$V_{DS} = -16V, V_{GS} = 0V$	
Gate-Source Leakage	Igss	_	1	-100	nA	$V_{GS} = -6V$ , $V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage	Vgs(th)	-0.4	-0.8	-1.2	V	$V_{DS} = V_{GS}$ , $I_D = -250\mu A$	
Static Drain-Source On-Resistance	D- avanu	_	37	48	mΩ	V <sub>G</sub> S = -4.5V, I <sub>D</sub> =-1A	
Static Drain-Source Off-Resistance	R <sub>DS(ON)</sub>	_	49	65	1112.2	$V_{GS} = -2.5V, I_D = -1A$	
Diode Forward Voltage	VsD	_	-0.7	-1.0	V	Vgs = 0V, Is = -1A	
DYNAMIC CHARACTERISTICS (Note 8)							
Input Capacitance	Ciss		218	_		V <sub>DS</sub> = -10V, V <sub>GS</sub> = 0V, f = 1.0MHz	
Output Capacitance	Coss		148	_	pF		
Reverse Transfer Capacitance	C <sub>rss</sub>	_	11	_			
Series Gate Resistance	Rg	_	20	_	Ω	$f = 1MHz, V_{GS} = 0V, V_{DS} = 0V$	
Series Clamp Resistance	Rc		5000	_	12		
Total Gate Charge	Qg	_	2.5	_			
Gate-Source Charge	Qgs		0.4	_	nC	V <sub>G</sub> S = -4.5V, V <sub>D</sub> S = -10V, I <sub>D</sub> =-1A	
Gate-Drain Charge	Qgd	_	0.4	_	IIC		
Gate Charge at VTH	Q <sub>g(TH)</sub>		0.2	_			
Turn-On Delay Time	t <sub>D(ON)</sub>		0.6	_	_		
Turn-On Rise Time	t <sub>R</sub>	_	0.8	_		$V_{DS} = -10V$ , $V_{GS} = -2.5V$ ,	
Turn-Off Delay Time	tD(OFF)		1.4	_	μS	$R_g = 10\Omega$ , $I_D = -1A$	
Turn-Off Fall Time	tF	_	0.8	_			

Notes:

- Repetitive rating, pulse width limited by junction temperature.
  Device mounted on FR-4 PCB with minimum recommended pad layout, single sided.
  Short duration pulse test used to minimize self-heating effect.
  Guaranteed by design. Not subject to production testing.





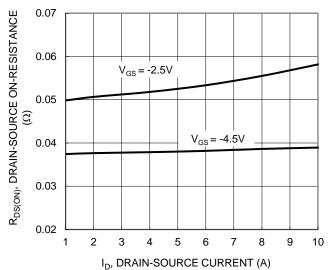


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

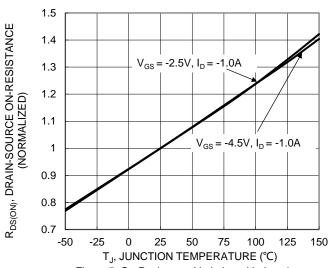


Figure 5. On-Resistance Variation with Junction Temperature

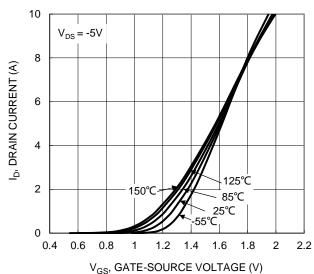


Figure 2. Typical Transfer Characteristic

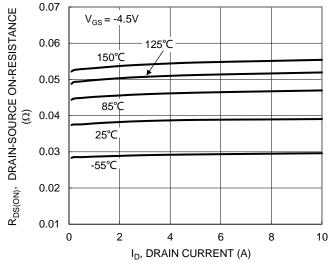


Figure 4. Typical On-Resistance vs. Drain Current and Junction Temperature

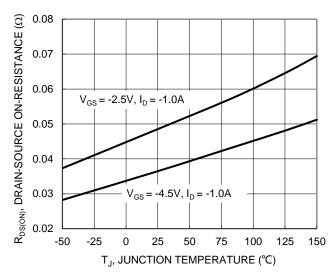


Figure 6. On-Resistance Variation with Junction Temperature





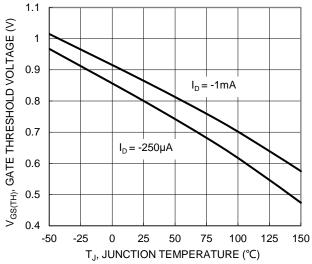
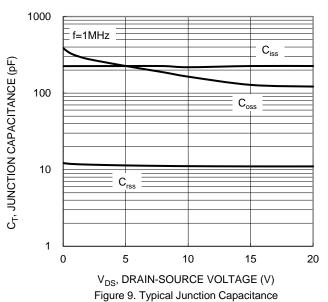


Figure 7. Gate Threshold Variation vs. Junction Temperature



 $R_{DS(ON)}$  Limited =100µs 10 ID, DRAIN CURRENT (A) P<sub>w</sub> =10ms P<sub>W</sub> =100ms T<sub>J(Max)</sub> = 150 °C 0.1 Single Pulse DUT on 1\*MRP Board DC  $V_{GS} = -4.5V$ 0.01 0.1 10 100 V<sub>DS</sub>, DRAIN-SOURCE VOLTAGE (V)

Figure 11. SOA, Safe Operation Area

5  $V_{GS} = 0V$ 4 Is, SOURCE CURRENT (A) 3 2  $T_J = 85^{\circ}C$ T<sub>J</sub> = 125°C  $T_{.1} = 25^{\circ}C$  $T_J = 150$ °C -55°C 0 0 0.3 0.6 0.9 1.2  $V_{SD}$ , SOURCE-DRAIN VOLTAGE (V)

Figure 8. Diode Forward Voltage vs. Current

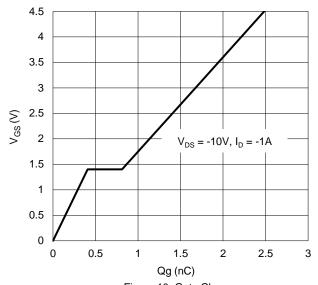


Figure 10. Gate Charge

100



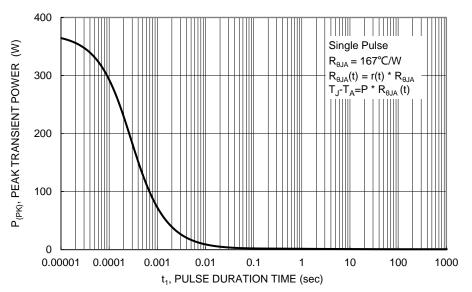


Figure 12. Single Pulse Maximum Power Dissipation

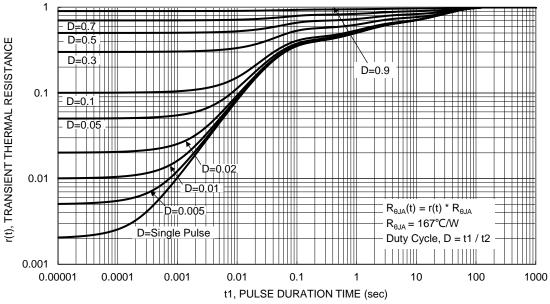


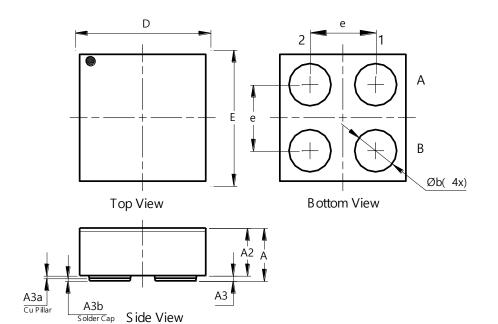
Figure 13. Transient Thermal Resistance



## **Package Outline Dimensions**

Please see http://www.diodes.com/package-outlines.html for the latest version.

### X1-DSN1010-4 (Type C)

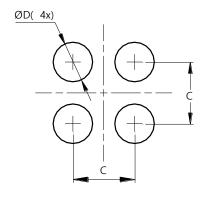


X1-DSN1010-4 (Type C)							
Dim	Min	Max	Тур				
Α		0.45	0.40				
A2		1	0.36				
A3	0.034	0.046	0.040				
A3a	0.015	0.025	0.020				
A3b	0.017	0.023	0.020				
b	0.27	0.37	0.32				
D	0.92	1.00	0.96				
Е	0.92	1.00	0.96				
е			0.50				
All Dimensions in mm							

# **Suggested Pad Layout**

Please see http://www.diodes.com/package-outlines.html for the latest version.

### X1-DSN1010-4 (Type C)



Dimensions	Value (in mm)
С	0.50
D	0.25



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