



Product Summary

BV _{DSS}	Rds(ON) Max	I _D T _A = +25°C
	2Ω @ V _{GS} = 5V	480mA
50V	2.5Ω @ V _{GS} = 2.5V	440mA
	4Ω @ V _{GS} = 1.8V	370mA

Description and Applications

This MOSFET is designed to meet the stringent requirements of automotive applications. It is qualified to AEC-Q101, supported by a PPAP and is ideal for use in:

- Battery-management systems
- Power-management functions
- Load switches

50V N-CHANNEL ENHANCEMENT MODE MOSFET

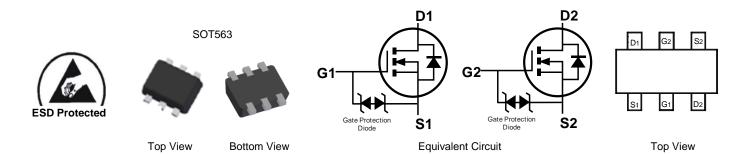
Features and Benefits

- Dual N-Channel MOSFET
- Low On-Resistance
- Very Low Gate Threshold Voltage, 1.0V Max
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface-Mount Package
- ESD Protected
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- The DMN52D0UVQ is suitable for automotive applications requiring specific change control; this part is AEC-Q101 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.

https://www.diodes.com/quality/product-definitions/

Mechanical Data

- Package: SOT563
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 (e3)
- Weight: 0.006 grams (Approximate)



Ordering Information (Note 4)

Part Number	Backaga	Packing		
	Package	Qty.	Carrier	
DMN52D0UVQ-7	SOT563	3,000	Reel	
DMN52D0UVQ-13	SOT563	10,000	Reel	

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.

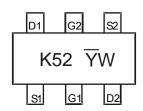
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.

3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.



Marking Information



 $\begin{array}{l} \underline{K52} = \mbox{Product Type Marking Code} \\ \overline{YW} = \mbox{Date Code Marking} \\ \overline{Y} = \mbox{Year (ex: 3 = 2023)} \\ W = \mbox{Week (ex: a = week 27; z represents week 52 and 53)} \end{array}$

Date Code Key

Year	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033
Code	2	3	4	5	6	7	8	9	0	1	2	3
Week	Week 1-26					27-	-52		53			
Code	A-Z				a	-Z			2	2		

Maximum Ratings (@TA = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit	
Drain-Source Voltage		Vdss	50	V	
Gate-Source Voltage	V _{GSS}	±12	V		
Continuous Drain Current (Note 5) $V_{GS} = 5V$	Steady $T_A = +25^{\circ}C$ State $T_A = +70^{\circ}C$		ID	480 380	mA
Maximum Continuous Body Diode Forward Curr	ent (Note 5)		ls	480	mA
Pulsed Drain Current (10µs Pulse, Duty Cycle =	1%)	I _{DM}	1.2	A	
Pulsed Source Current (10µs Pulse, Duty Cycle	= 1%)	I _{SM}	1.2	А	

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 6)		PD	0.48	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	Reja	261	°C/W
Total Power Dissipation (Note 5)		PD	0.89	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	Reja	139	°C/W
Operating and Storage Temperature Range		TJ, TSTG	-55 to +150	°C

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.

6. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.



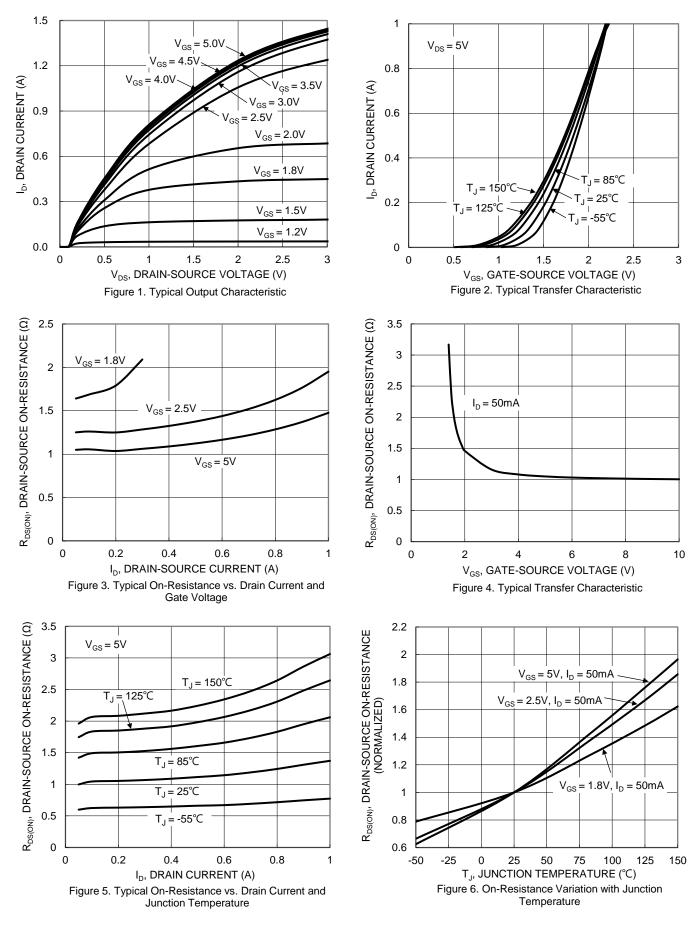
Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)	. ,		- 71-			
Drain-Source Breakdown Voltage	BVDSS	50			V	Vgs = 0V, ID = 250µA
Zero Gate Voltage Drain Current	IDSS	_	_	1	μA	V _{DS} = 50V, V _{GS} = 0V
Gate-Source Leakage	lgss			±10	μA	$V_{GS} = \pm 12V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	VGS(TH)	0.49	_	1.0	V	$V_{DS} = V_{GS}, I_D = 250 \mu A$
		_	1.6	4.0		$V_{GS} = 1.8V, I_D = 50mA$
Static Drain-Source On-Resistance	R _{DS(ON)}	—	1.2	2.5	Ω	$V_{GS} = 2.5V, I_D = 50mA$
		_	1.0	2.0		$V_{GS} = 5.0V, I_{D} = 50mA$
Diode Forward Voltage	Vsd	_	0.6	1.2	V	$V_{GS} = 0V, I_D = 50mA$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	Ciss	—	39	_	pF	
Output Capacitance	Coss	—	4.8	—	pF	VDS = 25V, VGS = 0V f = 1.0MHz
Reverse Transfer Capacitance	Crss	_	3.6	_	pF	1 - 1.00012
Gate Resistance	Rg	—	47.8	_	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1MHz$
Total Gate Charge (V _{GS} = 4.5V)	Qg	_	0.8	_	nC	
Total Gate Charge (V _{GS} = 10V)	Qg	_	1.5	_	nC	
Gate-Source Charge	Q _{gs}	—	0.1	—	nC	$V_{DS} = 25V, I_D = 50mA$
Gate-Drain Charge	Q _{gd}	—	0.1	—	nC	
Turn-On Delay Time	tD(ON)	_	1.05	_	ns	
Turn-On Rise Time	tR		11.3		ns	V _{DS} = 25V, V _{GS} = 10V
Turn-Off Delay Time	t _{D(OFF)}	_	33	_	ns	$R_g = 50\Omega, I_D = 50mA$
Turn-Off Fall Time	tF	_	38.5	_	ns	

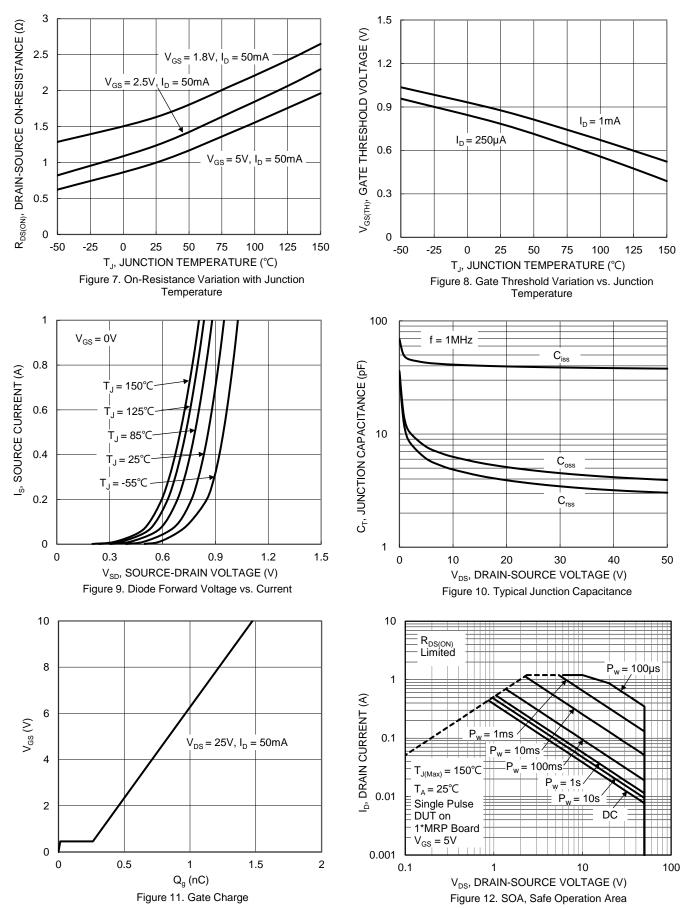
 Short duration pulse test used to minimize self-heating effect.
Guaranteed by design. Not subject to product testing. Notes:



DMN52D0UVQ

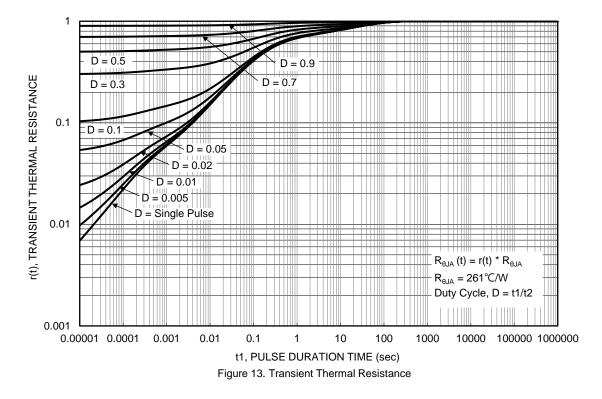






DMN52D0UVQ Document number: DS44986 Rev. 3 - 2

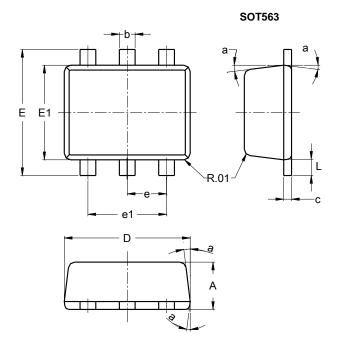






Package Outline Dimensions

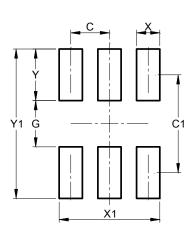
Please see http://www.diodes.com/package-outlines.html for the latest version.



	SOT563							
Dim	Min	Max	Тур					
Α	0.55	0.60						
b	0.15	0.30	0.20					
C	0.10	0.18	0.11					
D	1.50	1.70	1.60					
Е	1.55	1.70	1.60					
E1	1.10	1.25	1.20					
е			0.50					
e1	0.90	1.10	1.00					
L	0.10	0.30	0.20					
а	8°	9°	7°					
All Dimensions in mm								

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.



SOT563

Dimensions	Value (in mm)
С	0.500
C1	1.270
G	0.600
Х	0.300
X1	1.300
Y	0.670
Y1	1.940



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