



20V N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV _{DSS}	Rds(on) Max	I _D Max T _A = +25°C
	$22m\Omega$ @ $V_{GS} = 4.5V$	7.1A
201/	$26m\Omega$ @ $V_{GS} = 2.5V$	6.5A
20V	36mΩ @ V _{GS} = 1.8V	5.5A
	50mΩ @ V _{GS} = 1.5V	4.7A

Description

This MOSFET is designed to minimize the on-state resistance (RDS(ON)) yet maintain superior switching performance, which makes it ideal for high-efficiency power management applications.

Applications

- Battery Management Application
- Power Management Functions
- DC-DC Converters

Features

- 0.6mm Profile—Ideal for Low Profile Applications
- PCB Footprint of 4mm²
- Low Gate Threshold Voltage
- Fast Switching Speed
- ESD Protected Gate
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please <u>contact us</u> or your local Diodes representative. https://www.diodes.com/quality/product-definitions/

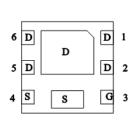
Mechanical Data

- Case: U-DFN2020-6
- Case Material: Molded Plastic, "Green" Molding Compound.
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish—NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 @4
- Weight: 0.0065 grams (Approximate)

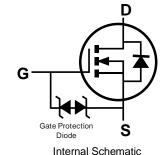


Top View

Bottom View



Pin Out Bottom View



Ordering Information (Note 4)

Part Number	Reel Size (inches)	Quantity Per Reel
DMN2024UFDF-7	7	3,000
DMN2024UFDF-13	13	10,000

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/



Marking Information

Site1



OA = Product Type Marking Code YM = Date Code Marking Y = Year (ex: H = 2020) M = Month (ex: 9 = September)

Date Code Key

Year	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029
Code	F	G	Н	ı	J	K	L	М	N	0	Р	R
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec

Site 2



OA = Product Type Marking Code YWX = Date Code Marking Y = Year (ex: 0 = 2020) W = Week (ex: a = Week 27; z Represents Week 52 and 53) X = Internal Code (ex: U = Monday)

Date Code Key

Year	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029
Code	8	9	0	1	2	3	4	5	6	7	8	9

Week	1-26	27-52	53
Code	A-Z	a-z	z

Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat
Code	Т	U	V	W	X	Y	Z



Maximum Ratings (@ $T_A = +25^{\circ}C$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit		
Drain-Source Voltage			VDSS	20	V
Gate-Source Voltage			V_{GSS}	±10	V
Continuous Drain Current (Note 6) V _{GS} = 4.5V	l _D	7.1 5.6	А		
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)		I _{DM}	40	Α
Continuous Source-Drain Diode Current	inuous Source-Drain Diode Current		Is	2.6	Α
Avalanche Current (Note 7) L = 0.1mH	valanche Current (Note 7) L = 0.1mH		las	12	Α
Avalanche Energy (Note 7) L = 0.1mH			Eas	8	mJ

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	T _A = +25°C	PD	0.96	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	Rөja	130	°C/W
Total Power Dissipation (Note 6)	T _A = +25°C	PD	1.67	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	Rөja	75	°C // /
Thermal Resistance, Junction to Case (Note 6)		Rejc	16	°C/W
Operating and Storage Temperature Range		TJ, TSTG	-55 to +150	°C

Electrical Characteristics (@TA = +25°C, unless otherwise specified.)

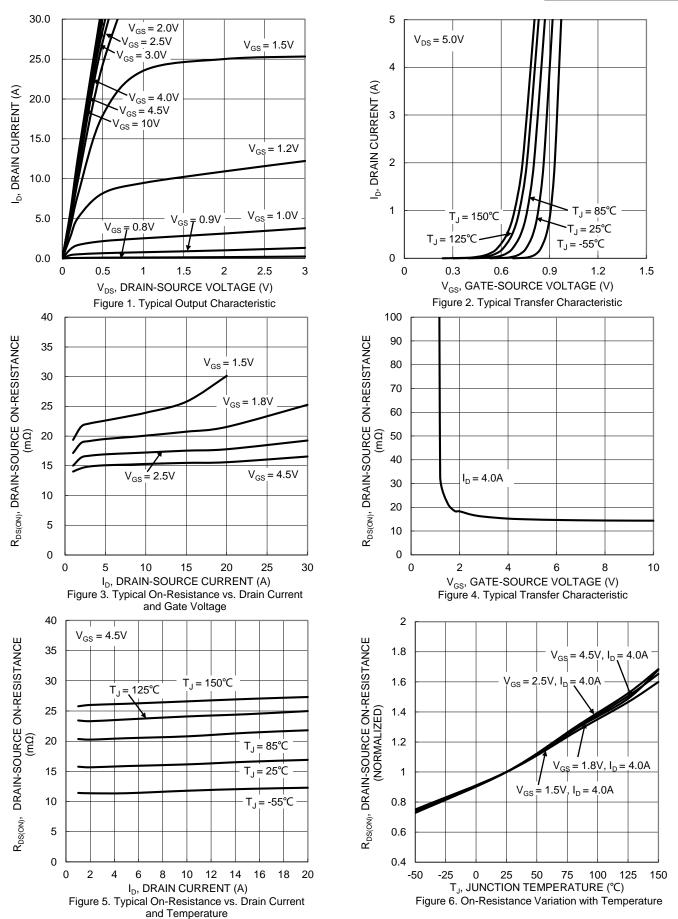
Observation leader	0	NA!	T		1124	Tarat Oran didiran
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)	D) /	-00		1		N/ 050 A
Drain-Source Breakdown Voltage	BV _{DSS}	20		_	V	$V_{GS} = 0V, I_{D} = 250\mu A$
Zero Gate Voltage Drain Current T _J = +25°C	IDSS	_	_	1	μΑ	$V_{DS} = 20V, V_{GS} = 0V$
Gate-Source Leakage	I _{GSS}	_	_	±10	μA	$V_{GS} = \pm 8V$, $V_{DS} = 0V$
ON CHARACTERISTICS (Note 8)	1	1		ı		
Gate Threshold Voltage	V _{GS(TH)}	0.5	_	1.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
			15	22		$V_{GS} = 4.5V, I_{D} = 4A$
Static Drain-Source On-Resistance	D- even		17	26	mΩ	$V_{GS} = 2.5V, I_{D} = 4A$
Static Dialit-Source Off-Nesistance	R _{DS(ON)}	_	20	36	11122	$V_{GS} = 1.8V$, $I_D = 4A$
			23	50		$V_{GS} = 1.5V, I_{D} = 4A$
Diode Forward Voltage	VsD	_	0.7	1.0	V	$V_{GS} = 0V$, $I_{S} = 5A$
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	Ciss	_	647	_		
Output Capacitance	Coss	_	78	_	pF	$V_{DS} = 10V, V_{GS} = 0V,$ f = 1.0MHz
Reverse Transfer Capacitance	Crss	_	38	_		1 – 1.01/11/12
Gate Resistance	Rg	_	400		Ω	$V_{DS} = 0V$, $V_{GS} = 0V$, $f = 1MHz$
Total Gate Charge (V _{GS} = 4.5V)	Qg	_	6.5	_		
Total Gate Charge (V _{GS} = 10V)	Qg	_	14.8	_	nC	\/ 40\/ I= 0.5A
Gate-Source Charge	Qgs	_	1.1	_	nc	$V_{DS} = 10V, I_{D} = 6.5A$
Gate-Drain Charge	Q _{gd}	_	1.7	_		
Turn-On Delay Time	t _D (ON)	_	98	_		
Turn-On Rise Time	t _R	_	140		20	$V_{DS} = 10V, V_{GS} = 4.5V,$
Turn-Off Delay Time	t _{D(OFF)}	_	1024	_	ns	$R_G=6\Omega,~R_L=10\Omega,~I_D=1A$
Turn-Off Fall Time	t _F	_	434	_		
Reverse Recovery Time	trr	_	245	_	ns	IF = 1A, di/dt = 100A/µs
Reverse Recovery Charge	Qrr	_	149	_	nC	IF = 1A, di/dt = 100A/µs

5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

^{7.} I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep T_J = +25°C.

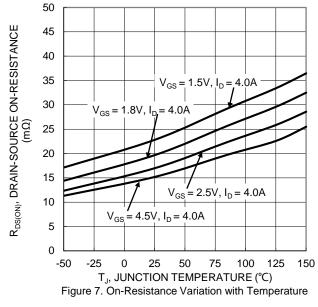
Short duration pulse test used to minimize self-heating effect.
 Guaranteed by design. Not subject to product testing.

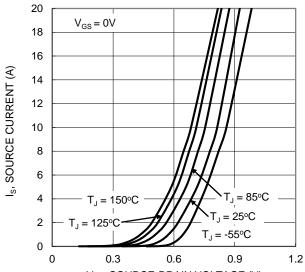












V_{SD}, SOURCE-DRAIN VOLTAGE (V) Figure 9. Diode Forward Voltage vs. Current

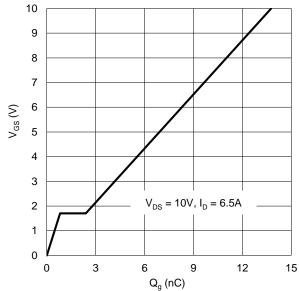


Figure 11. Gate Charge

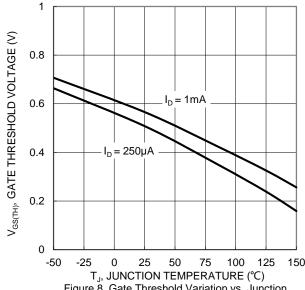


Figure 8. Gate Threshold Variation vs. Junction Temperature

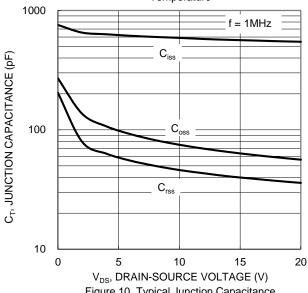


Figure 10. Typical Junction Capacitance

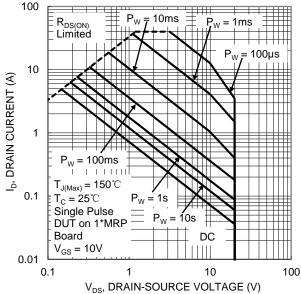


Figure 12. SOA, Safe Operation Area



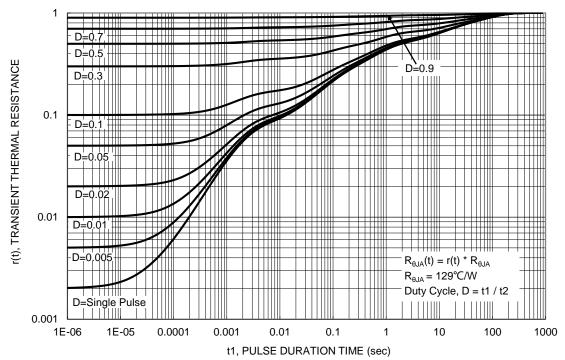


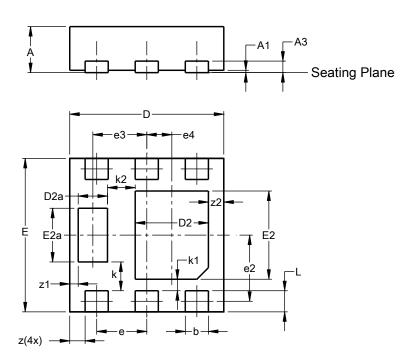
Figure 13. Transient Thermal Resistance



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2020-6 (Type F)

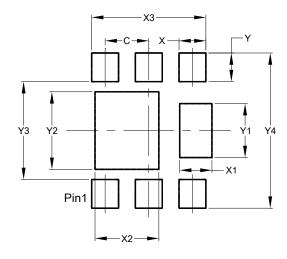


	U-DFN2020-6						
	(Type F)						
Dim	Min	Max	Тур				
Α	0.57	0.63	0.60				
A1	0.00	0.05	0.03				
A3	-	-	0.15				
b	0.25	0.35	0.30				
D	1.95	2.05	2.00				
D2	0.85	1.05	0.95				
D2a	0.33	0.43	0.38				
Е	1.95	2.05	2.00				
E2	1.05	1.25	1.15				
E2a	0.65	0.75	0.70				
е		0.65 BS	С				
e2	().863 BS	SC				
е3		0.70 BS	С				
e4	().325 BS	SC				
k		0.37 BS	С				
k1		0.15 BS	С				
k2		0.36 BS	С				
L	0.225 0.325 0.275						
Z	0.20 BSC						
z 1	0.110 BSC						
z2		0.20 BS	С				
All C	Dimens	ions in	mm				

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2020-6 (Type F)



Dimensions	value
פווטופווסוטווס	(in mm)
С	0.650
X	0.400
X1	0.480
X2	0.950
Х3	1.700
Υ	0.425
Y1	0.800
Y2	1.150
Y3	1.450
Y4	2.300



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