

**HIGH FREQUENCY HIGH-SIDE AND LOW-SIDE GATE DRIVER IN W-DFN3030-10**

**Description**

The DGD0507 is a high-frequency gate driver capable of driving N-channel MOSFETs. The floating high-side driver is rated up to 50V.

The DGD0507 logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with MCUs. The UVLO for high-side and low-side will protect a MOSFET with loss of supply. To protect MOSFETs, cross conduction prevention logic prevents the HO and LO outputs from being on at the same time.

Fast and well matched propagation delays allow a higher switching frequency, enabling a smaller, more compact power switching design, using smaller associated components. To minimize space an internal bootstrap diode is included.

The DGD0507 is offered in the W-DFN3030-10 (Type TH) package and operates over an extended -40°C to +125°C temperature range.

**Applications**

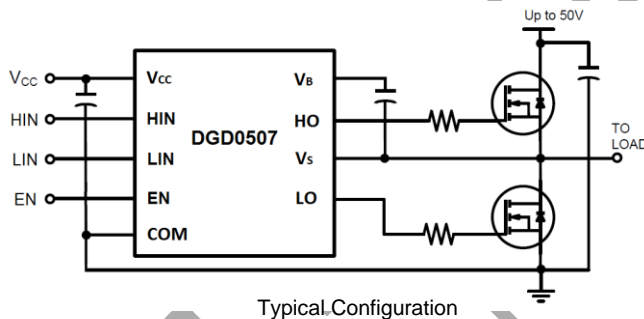
- DC-DC Converters
- Motor Controls
- Battery Powered Hand Tools
- eCig Devices
- Class D Power Amplifiers

**Features**

- 50V Floating High-Side Driver
- Drives Two N-channel MOSFETs in a Half-Bridge Configuration
- 1.25A Source / 2.0A Sink Output Current Capability
- Internal Bootstrap Schottky Diode Included
- Undervoltage Lockout for High-Side and Low-Side Drivers
- Delay Matching a Typical of 5ns
- Propagation Delay Typical of 35ns
- Logic Input (HIN, LIN and EN) 3.3V Capability
- Ultra Low Standby Currents (<1µA)
- Extended Temperature Range: -40°C to +125°C
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony free. "Green" Device (Note 3)**

**Mechanical Data**

- Case: W-DFN3030-10 (Type TH)
- Case Material: Molded Plastic. "Green" Molding Compound  
UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 3 per J-STD-020
- Terminals: Finish – Matte Tin Finish  
Solderable per MIL-STD-202, Method 208 <sup>(e3)</sup>
- Weight: 0.017 grams (Approximate)



**Ordering Information** (Note 4)

Product	Marking	Reel Size (inches)	Tape Width (mm)	Quantity per Reel
DGD0507FN-7	DGD0507	7	8	3,000

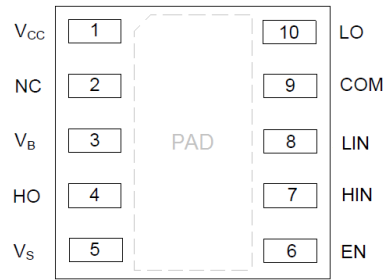
- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

**Marking Information**



DGD0507 = Product Type Marking Code  
 YY = Year (ex: 17 = 2017)  
 WW = Week (01 to 53)

## Pin Diagrams

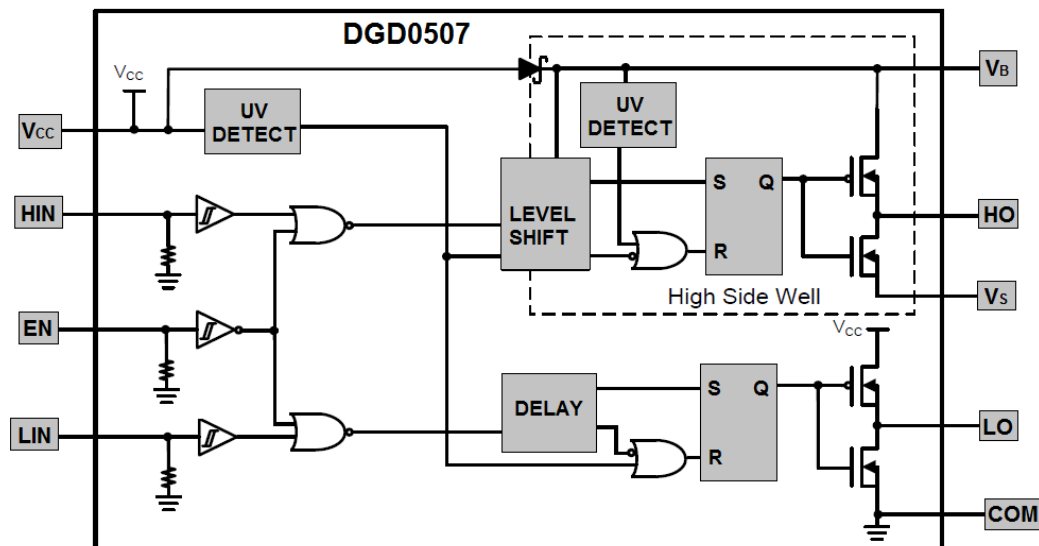


Top View: W-DFN3030-10 (Type TH)

## Pin Descriptions

Pin Number	Pin Name	Function
1	V <sub>CC</sub>	Low-Side and Logic Supply
2	NC	No Connect (No Internal Connection)
3	V <sub>B</sub>	High-Side Floating Supply
4	HO	High-Side Gate Drive Output
5	V <sub>S</sub>	High-Side Floating Supply Return
6	EN	Logic Input Enable, a Logic Low Turns off Gate Driver
7	HIN	Logic Input for High-Side Gate Driver, in Phase with HO
8	LIN	Logic Input for Low-Side Gate Driver, in Phase with LO
9	COM	Low-Side and Logic Return
10	LO	Low-Side Gate Drive Output
PAD	Substrate	Connect to COM on PCB

## Functional Block Diagram



**Absolute Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
High-Side Floating Positive Supply Voltage	V <sub>B</sub>	-0.3 to +50	V
High-Side Floating Negative Supply Voltage	V <sub>S</sub>	V <sub>B</sub> -14 to V <sub>B</sub> +0.3	V
High-Side Floating Output Voltage	V <sub>HO</sub>	V <sub>S</sub> -0.3 to V <sub>B</sub> +0.3	V
Offset Supply Voltage Transient	dV <sub>S</sub> / dt	50	V/ns
Logic and Low-Side Fixed Supply Voltage	V <sub>CC</sub>	-0.3 to +15	V
Low-Side Output Voltage	V <sub>LO</sub>	-0.3 to V <sub>CC</sub> +0.3	V
Logic Input Voltage (HIN, LIN and EN)	V <sub>IN</sub>	-0.3 to 15	V

**Thermal Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Power Dissipation Linear Derating Factor (Note 5)	P <sub>D</sub>	0.4	W
Thermal Resistance, Junction to Ambient (Note 5)	R <sub>θJA</sub>	64	°C/W
Thermal Resistance, Junction to Case (Note 5)	R <sub>θJC</sub>	42	°C/W
Operating Temperature	T <sub>J</sub>	+150	°C
Lead Temperature (Soldering, 10s)	T <sub>L</sub>	+300	
Storage Temperature Range	T <sub>STG</sub>	-55 to +150	

Note: 5. When mounted on a standard JEDEC 2-layer FR-4 board.

**Recommended Operating Conditions**

Parameter	Symbol	Min	Max	Unit
High-Side Floating Supply	V <sub>B</sub>	V <sub>S</sub> + 8	V <sub>S</sub> + 14	V
High-Side Floating Supply Offset Voltage	V <sub>S</sub>	(Note 6)	50 (Note 7)	V
High-Side Floating Output Voltage	V <sub>HO</sub>	V <sub>S</sub>	V <sub>B</sub>	V
Logic and Low Side Fixed Supply Voltage	V <sub>CC</sub>	8	14	V
Low-Side Output Voltage	V <sub>LO</sub>	0	V <sub>CC</sub>	V
Logic Input Voltage (HIN, LIN and EN)	V <sub>IN</sub>	0	5	V
Ambient Temperature	T <sub>A</sub>	-40	+125	°C

Notes: 6. Logic operation for V<sub>S</sub> of -5V to +50V. Logic state held for V<sub>S</sub> of -5V to -V<sub>BS</sub>.  
7. Provided V<sub>B</sub> doesn't exceed absolute maximum rating of 50V.

**DC Electrical Characteristics** ( $V_{CC} = V_{BS} = 12V$ ,  $COM = V_S = 0V$ , @ $T_A = +25^\circ C$ , unless otherwise specified.) (Note 8)

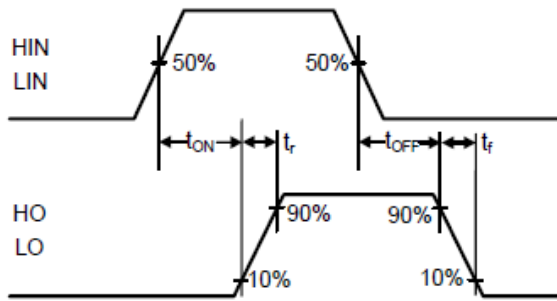
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Logic "1" Input Voltage	$V_{IH}$	2.4	–	–	V	–
Logic "0" Input Voltage	$V_{IL}$	–	–	0.8	V	–
Enable Logic "1" Input Voltage	$V_{ENIH}$	1.5	–	–	V	–
Enable Logic "0" Input Voltage	$V_{ENIL}$	–	–	0.7	V	–
Input Voltage Hysteresis	$V_{INHYS}$	–	0.6	–	V	–
Enable Input Voltage Hysteresis	$V_{ENINHYS}$	–	0.1	–	V	–
High Level Output Voltage, $V_{BIAS} - V_O$	$V_{OH}$	–	0.45	0.6	V	$I_{O+} = 100mA$
Low Level Output Voltage, $V_O$	$V_{OL}$	–	0.15	0.22	V	$I_{O-} = 100mA$
Offset Supply Leakage Current	$I_{LK}$	–	10	50	$\mu A$	$V_B = V_S = 50V$
$V_{CC}$ Shutdown Supply Current	$I_{CCSD}$	–	0	1	$\mu A$	$V_{IN} = 0V$ or $5V$ , $V_{EN} = 0V$
$V_{CC}$ Quiescent Supply Current	$I_{CCQ}$	100	150	200	$\mu A$	$V_{IN} = 0V$ or $5V$
$V_{CC}$ Operating Supply Current	$I_{CCOP}$	–	2.1	3.0	mA	$f_s = 500kHz$
$V_{BS}$ Quiescent Supply Current	$I_{BSQ}$	–	62	100	$\mu A$	$V_{IN} = 0V$ or $5V$
$V_{BS}$ Operating Supply Current	$I_{BSOP}$	–	1.1	2.0	mA	$f_s = 500kHz$
Logic "1" Input Bias Current	$I_{IN+}$	–	–	50	$\mu A$	$V_{IN} = 5V$
Logic "0" Input Bias Current	$I_{IN-}$	–	–	5	$\mu A$	$V_{IN} = 0V$
Enable Logic "1" Input Bias Current	$I_{ENIN+}$	–	43	60	$\mu A$	$V_{IN} = 5V$
Enable Logic "0" Input Bias Current	$I_{ENIN-}$	–	0	5	$\mu A$	$V_{IN} = 0V$
$V_{BS}$ Supply Undervoltage Positive Going Threshold	$V_{BSUV+}$	5.9	6.9	7.9	V	–
$V_{BS}$ Supply Undervoltage Negative Going Threshold	$V_{BSUV-}$	5.6	6.6	7.6	V	–
$V_{CC}$ Supply Undervoltage Positive Going Threshold	$V_{CCUV+}$	5.9	6.9	7.9	V	–
$V_{CC}$ Supply Undervoltage Negative Going Threshold	$V_{CCUV-}$	5.6	6.6	7.6	V	–
Output High Short Circuit Pulsed Current	$I_{O+}$	0.9	1.25	–	A	$V_O = 0V$ , $PW \leq 10\mu s$
Output Low Short Circuit Pulsed Current	$I_{O-}$	1.5	2.0	–	A	$V_O = 15V$ , $PW \leq 10\mu s$
Forward Voltage of Bootstrap Diode	$V_{F1}$	–	0.27	–	V	$I_F = 100\mu A$
Forward Voltage of Bootstrap Diode	$V_{F2}$	–	0.8	–	V	$I_F = 100mA$

Note: 8. The  $V_{IN}$  and  $I_{IN}$  parameters are applicable to the two logic pins: HIN, LIN and EN. The  $V_O$  and  $I_O$  parameters are applicable to the respective output pins: HO and LO.

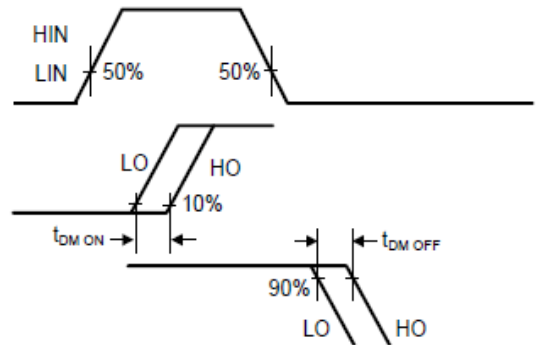
**AC Electrical Characteristics** ( $V_{CC} = V_{BS} = 12V$ ,  $COM = V_S = 0V$ ,  $C_L = 1000pF$ , @ $T_A = +25^\circ C$ , unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Turn-On Propagation Delay	$t_{ON}$	–	20	35	ns	–
Turn-Off Propagation Delay	$t_{OFF}$	–	23	56	ns	$V_S = 50V$
Delay Matching, HO & LO Turn-On	$t_{DM}$	–	–	5	ns	–
Turn-On Rise Time	$t_R$	–	23	35	ns	–
Turn-Off Fall Time	$t_F$	–	18	25	ns	–

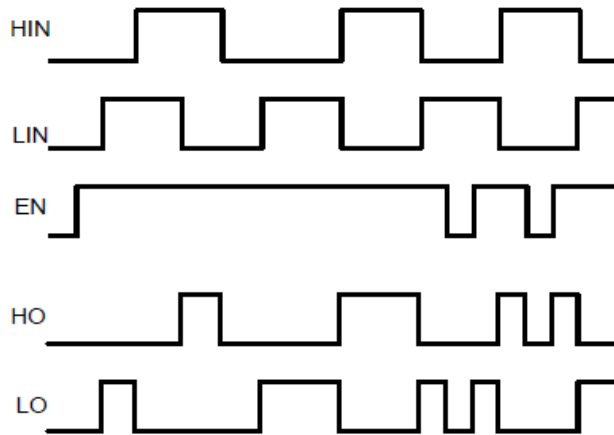
**Timing Waveforms**



**Figure 1. Switching Time Waveform Definitions**



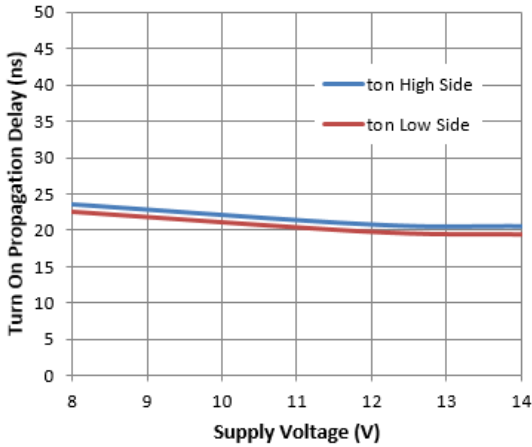
**Figure 2. Delay Matching Waveform Definitions**



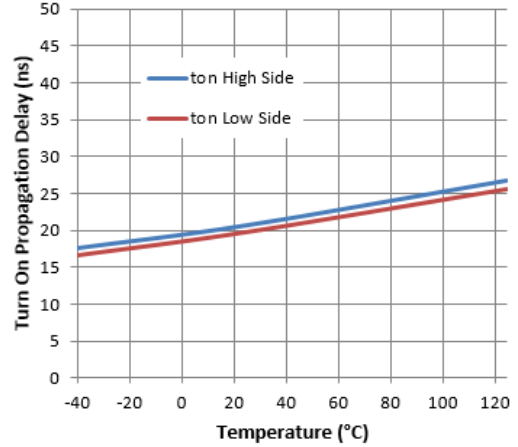
**Figure 3. Input / Output Timing Diagram**

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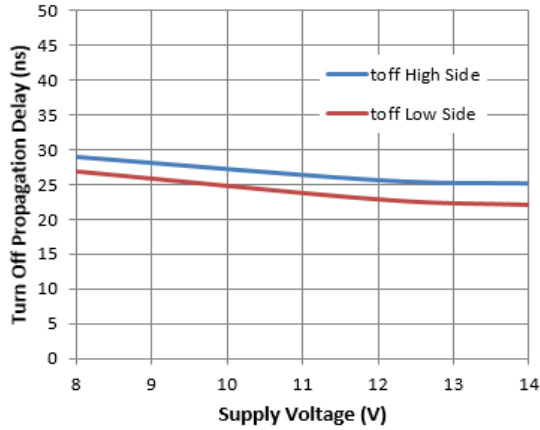
**Typical Performance Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)



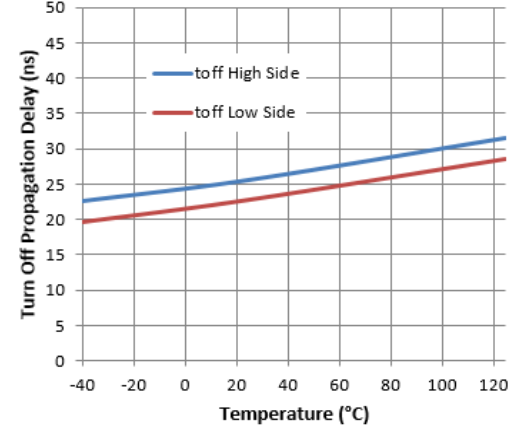
**Figure 4.** Turn-on Propagation Delay vs. Supply Voltage



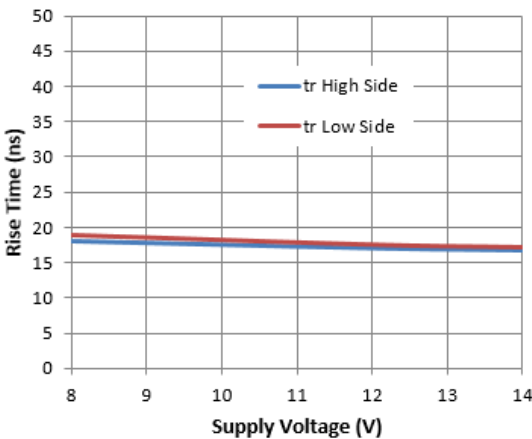
**Figure 5.** Turn-on Propagation Delay vs. Temperature



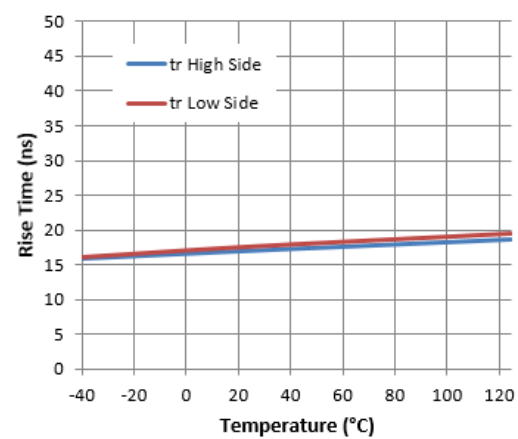
**Figure 6.** Turn-off Propagation Delay vs. Supply Voltage



**Figure 7.** Turn-off Propagation Delay vs. Temperature

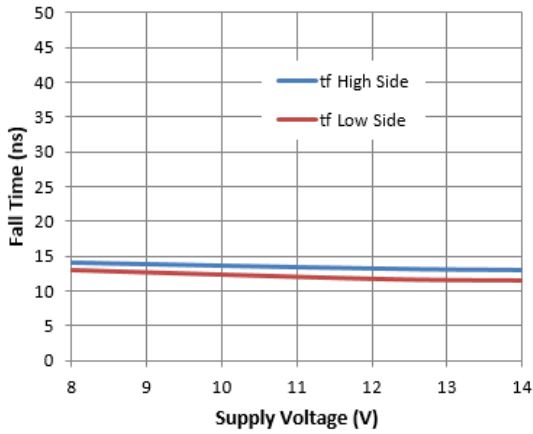


**Figure 8.** Rise Time vs. Supply Voltage

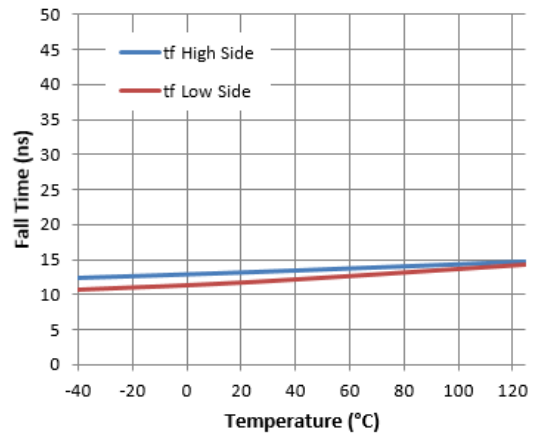


**Figure 9.** Rise Time vs. Temperature

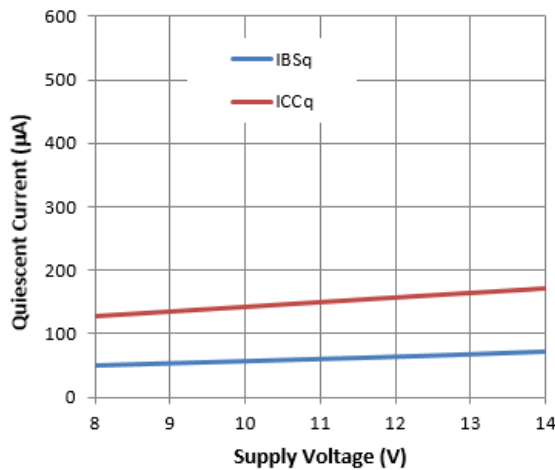
**Typical Performance Characteristics (Cont.)**



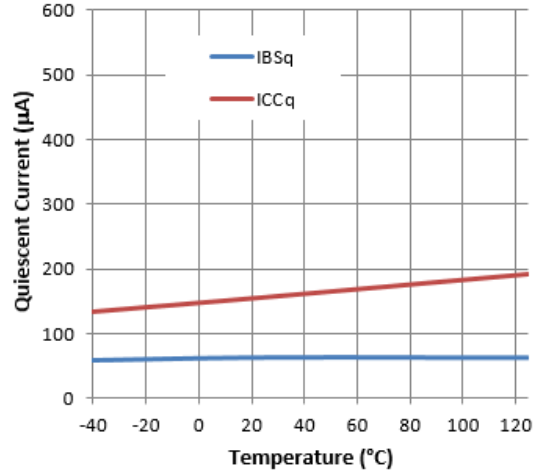
**Figure 10.** Fall Time vs. Supply Voltage



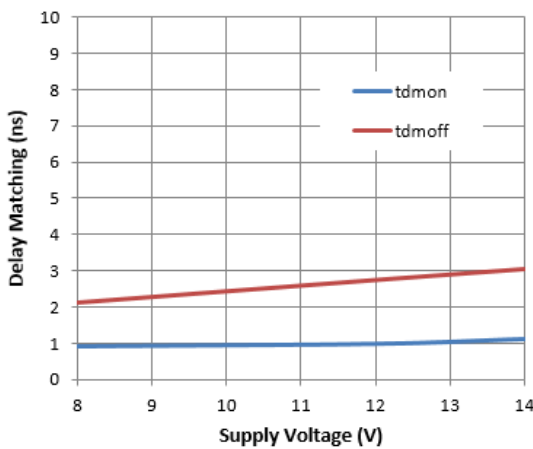
**Figure 11.** Fall Time vs. Temperature



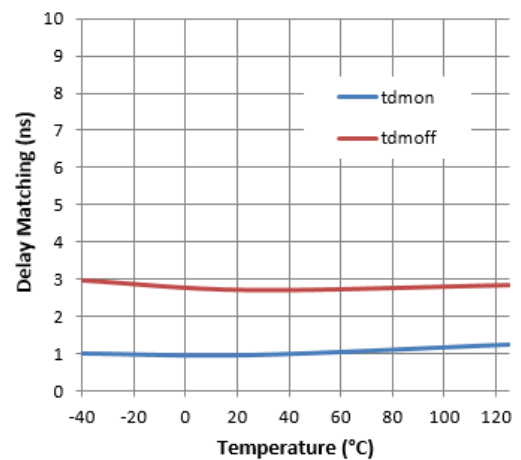
**Figure 12.** Quiescent Current vs. Supply Voltage



**Figure 13.** Quiescent Current vs. Temperature

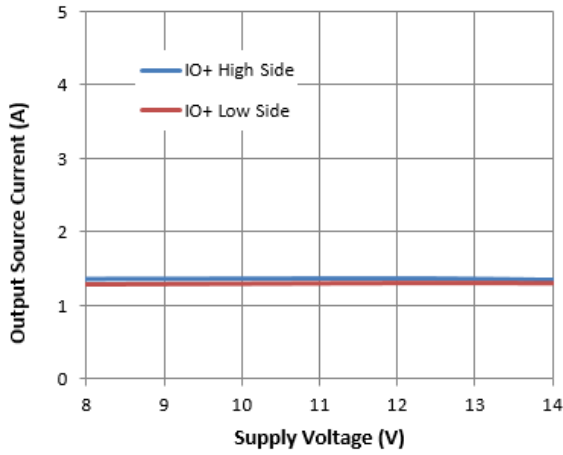


**Figure 14.** Delay Matching vs. Supply Voltage

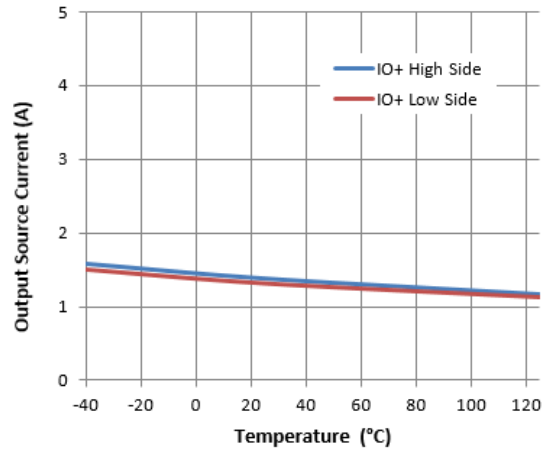


**Figure 15.** Delay Matching vs. Temperature

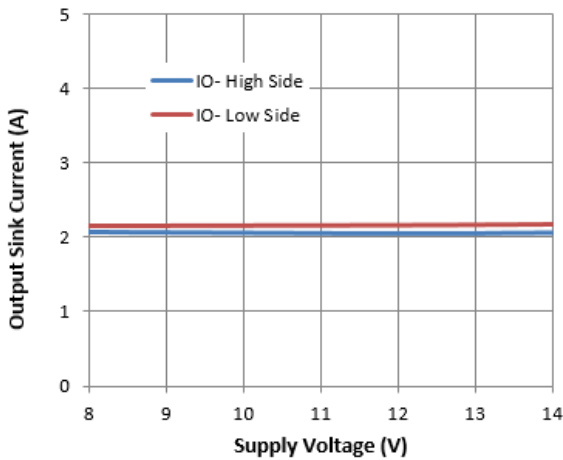
**Typical Performance Characteristics (Cont.)**



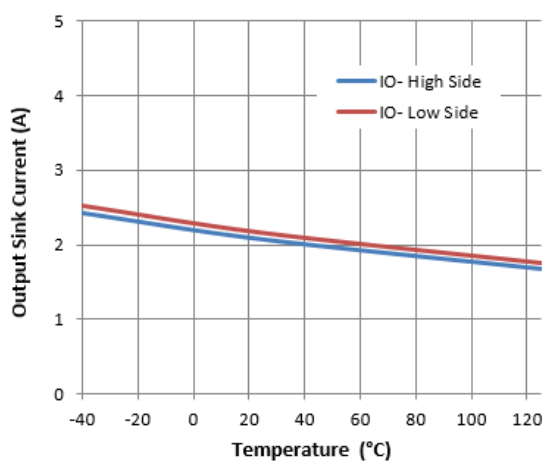
**Figure 16.** Output Source Current vs. Supply Voltage



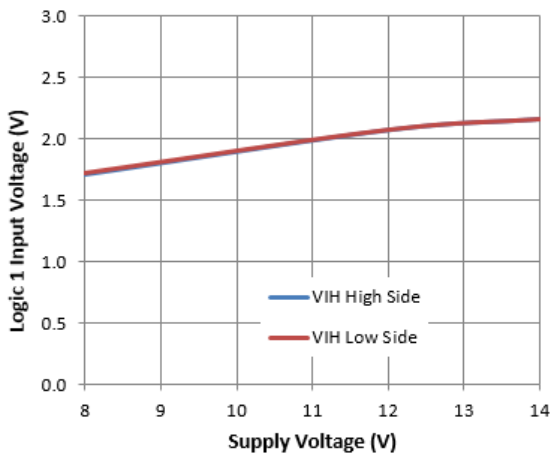
**Figure 17.** Output Source Current vs. Temperature



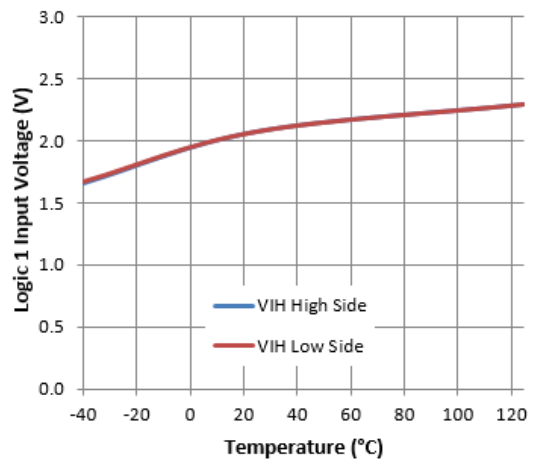
**Figure 18.** Output Sink Current vs. Supply Voltage



**Figure 19.** Output Sink Current vs. Temperature



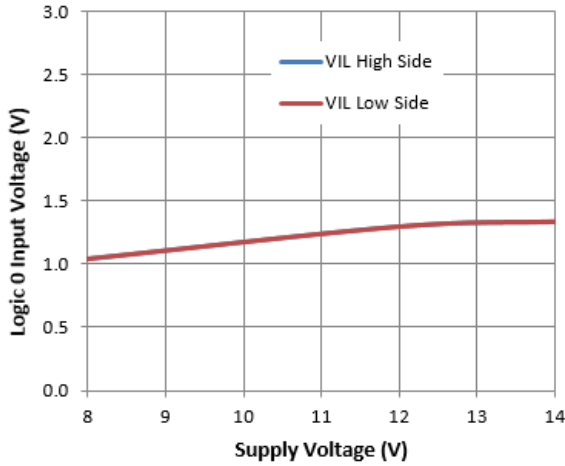
**Figure 20.** Logic 1 Input Voltage vs. Supply Voltage



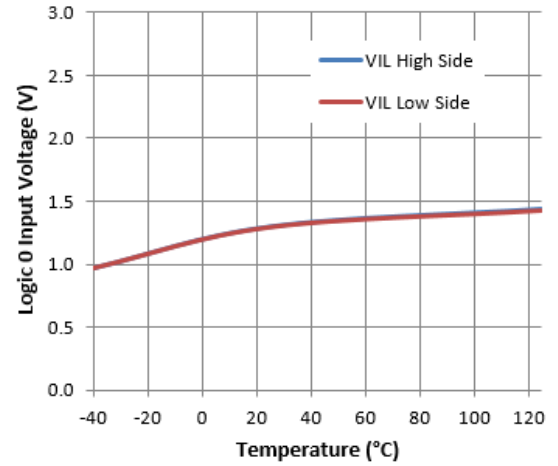
**Figure 21.** Logic 1 Input Voltage vs. Temperature



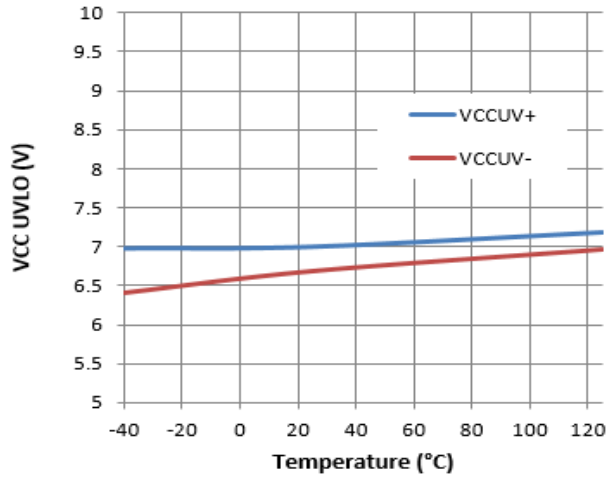
**Typical Performance Characteristics (Cont.)**



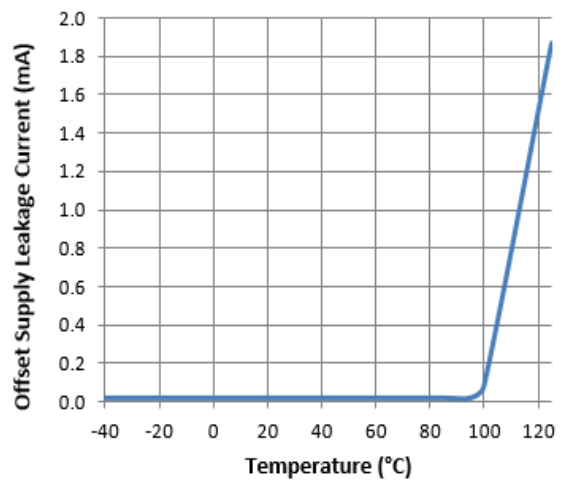
**Figure 22.** Logic 0 Input Voltage vs. Supply Voltage



**Figure 23.** Logic 0 Input Voltage vs. Temperature



**Figure 24.** VCC UVLO vs. Temperature



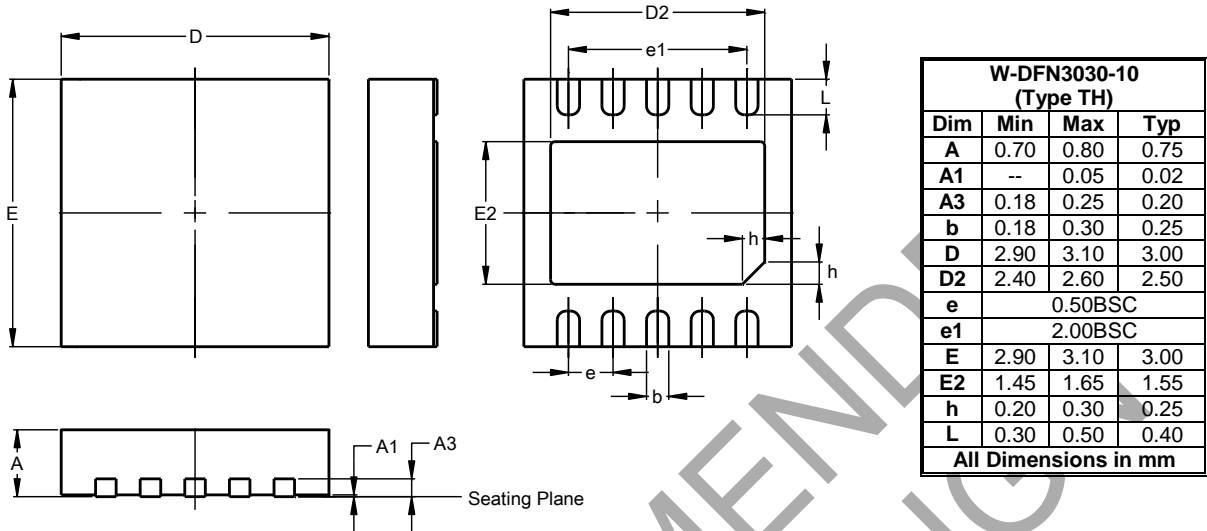
**Figure 25.** Offset Supply Leakage Current vs. Temperature

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**Package Outline Dimensions**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

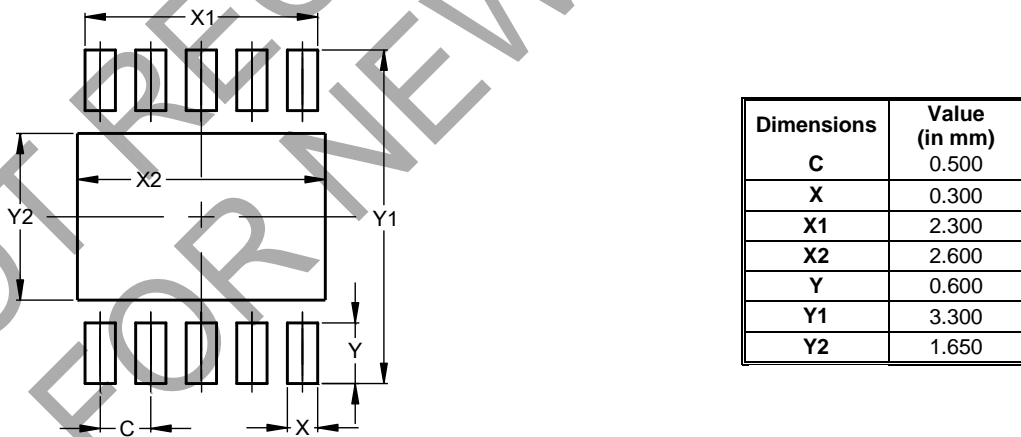
**W-DFN3030-10 (Type TH)**



**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**W-DFN3030-10 (Type TH)**



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