

## Description

The AP7176B is a 3.0A ultra low-dropout (LDO) linear regulator that features an enable input and a power-good output.

The enable input and power-good output allow users to configure power management solutions that can meet the sequencing requirements of FPGAs, DSPs, and other applications with different startup and power-down requirements.

The AP7176B features two supply inputs, for power conversion supply and control. With the separation of the control and the power input very low dropout voltages can be reached and power dissipation is reduced.

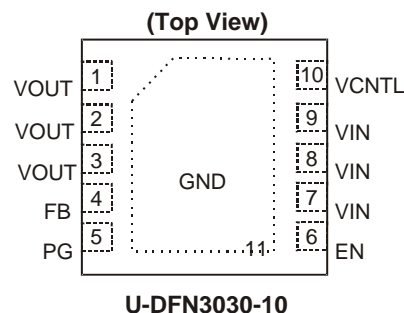
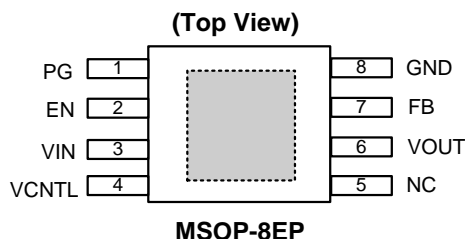
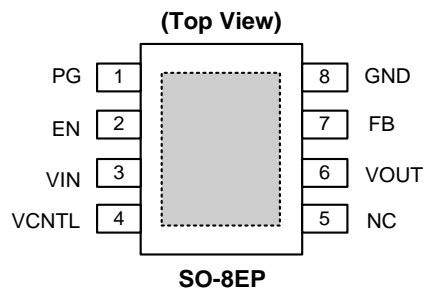
A precision reference and feedback control deliver 1.5% accuracy over load, line, and operating temperature ranges.

The AP7176B is available in SO-8EP, MSOP-8EP and U-DFN3030-10 packages with an exposed PAD to reduce the junction to case resistance and extend the temperature range it can be used in.

## Features

- $V_{IN}$  Range: 1.2V to 3.65V,  $V_{CNTL}$  3.0V to 5.5V
- Adjustable Output Voltage
- Continuous Output Current  $I_{OUT} = 3A$
- Fast Transient Response
- Power-On-Reset Monitoring on  $V_{CNTL}$  and  $V_{IN}$
- Internal Soft-Start
- Stable with Low ESR MLCC Capacitors
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](https://www.diodes.com/quality/product-definitions/) or your local Diodes representative. <https://www.diodes.com/quality/product-definitions/>**

## Pin Assignments



= PAD  
(connected to ground plane for better heat dissipation)

## Applications

- Notebooks
- PCs
- Netbooks
- Wireless communication
- Servers
- Motherboards
- Dongles
- Front side bus VTT (1.2V/3.3A)

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.  
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.  
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

**Typical Applications Circuit**

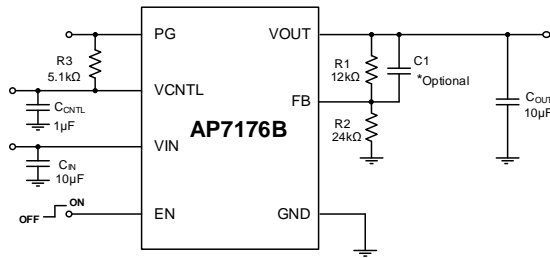
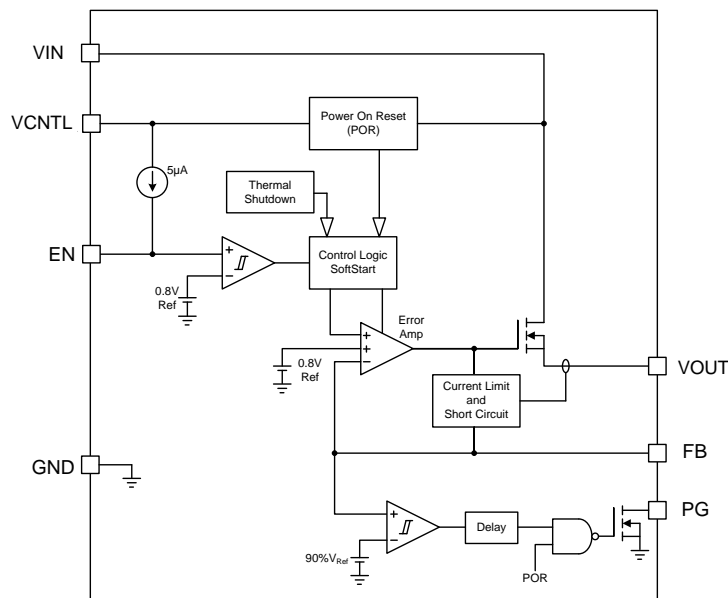


Figure 1. Typical Application Circuit

**Pin Descriptions**

Pin Name	Pin Number			Function
	SO-8EP	MSOP-8EP	U-DFN3030-10	
PG	1	1	5	Power-Good. Output open drain to indicate the status of V <sub>OUT</sub> via monitoring the FB pin. This pin is pulled low when the voltage is outside the limits, during thermal shutdown and if either V <sub>CTRL</sub> or V <sub>IN</sub> goes below their thresholds.
EN	2	2	6	Enable pin. Driving this pin low will disable the part. When left floating an internal current source will pull this pin high and enable it.
VIN	3	3	7, 8, 9	Power input pin for current supply. Connect a decoupling capacitor (≥ 10μF) as close as possible to the pin for noise filtering.
VCNTL	4	4	10	BIAS supply for the controller, recommended 5V. Connect a decoupling capacitor (≥ 1μF) as close as possible to the pin for noise filtering.
NC	5	5	—	No connection
VOUT	6	6	1, 2, 3	Power output pin
FB	7	7	4	Feedback to set the output voltage via an external resistor divider between V <sub>OUT</sub> and GND
GND	8	8	11	Ground
PAD	EP	EP	EP	Exposed pad connected to GND for good thermal conductivity.

**Functional Block Diagram**



**Absolute Maximum Ratings** (Note 4) (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
V <sub>IN</sub>	VIN Supply Voltage (VIN to GND)	-0.3 to +4.0	V
V <sub>CNTL</sub>	VCNTL Supply Voltage (VCNTL to GND)	-0.3 to +7.0	V
V <sub>OUT</sub>	VOUT to GND Voltage	-0.3 to V <sub>IN</sub> +0.3	V
—	PG to GND Voltage	-0.3 to +7.0	V
—	EN, FB to GND Voltage	-0.3 to V <sub>CNTL</sub> +0.3	V
P <sub>D</sub>	Power Dissipation (SO-8EP)	1.7	W
	Power Dissipation (MSOP-8EP)	1.5	
	Power Dissipation (U-DFN3030-10)	1.9	
T <sub>J</sub>	Maximum Junction Temperature	+150	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
T <sub>SDR</sub>	Maximum Lead Soldering Temperature, 10 Seconds	+260	°C

Note: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.

**Recommended Operating Conditions** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Symbol	Parameter	Test Condition	Range	Unit
V <sub>CNTL</sub>	VCNTL Supply Voltage		3.0 to 5.5	V
V <sub>IN</sub>	VIN Supply Voltage		1.2 to 3.65	V
V <sub>OUT</sub>	VOUT Output Voltage (when V <sub>CNTL</sub> - V <sub>OUT</sub> > 1.9V)		0.8 to V <sub>IN</sub> - V <sub>DROP</sub>	V
I <sub>OUT</sub>	VOUT Output Current		0 to 3	A
C <sub>OUT</sub>	VOUT Output Capacitance	I <sub>OUT</sub> = 3A at 25% nominal V <sub>OUT</sub>	8 to 1100	μF
		I <sub>OUT</sub> = 2A at 25% nominal V <sub>OUT</sub>	8 to 1700	
		I <sub>OUT</sub> = 1A at 25% nominal V <sub>OUT</sub>	8 to 2400	
ESRCOUT	ESR of VOUT Output Capacitor		0 to 200	mΩ
T <sub>A</sub>	Ambient Temperature		-40 to +85	°C
T <sub>J</sub>	Junction Temperature		-40 to +125	°C

**Electrical Characteristics** (Specifications apply over V<sub>CNTL</sub> = 5V, V<sub>IN</sub> = 1.8V, V<sub>OUT</sub> = 1.2V and T<sub>A</sub> = -40°C to +85°C, typical values @T<sub>A</sub> = +25°C, unless otherwise specified.)

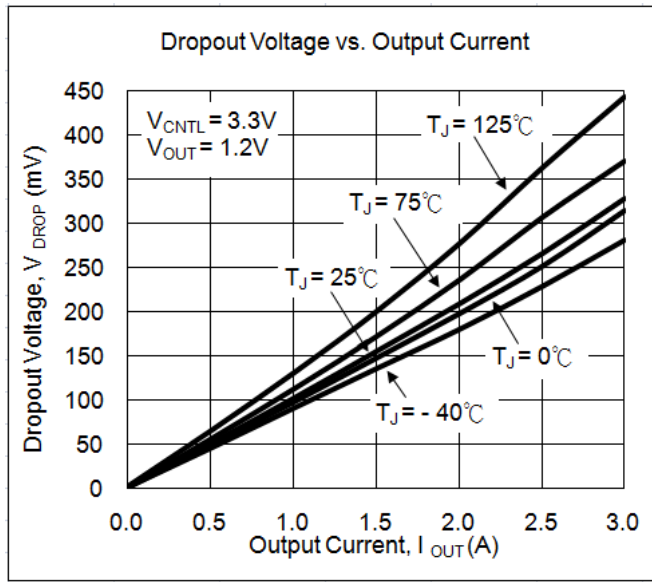
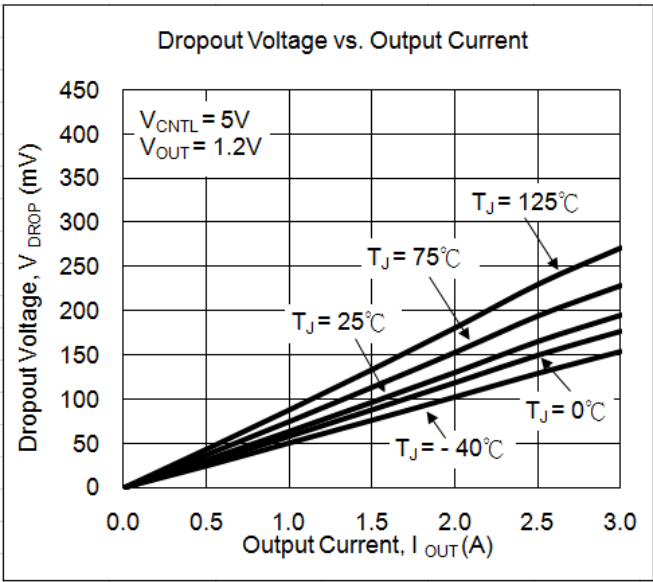
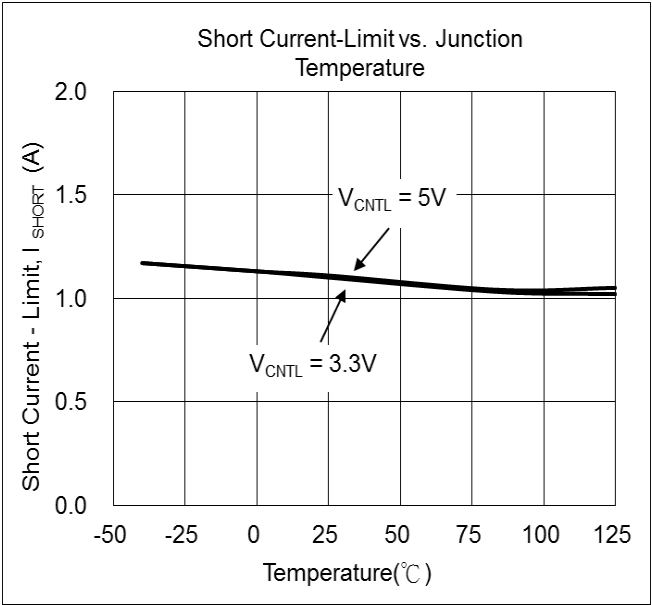
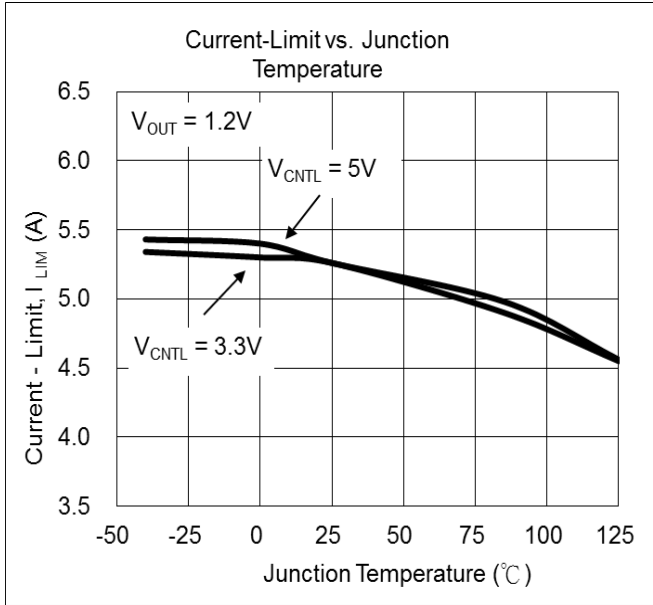
Symbol	Parameter	Conditions	AP7176B			Unit
			Min	Typ	Max	
<b>SUPPLY CURRENT</b>						
I <sub>VCNTL</sub>	VCNTL Supply Current	EN = V <sub>CNTL</sub> , I <sub>OUT</sub> = 0A	—	1.0	1.5	mA
I <sub>SD</sub>	VCNTL Supply Current at Shutdown	EN = GND	—	15	30	μA
	VIN Supply Current at Shutdown	EN = GND, V <sub>IN</sub> = 3.65V	—	—	1	μA
<b>POWER-ON RESET (POR)</b>						
V <sub>POR_Rising (VCNTL)</sub>	Rising VCNTL POR Threshold	—	2.50	2.70	2.95	V
V <sub>POR_Hysteresis (VCNTL)</sub>	VCNTL POR Hysteresis	—	—	0.4	—	V
V <sub>POR_Rising (VIN)</sub>	Rising VIN POR Threshold	—	0.8	0.9	1.0	V
V <sub>POR_Hys (VIN)</sub>	VIN POR Hysteresis	—	—	0.5	—	V

**Electrical Characteristics** (continued) (Specifications apply over  $V_{CNTL} = 5V$ ,  $V_{IN} = 1.8V$ ,  $V_{OUT} = 1.2V$  and  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , typical values @  $T_A = +25^{\circ}C$ , unless otherwise specified.)

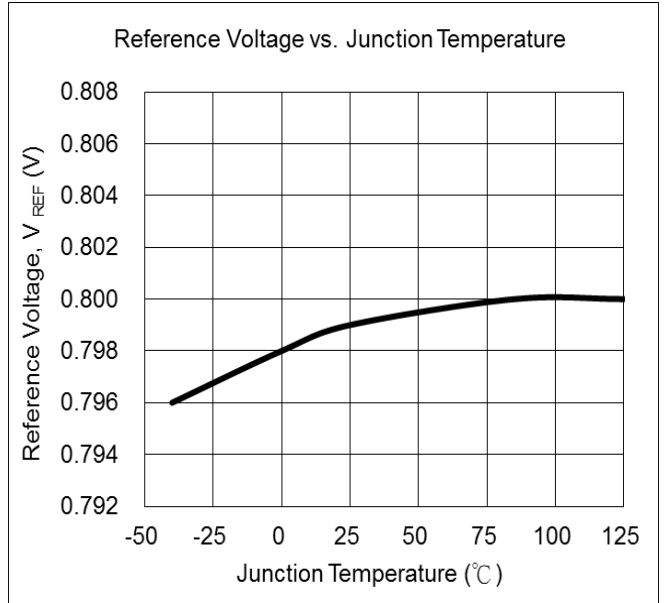
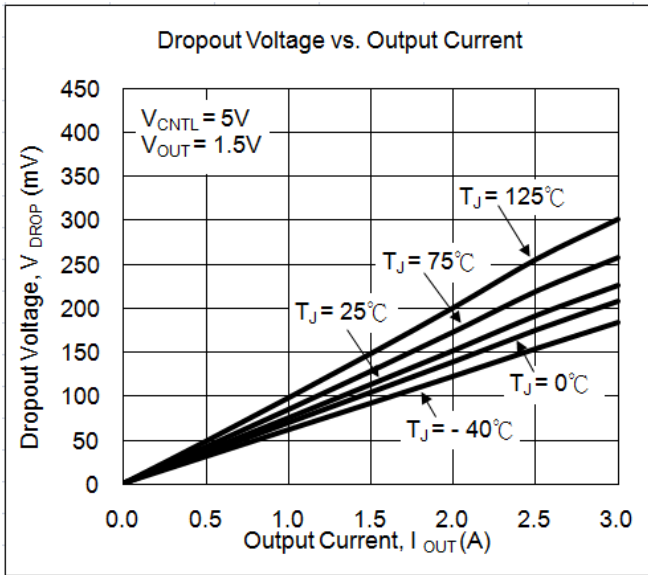
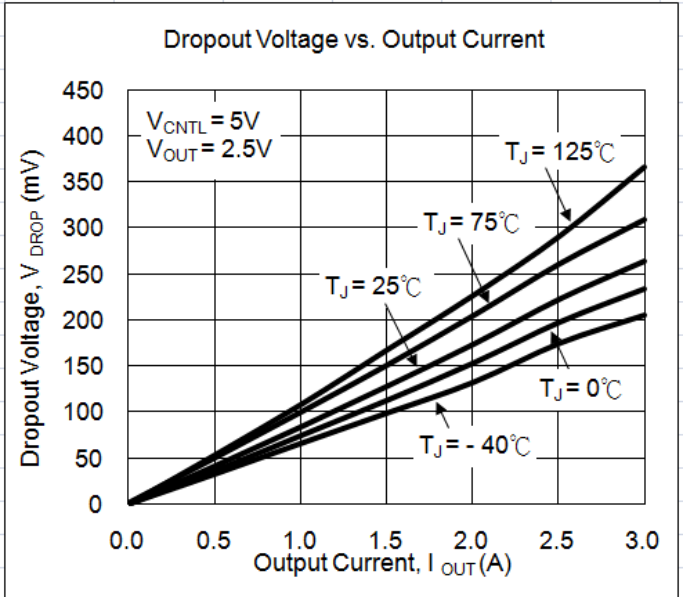
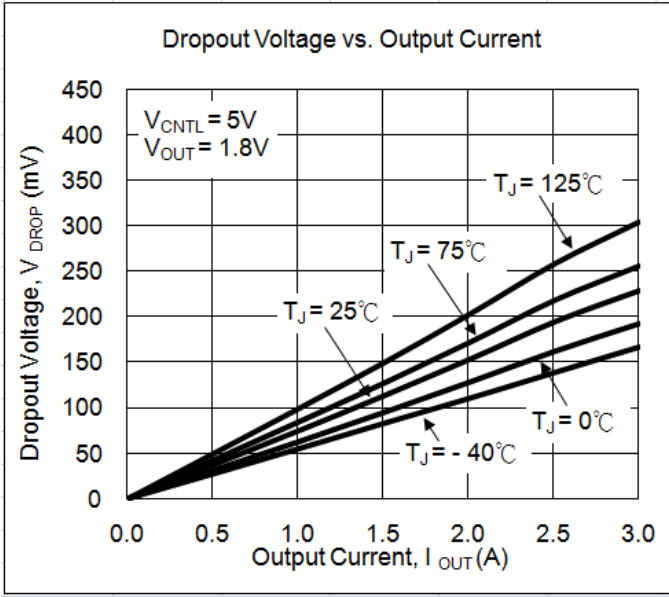
Symbol	Parameter	Conditions	AP7176B			Unit		
			Min	Typ	Max			
<b>OUTPUT VOLTAGE</b>								
V <sub>REF</sub>	Reference Voltage	FB = V <sub>OUT</sub>	—	0.8	—	V		
	Output Voltage Accuracy	V <sub>CNTL</sub> = 3.0V to 5.5V, I <sub>OUT</sub> = 0A to 3A T <sub>J</sub> = -40°C to +125°C	-1.5	—	+1.5	%		
	Load Regulation	I <sub>OUT</sub> = 0A to 3A	—	0.06	0.25	%		
	Line Regulation	I <sub>OUT</sub> = 10mA, V <sub>CNTL</sub> = 3.0V to 5.5V	-0.15	—	+0.15	%/V		
	V <sub>OUT</sub> Pull-Low Resistance	V <sub>CNTL</sub> = 3.3V, V <sub>EN</sub> = 0V, V <sub>OUT</sub> < 0.8V	—	10	—	Ω		
	FB Input Current	V <sub>FB</sub> = 0.8V	-100	—	+100	nA		
<b>DROPOUT VOLTAGE</b>								
V <sub>DROP</sub>	VIN-to-V <sub>OUT</sub> Dropout Voltage (Note 5)	V <sub>CNTL</sub> = 5.0V I <sub>OUT</sub> = 3A	V <sub>OUT</sub> = 2.5V	T <sub>J</sub> = +25°C	—	0.33	0.38	V
				T <sub>J</sub> = -40°C to +125°C	—	—	0.53	
			V <sub>OUT</sub> = 1.8V	T <sub>J</sub> = +25°C	—	0.31	0.36	
				T <sub>J</sub> = -40°C to +125°C	—	—	0.50	
			V <sub>OUT</sub> = 1.2V	T <sub>J</sub> = +25°C	—	0.30	0.35	
				T <sub>J</sub> = -40°C to +125°C	—	—	0.48	
I <sub>LIM</sub>	Current-Limit Level	T <sub>J</sub> = +25°C, V <sub>OUT</sub> = 80% V <sub>NOMINAL</sub> T <sub>J</sub> = -40°C to +125°C	T <sub>J</sub> = +25°C, V <sub>OUT</sub> = 80% V <sub>NOMINAL</sub>	4.5	5.7	6.7	A	
			T <sub>J</sub> = -40°C to +125°C	4.2	—	—	A	
<b>PROTECTIONS</b>								
I <sub>SHORT</sub>	Short Current-Limit Level	V <sub>FB</sub> < 0.2V	—	1.1	—	A		
T <sub>SD</sub>	Thermal Shutdown Temperature	T <sub>J</sub> rising	—	+170	—	°C		
T <sub>SD_HYS</sub>	Thermal Shutdown Hysteresis	—	—	+50	—	°C		
<b>ENABLE AND SOFT-START</b>								
EN_HI	EN Logic High Threshold Voltage	V <sub>EN</sub> rising	0.5	0.8	1.1	V		
EN_Hys	EN Hysteresis	—	—	0.1	—	V		
I <sub>EN</sub>	EN Pull-High Current	EN = GND	—	5	—	μA		
t <sub>SS</sub>	Soft-Start Interval	—	0.3	0.6	1.2	ms		
t <sub>DELAY</sub>	Turn-On Delay	From being enabled to V <sub>OUT</sub> rising 10%	200	350	500	μs		
<b>POWER-GOOD AND DELAY</b>								
V <sub>THPG</sub>	Rising PG Threshold Voltage	V <sub>FB</sub> rising	90	92	95	%		
V <sub>PG_Hys</sub>	PG Threshold Hysteresis	—	—	8	—	%		
V <sub>PG_Low</sub>	PG Pull-Low Voltage	PG sinks 5mA	—	0.25	0.4	V		
t <sub>PG_Deb</sub>	PG Debounce Interval	V <sub>FB</sub> < falling PG voltage threshold	—	10	—	μs		
t <sub>PGDEL</sub>	PG Delay Time	From V <sub>FB</sub> = V <sub>THPG</sub> to rising edge of the V <sub>PG</sub>	1	2	4	ms		
<b>THERMAL CHARACTERISTIC</b>								
θ <sub>JA</sub>	Thermal Resistance Junction-to-Ambient	SO-8EP (Note 6)	—	70	—	°C/W		
		MSOP-8EP (Note 7)	—	80	—	°C/W		
		U-DFN3030-10 (Note 6)	—	60	—	°C/W		
θ <sub>JC</sub>	Thermal Resistance Junction-to-Case	SO-8EP (Note 6)	—	30	—	°C/W		
		MSOP-8EP (Note 7)	—	30	—	°C/W		
		U-DFN3030-10 (Note 6)	—	20	—	°C/W		

Notes: 5. Dropout voltage is the voltage difference between the input and the output at which the output voltage drops 2% below its nominal value.  
6. Device mounted on 2" x 2" FR-4 substrate PC board, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.  
7. Device mounted on 2" x 2" FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

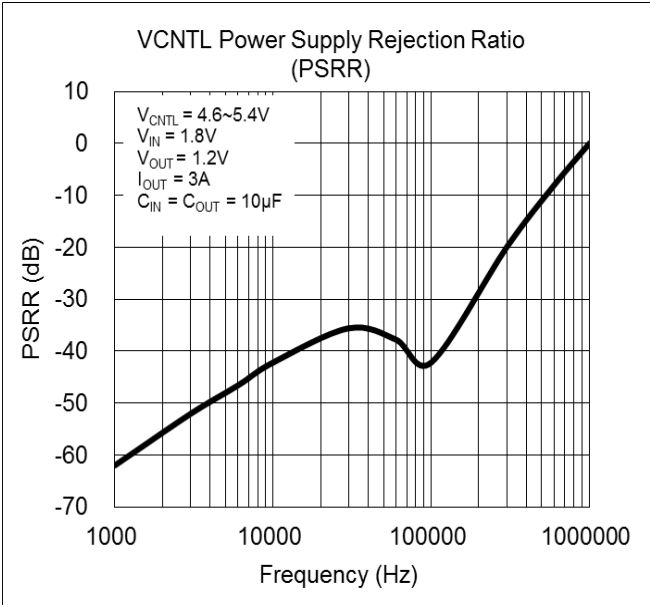
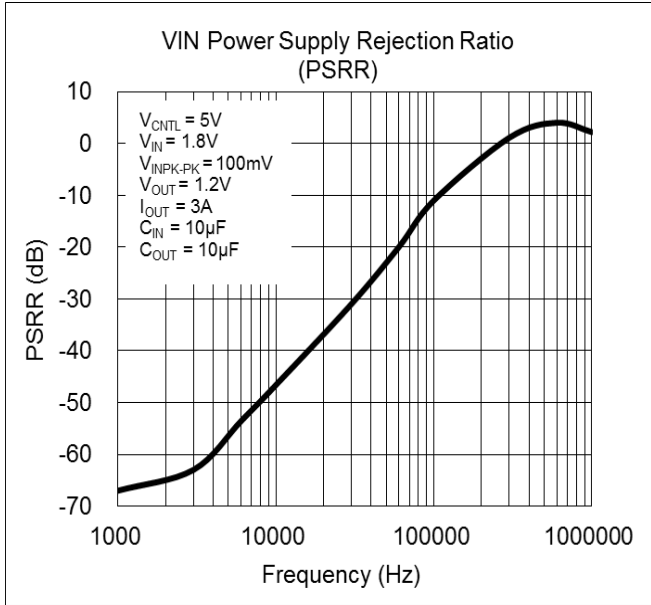
**Typical Characteristics**



**Typical Characteristics** (continued)

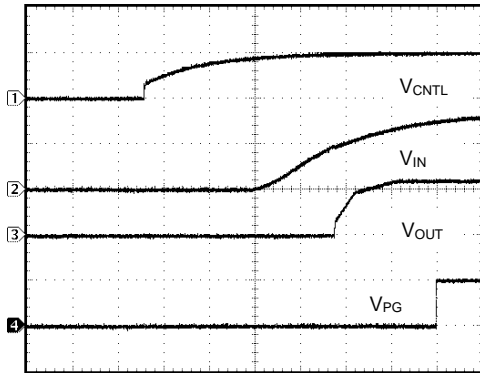


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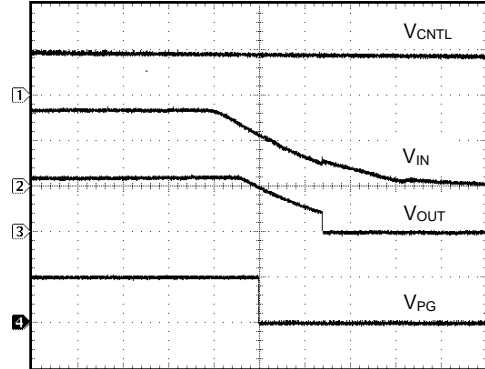
**Operating Waveforms** (Test Conditions  $V_{IN} = 1.8V$ ,  $V_{CNTL} = 5V$ ,  $V_{OUT} 1.2V$ ,  $T_A = +25^\circ C$  unless otherwise specified.)

**Power On**



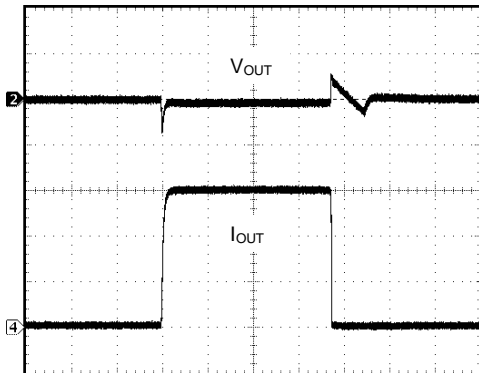
$C_{OUT} = 10\mu F$ ,  $C_{IN} = 10\mu F$ ,  $R_L = 0.4\Omega$   
 CH1:  $V_{CNTL}$ , 5V/Div, DC  
 CH2:  $V_{IN}$ , 1V/Div, DC  
 CH3:  $V_{OUT}$ , 1V/Div, DC  
 CH4:  $V_{PG}$ , 5V/Div, DC  
 TIME: 2ms/Div

**Power Off**



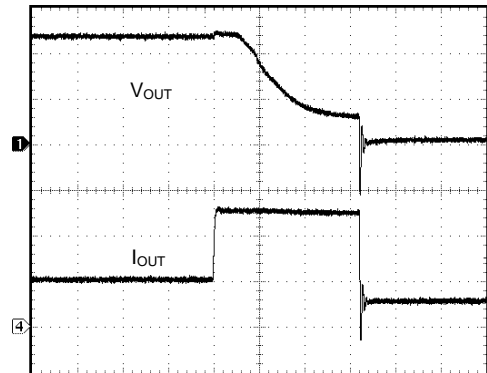
$C_{OUT} = 10\mu F$ ,  $C_{IN} = 10\mu F$ ,  $R_L = 0.4\Omega$   
 CH1:  $V_{CNTL}$ , 5V/Div, DC  
 CH2:  $V_{IN}$ , 1V/Div, DC  
 CH3:  $V_{OUT}$ , 1V/Div, DC  
 CH4:  $V_{PG}$ , 5V/Div, DC  
 TIME: 2ms/Div

**Load Transient Response**



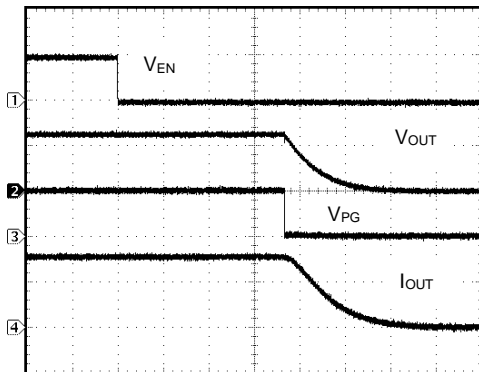
$I_{OUT} = 10mA$  to  $3A$  to  $10mA$  (rise / fall time =  $1\mu s$ )  
 $C_{OUT} = 10\mu F$ ,  $C_{IN} = 10\mu F$   
 CH2:  $V_{OUT}$ , 50mV/Div, AC  
 CH4:  $I_{OUT}$ , 1A/Div, DC  
 TIME: 50µs/Div

**Overcurrent Protection**



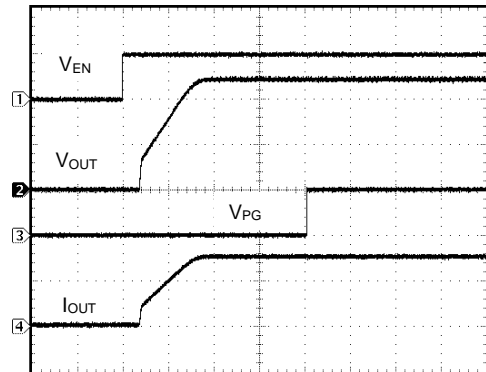
$C_{OUT} = 10\mu F$ ,  $C_{IN} = 10\mu F$ ,  $I_{OUT} = 2A$  to  $5.6A$   
 CH1:  $V_{OUT}$ , 0.5V/Div, DC  
 CH4:  $I_{OUT}$ , 2A/Div, DC  
 TIME: 0.2ms/Div

**Shutdown**



$C_{OUT} = 10\mu F$ ,  $C_{IN} = 10\mu F$ ,  $R_L = 0.4\Omega$   
 CH1:  $V_{EN}$ , 5V/Div, DC  
 CH2:  $V_{OUT}$ , 1V/Div, DC  
 CH3:  $V_{PG}$ , 5V/Div, DC  
 CH4:  $I_{OUT}$ , 2A/Div, DC  
 TIME: 4µs/Div

**Enable**



$C_{OUT} = 10\mu F$ ,  $C_{IN} = 10\mu F$ ,  $R_L = 0.4\Omega$   
 CH1:  $V_{EN}$ , 5V/Div, DC  
 CH2:  $V_{OUT}$ , 1V/Div, DC  
 CH3:  $V_{PG}$ , 5V/Div, DC  
 CH4:  $I_{OUT}$ , 2A/Div, DC  
 TIME: 1ms/Div



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## Application Information

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### Power-Good and Delay

AP7176B monitors the feedback voltage  $V_{FB}$  on the FB pin. An internal delay timer is started after the PG voltage threshold ( $V_{THPG}$ ) on the FB pin is reached. At the end of the delay time an internal nMOS of the PG is turned off to indicate that the power at the output is good (PG). This monitoring function is continued during operation and if  $V_{FB}$  falls 8% (typ) below  $V_{THPG}$ , the nMOS of the PG is turned on after a delay time of typical 10 $\mu$ s to avoid oscillating of the PG signal.

### Power-On Reset

AP7176B monitors both supply voltages,  $V_{CNTL}$  and  $V_{IN}$  to ensure operation as intended. A Soft-Start process is initiated after both voltages exceed their POR threshold during power on. During operation the POR component continues to monitor the supply voltage and pulls the PG low to indicate an out of regulation supply. This function will engage without regard to the status of the output.

### Soft-Start

AP7176B incorporates an internal Soft-Start function. The output voltage rise is controlled to limit the current surge during startup. The typical Soft-Start time is 0.6ms

### Current-Limit Protection

AP7176B monitors the current flow through the nMOS and limits the maximum current to avoid damage to the load and AP7176B during overload conditions.

### Short-Circuit Current-Limit Protection

AP7176B incorporates a current-limit function to reduce the maximum current to 1.1A (typ) when the voltage at FB falls below 0.2V (typ) during an overload or short-circuit situation.

During startup period, this function is disabled to ensure successful heavy load startup.

### Enable Control

If the enable pin (EN) is left open, an internal current source around 5 $\mu$ A pulls the pin up and enables the AP7176B. This will reduce the bill of material saving an external pullup resistor. Driving the enable pin low disables the device. Driving the pin high subsequently initiates a new Soft-Start cycle.

### Output Voltage Regulation

Output Voltage is set by resistor divider from  $V_{OUT}$  via FB pin to GND. Internally  $V_{FB}$  is compared to a 0.8V temperature compensated reference voltage and the nMOS pass element regulates the output voltage while delivering current from  $V_{IN}$  to  $V_{OUT}$ .

### Setting the Output Voltage

A resistor divider connected to FB pin programs the output voltage.

$$V_{OUT} = V_{REF} * \left( 1 + \frac{R1}{R2} \right) V$$

R1 is connected from  $V_{OUT}$  to FB with Kelvin sensing connection. R2 is connected from FB to GND. To improve load transient response and stability, a bypass capacitor can be connected in parallel with R1. (optional in typical application circuit)

### Power Sequencing

AP7176B requires no specific sequencing between  $V_{IN}$  and  $V_{CNTL}$ . However, care should be taken to avoid forcing  $V_{OUT}$  for prolonged times without the presence of  $V_{IN}$ . Conduction through internal parasitic diode (from  $V_{OUT}$  to  $V_{IN}$ ) could damage AP7176B.

### Thermal Shutdown

The PCB layout and power requirements for AP7176B under normal operation condition should allow enough cooling to restrict the junction temperature to +125°C. The packages for AP7176B have an exposed PAD to support this. These packages provide better connection to the PCB and thermal performance. Refer to the *Layout Consideration*.

If AP7176B junction temperature reaches +170°C a thermal protection block disables the nMOS pass element and lets the part cool down. After its junction temperature drops by 50°C (typ), a new Soft-Start cycle will be initiated. A new thermal protection will start, if the load or ambient conditions continue to raise the junction temperature to +170°C. This cycle will repeat until normal operation temperature is maintained again.

## Application Information (continued)

### Output Capacitor

An output capacitor ( $C_{OUT}$ ) is needed to improve transient response and maintain stability. The ESR (equivalent series resistance) and capacitance drives the selection. Care needs to be taken to cover the entire operating temperature range.

The output capacitor can be an Ultra-Low-ESR ceramic chip capacitor or a low ESR bulk capacitor like a solid tantalum, POSCap or aluminum electrolytic capacitor.

$C_{OUT}$  is used to improve the output stability and reduces the changes of the output voltage during load transitions. The slew rate of the current sensed via the FB pin in AP7176B is reduced. If the application has large load variations, it is recommended to utilize low-ESR bulk capacitors.

It is recommended to place ceramic capacitors as close as possible to the load and the ground pin and care should be taken to reduce the impedance in the layout.

### Input Capacitor

To prevent the input voltage from dropping during load steps it is recommended to utilize an input capacitor ( $C_{IN}$ ). As with the output capacitor the following are acceptable, Ultra-Low-ESR ceramic chip capacitor or low ESR bulk capacitor like a solid tantalum, POSCap or aluminum electrolytic capacitor. Typically, it is recommended to utilize a capacitance of at least  $10\mu\text{F}$  to avoid output voltage drop due to reduced input voltage. The value can be lower if  $V_{IN}$  changes are not critical for the application.

## Layout Consideration

For good ground loop and stability, the input and output capacitors should be located close to the input, output, and ground pins of the device. No other application circuit is connected within the loop. Avoid using vias within ground loop. If vias must be used, multiple vias should be used to reduce via inductance.

The regulator ground pin should be connected to the external circuit ground to reduce voltage drop caused by trace impedance. Ground plane is generally used to reduce trace impedance.

Wide trace should be used for large current paths from  $V_{IN}$  to  $V_{OUT}$ , and load circuit.

Place the  $R_1$ ,  $R_2$ , and  $C_1$  (optional) near the LDO as close as possible to avoid noise coupling.

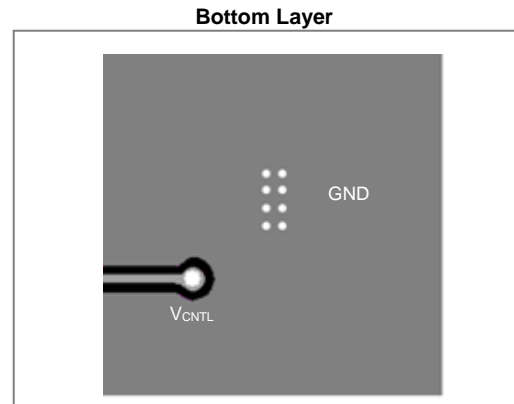
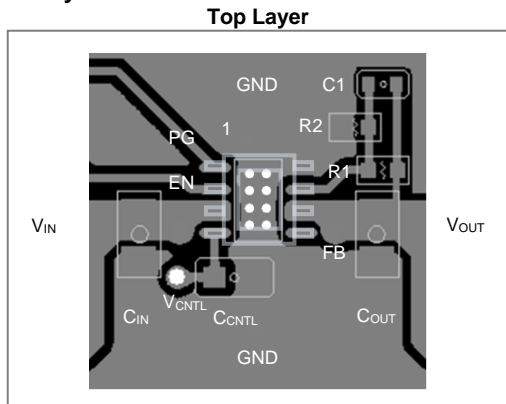
$R_2$  is placed close to device ground. Connect the ground of the  $R_2$  to the GND pin by using a dedicated trace.

Connect the pin of the  $R_1$  directly to the load for Kelvin sensing.

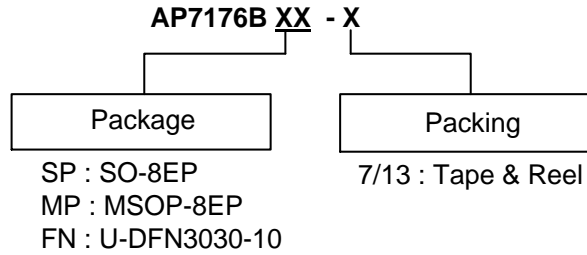
No high current should flow through the ground trace of feedback loop and affect reference voltage stability.

For the packages with exposed pads, heat sinking is accomplished using the heat spreading capability of the PCB and its copper traces. Suitable PCB area on the top layer and thermal vias (0.3mm drill size with 1mm spacing, 4 to 8 vias at least) to the  $V_{IN}$  power plane can help to reduce device temperature greatly.

### Reference Layout Plots:



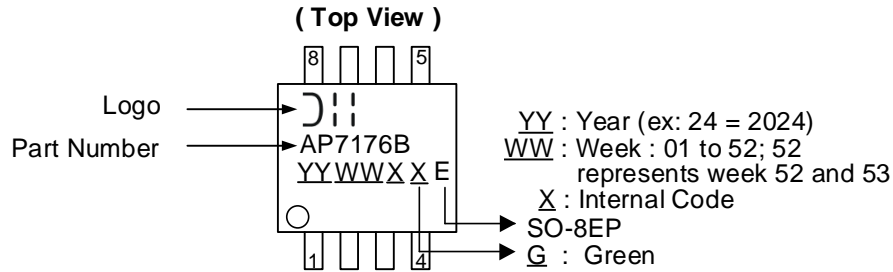
## Ordering Information



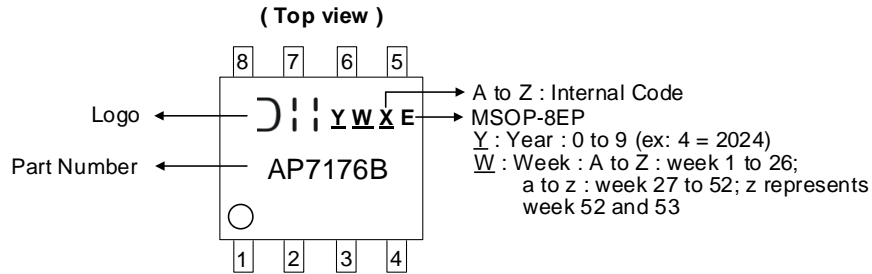
Orderable Part Number	Package Code	Package	Packing	
			Qty.	Carrier
AP7176BSP-13	SP	SO-8EP	2500	Tape & Reel
AP7176BMP-13	MP	MSOP-8EP	2500	Tape & Reel
AP7176BFN-7	FN	U-DFN3030-10	3000	Tape & Reel
AP7176BFN-13	FN	U-DFN3030-10	3000	Tape & Reel

## Marking Information

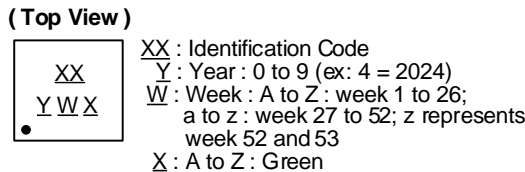
(1) SO-8EP



(2) MSOP-8EP



(3) U-DFN3030-10

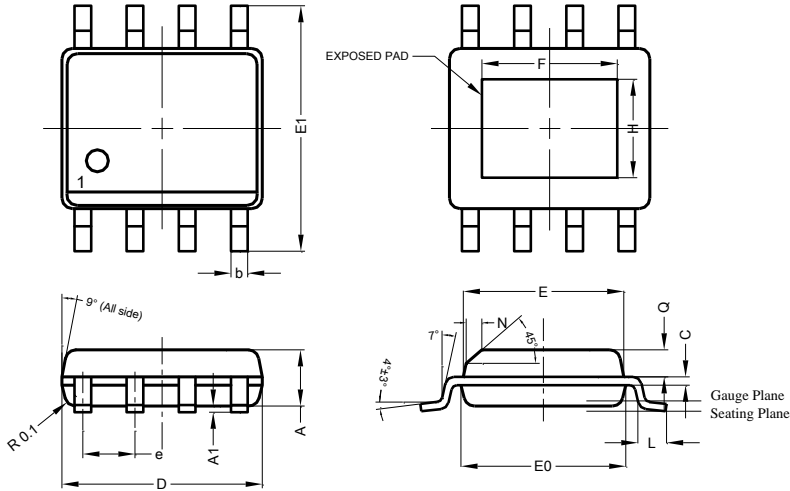


Orderable Part Number	Package	Identification Code
AP7176BFN-7	U-DFN3030-10	A7
AP7176BFN-13	U-DFN3030-10	A7

**Package Outline Dimensions**

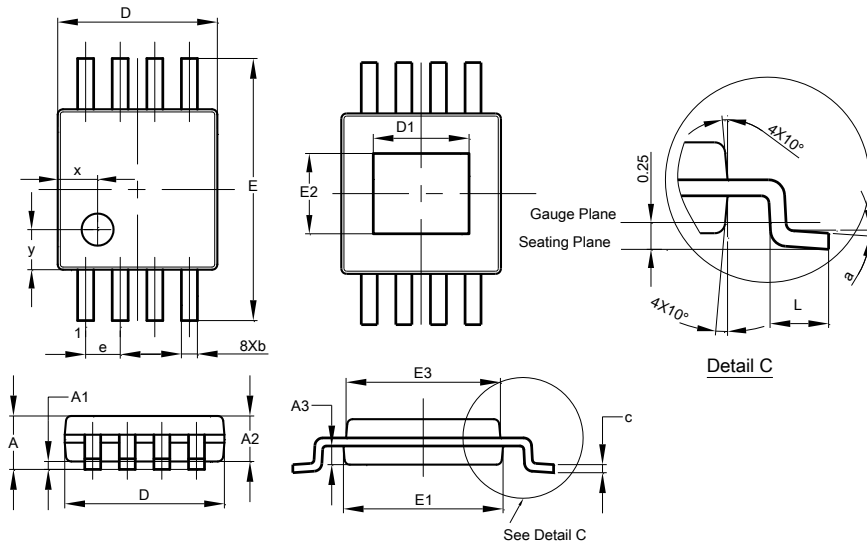
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**SO-8EP**



SO-8EP			
Dim	Min	Max	Typ
A	1.40	1.50	1.45
A1	0.00	0.13	-
b	0.30	0.50	0.40
C	0.15	0.25	0.20
D	4.85	4.95	4.90
E	3.80	3.90	3.85
E0	3.85	3.95	3.90
E1	5.90	6.10	6.00
e	-	-	1.27
F	2.75	3.35	3.05
H	2.11	2.71	2.41
L	0.62	0.82	0.72
N	-	-	0.35
Q	0.60	0.70	0.65
<b>All Dimensions in mm</b>			

**MSOP-8EP**

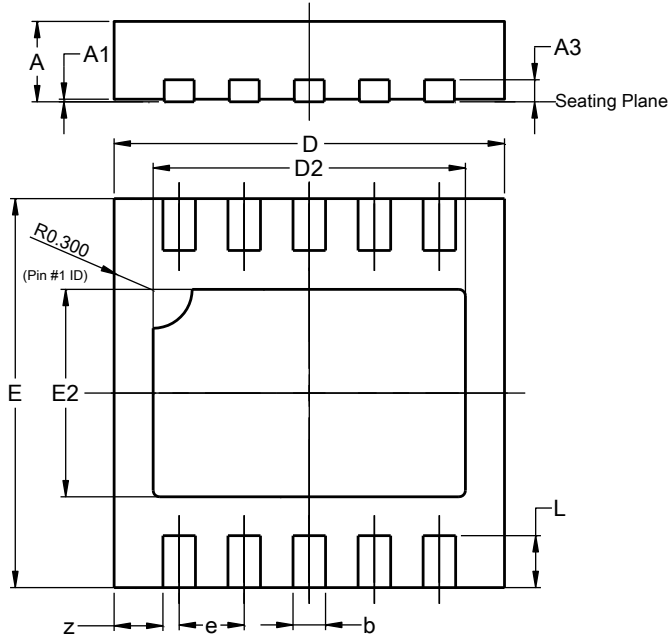


MSOP-8EP			
Dim	Min	Max	Typ
A	-	1.10	-
A1	0.05	0.15	0.10
A2	0.75	0.95	0.86
A3	0.29	0.49	0.39
b	0.22	0.38	0.30
c	0.08	0.23	0.15
D	2.90	3.10	3.00
D1	1.60	2.00	1.80
E	4.70	5.10	4.90
E1	2.90	3.10	3.00
E2	1.30	1.70	1.50
E3	2.85	3.05	2.95
e	-	-	0.65
L	0.40	0.80	0.60
a	0°	8°	4°
x	-	-	0.750
y	-	-	0.750
<b>All Dimensions in mm</b>			

**Package Outline Dimensions** (continued)

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**U-DFN3030-10**

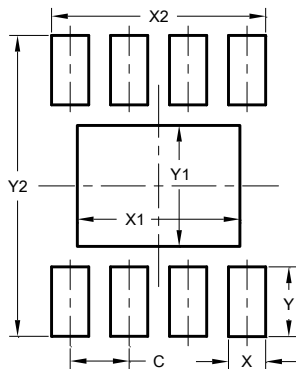


U-DFN3030-10			
Dim	Min	Max	Typ
A	0.57	0.63	0.60
A1	0.00	0.05	0.02
A3	—	—	0.15
b	0.20	0.30	0.25
D	2.90	3.10	3.00
D2	2.30	2.50	2.40
E	2.90	3.10	3.00
E2	1.50	1.70	1.60
e	--	--	0.50
L	0.25	0.55	0.40
z	—	—	0.375
All Dimensions in mm			

**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**SO-8EP**

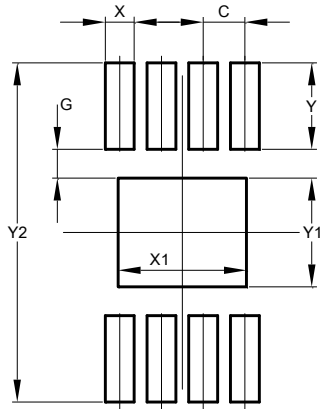


Dimensions	Value (in mm)
C	1.270
X	0.802
X1	3.502
X2	4.612
Y	1.505
Y1	2.613
Y2	6.500

**Suggested Pad Layout** (continued)

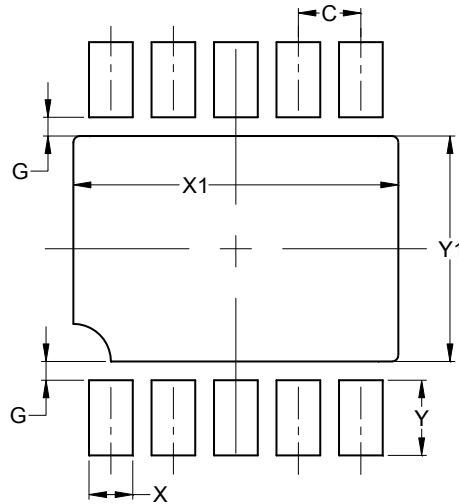
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**MSOP-8EP**



Dimensions	Value (in mm)
C	0.650
G	0.450
X	0.450
X1	2.000
Y	1.350
Y1	1.700
Y2	5.300

**U-DFN3030-10**



Dimensions	Value (in mm)
C	0.50
G	0.15
X	0.35
X1	2.60
Y	0.60
Y1	1.80

**Mechanical Data**

- Moisture Sensitivity: Level 1 Per J-STD-020
- Terminals:
  - SO-8EP/MSOP-8EP: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 ③
  - U-DFN3030-10: Finish – NiPdAu over Copper Leads, Solderable per MIL-STD-202, Method 208 ④
- Weight:
  - SO-8EP: 0.081 grams (Approximate)
  - MSOP-8EP: 0.026 grams (Approximate)
  - U-DFN3030-10: 0.01 grams (Approximate)

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