Typical Performance Characteristics (Continued)

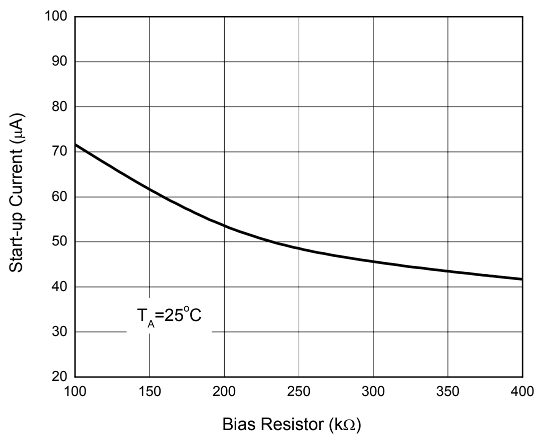

Figure 8. Start-up Current vs. Bias Resistor

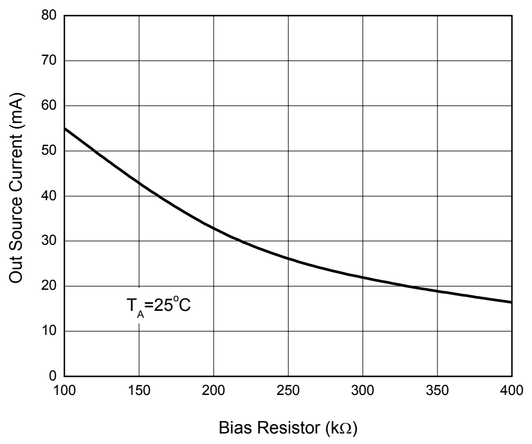

Figure 9. OUT Source Current vs. Bias Resistor

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Operation Description

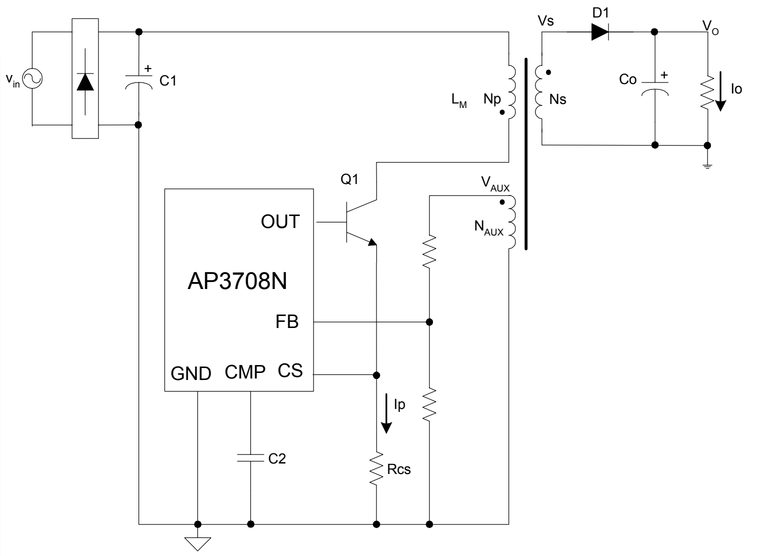

Figure 10. Simplified Flyback Converter Controlled by AP3708N

Figure 10 illustrates a simplified flyback converter controlled by AP3708N.

Constant Primary Peak Current

The primary current ip(t) is sensed by a current sense resistor R_{CS} as shown in Figure 10.

The current rises up linearly at a rate of:

$$\frac{dip(t)}{dt} = \frac{vg(t)}{L_M} \quad ......(1)$$

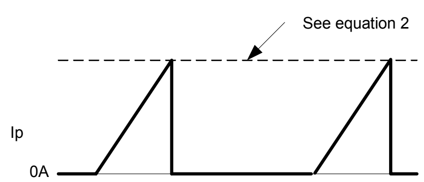

Figure 11. Primary Current Waveform

As illustrated in Figure 11, when the current ip(t) rises up to Ipk, the switch Q1 turns off. The constant peak current is given by:

$$Ipk = \frac{Vcs}{Rcs} \quad ......(2)$$

The energy stored in the magnetizing inductance L_M each cycle is therefore:

$$Eg = \frac{1}{2} \times L_M \times Ipk^2 \quad ......(3)$$

So the power transferring from the input to the output is given by:

$$P = \frac{1}{2} \times L_M \times Ipk^2 \times f_{SW} \quad ......(4)$$

where f_{SW} is the switching frequency. When the peak current Ipk is constant, the output power depends on the switching frequency f_{SW}.

Constant Voltage Operation

The AP3708N captures the auxiliary winding feedback voltage at FB pin and operates in constant-voltage (CV) mode to regulate the output voltage. Assuming the secondary winding is master, the auxiliary winding is slave during the D1 on-time. The auxiliary voltage is given by:

$$V_{AUX} = \frac{N_{AUX}}{N_S} \times (Vo + Vd) \quad ......(5)$$

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Operation Description (Continued)

where Vd is the diode forward drop voltage.

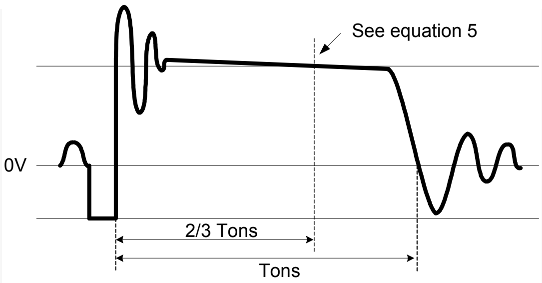

Figure 12. Auxiliary Voltage Waveform

The output voltage is different from the secondary voltage in a diode forward drop voltage that depends on the current. If the secondary voltage is always detected at a fixed secondary current, the difference between the output voltage and the secondary voltage will be a fixed Vd. The voltage detection point is at two-thirds of the D1 on-time. The CV loop control function of AP3708N then generates a D1 off-time to regulate the output voltage.

Constant Current Operation

Figure 13 shows the secondary current waveforms.

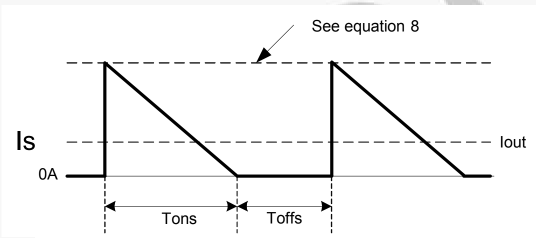

Figure 13. Secondary Current Waveform

In CC operation, the CC loop control function of AP3708N will keep a fixed proportion between D1 on-time Tons and D1 off-time Toffs by discharging or charging the capacitance connected in CMP pin. The fixed proportion is

$$\frac{Tons}{Toffs}=\frac{4}{3} \quad \text{......(6)}$$

The relationship between the output constant-current and secondary peak current Ipks is given by:

$$Iout=\frac{1}{2}\times Ipks\times\frac{Tons}{Tons+Toffs} \quad \text{......(7)}$$

At the instant of D1 turn-on, the primary current transfers to the secondary at an amplitude of:

$$Ipks=\frac{N_P}{N_S}\times Ipk \quad \text{......(8)}$$

Thus the output constant-current is given by:

$$Iout=\frac{1}{2}\times\frac{N_P}{N_S}\times Ipk\times\frac{Tons}{Tons+Toffs}=\frac{2}{7}\times\frac{N_P}{N_S}\times Ipk \quad \text{......(9)}$$

Leading Edge Blanking

When the power switch is turned on, a turn-on spike will occur on the sense-resistor. To avoid false-termination of the switching pulse, a 430ns leading-edge blanking is built in. During this blanking period, the current sense comparator is disabled and the gate driver can not be switched off.

CCM Protection

The AP3708N is designed to operate in discontinuous conduction mode (DCM) in both CV and CC modes. To avoid operating in continuous conduction mode (CCM), the AP3708N detects the falling edge of the FB input voltage on each cycle. If a 0.1V falling edge of FB is not detected, the AP3708N will stop switching.

OVP & OCkP

The AP3708N includes output over-voltage protection (OVP) and open circuit protection (OCkP) circuitry as shown in Figure 14. If the voltage at FB pin exceeds 8V, 100% above the normal detection voltage, or the -0.7V falling edge of the FB input can not be monitored, the AP3708N will immediately shut off and enter hiccup mode. The AP3708N sends out a fault detection pulse every 32ms in hiccup mode until the fault has been removed.

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Operation Description (Continued)

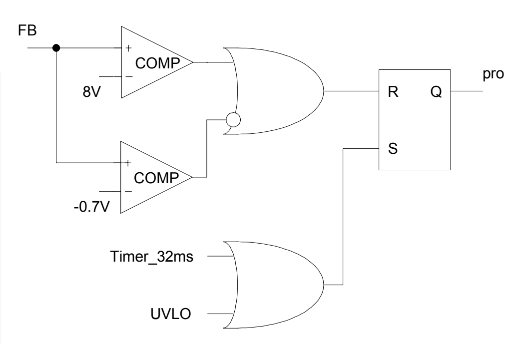

Figure 14. OVP and OCkP Function Block

Output Cable Compensation

The AP3708N integrates the output cable compensation circuitry as shown in Figure 15. Tons shows the variation for FB flyback voltage. Tons can be converted to a DC voltage by a low-pass filter. When system load current Iout changed from open load to full load Iload, The amplified voltage Vout1 through a rail-to-rail operation amplifier is obtained:

$$V_{OUT1} = (1 + \frac{RB}{RA}) \times 3.65V - \frac{RB}{RA} \times V_{CMP} \qquad ......(10)$$

Through the internal RA and RB, the FB voltage can be compensated by the Vout1, the compensation voltage is 0.4V when full load switch frequency is 60kHz.

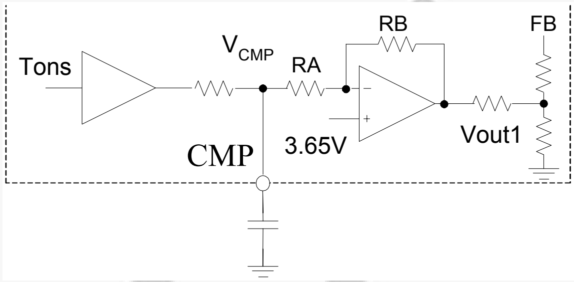

Figure 15. Output Cable Compensation Function Block

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Typical Application

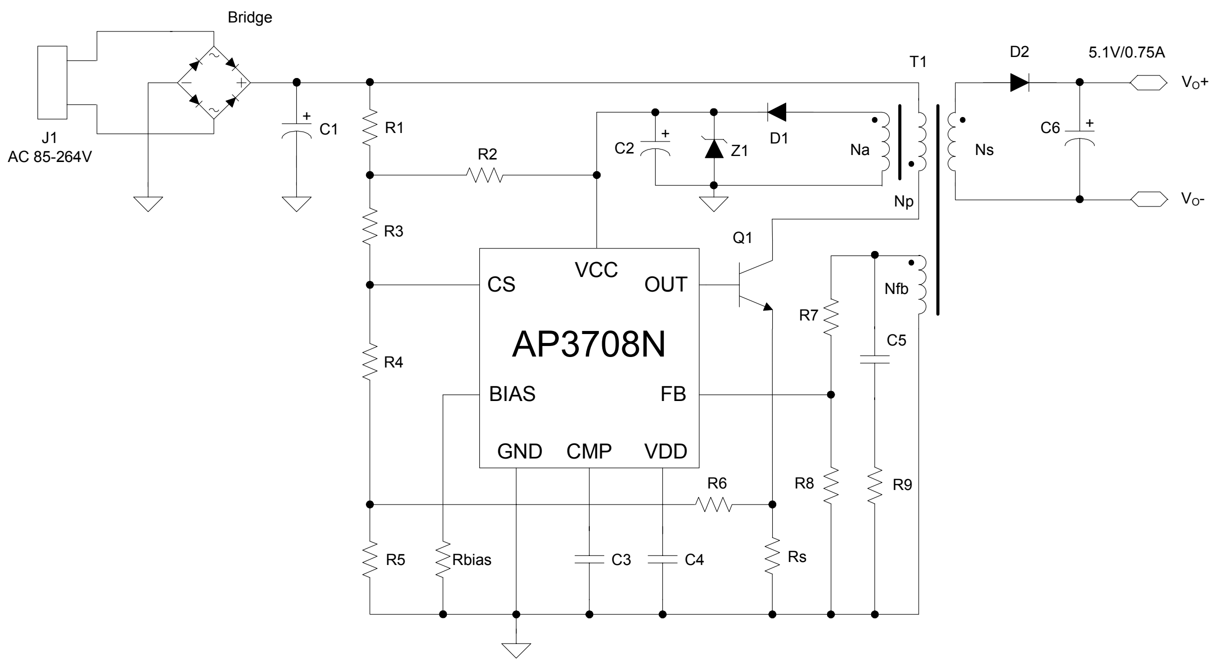

Figure 16. 5V/1A Output for Battery Charger of Mobile Phone

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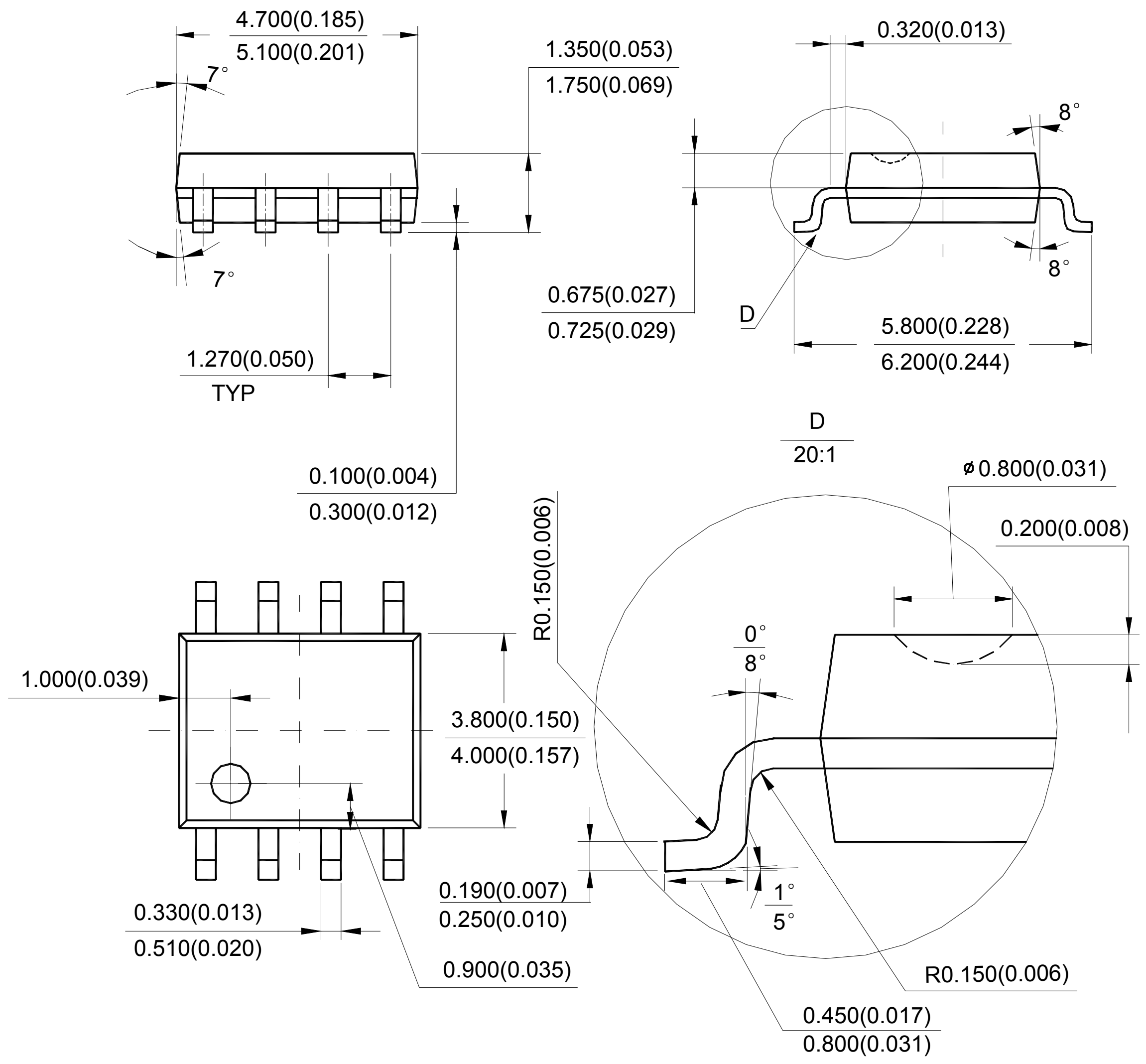
Mechanical Dimensions

SOIC-8 **Unit: mm(inch)**



Note: Eject hole, oriented hole and mold mark is optional.

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