Description

The AP33772S is a highly integrated USB Type-C® PD3.1 sink controller to support Extended Power Range (EPR) / Adjustable Voltage Supply (AVS) up to 28V and Standard Power Range (SPR) / Programmable Power Supply (PPS) up to 21V. The device is targeted for DC power request and control for flexible Type-C Connector-equipped Devices (TCDs) with an embedded host MCU (Micro Controller Unit) and I2C interface pins (SCL, SDA).

Through the I2C interface interaction and interrupt mechanism, the host MCU sets up proper desired power profile with relevant threshold parameters and delegates PD negotiation tasks to the AP33772S. The host MCU further inquiries about status of various I2C registers for intended applications.

Based on high-voltage process, the AP33772S offers short-protection between CC1/CC2 pins to adjacent high-voltage pin up to 34V. Smart built-in firmware of the AP33772S offers comprehensive safety protection scheme, including over-voltage protection (OVP), under-voltage protection (UVP), over-current protection (OCP), and moisture detection between DP and DN pins. In addition, over-temperature protection (OTP) and thermal de-rating are supported by an external NTC resistor.

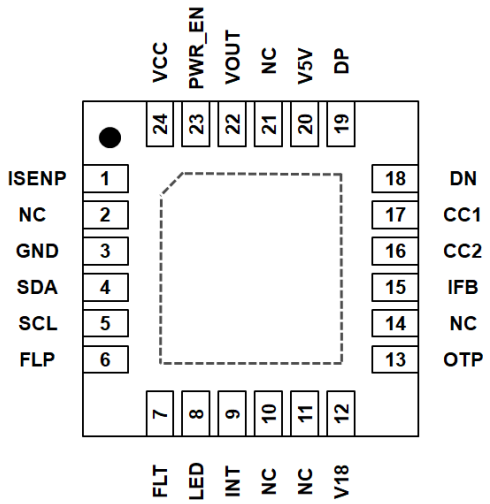
An LED indicator is used to show the PD power negotiation status, and the automatic cable voltage drop compensation for a long cable is implemented to cover practical usage situations.

Features

- USB PD3.1 v1.6 Certified with TID: 10062
- Operating Voltage Range of VCC: 3V to 31V
- Support PD3.1 EPR/AVS Up to 28V and SPR/PPS Up to 21V
- Support OVP with Hard Reset and Auto Restart
- Support UVP and OCP with Output Power Shut Down
- Support OTP and Thermal De-Rating Through NTC Resistor
- VBUS Short Protection on CC1/CC2 Pins Up to 34V
- I2C Commands for External MCU Monitoring, Control, and Parameter Programming
- Dedicated Pins for CC Flip Indication and Interrupt Request
- Dedicated Pins for Direct FAULT Control of VBUS MOS Switch
- Moisture Detection between DP and DN
- LED Indication for Different Negotiation Results
- Driver for Output Enable N-MOS Switch
- Support Dead Battery Function
- Automatic Cable Voltage Drop Compensation
- Support Legacy Type-A Charger with Type-A to Type-C Cable
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Pin Assignments

(Top View)



W-QFN4040-24 (Type A1)

Applications

- USB Type-C connector-equipped battery-powered devices
- USB Type-C connector-equipped DC-power input devices
- USB PD3.1 testers

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Application Circuit

The AP33772S is a USB Type-C power delivery sink controller used to request power for a typical TCD embedded with a host MCU from an attached USB PD charger, as shown in the Figure 1 below.

Once the cable attachment is completed, the AP33772S is powered from VCC pin, and starts to do power-on initiation by setting up its internal registers and receiving the TCD configuration parameters from the external host MCU via I2C interface. After the power-on initialization, the AP33772S starts to decode USB PD commands from CC pin, and gets the PD source capability. The host MCU makes a choice of the source PDOs, and sends this requested PDO to the AP33772S through I2C command.

The AP33772S then automatically initiates the PD negotiation progress with the attached Type-C PD compliance charger (through Type-C to Type-C cable) or legacy Type-A charger (through Type-A to Type-C cable). If the PDO is matched, the MOS switch is turned on to connect VBUS to VOUT, and then the source adapter successfully provides power to the AP33772S-embedded TCD device.

The AP33772S supports the dead battery function, and can be woken up as soon as an active PD adapter is plugged in the TCD Type-C receptacle. After the power link is set up between source and sink, OVP, UVP, OCP, and OTP protections are enabled to monitor the power charging status. In case power protection is triggered, the AP33772S shuts down the VOUT enable NMOS switch, and the host MCU will need to load new PD_REQMSG to start a PDO negotiation process to resume charging operation.

The back-to-back N-MOS switches shown in Figure 1 could be simplified to a simple N-MOS switch for the TCD when there is no concern on reverse current from power module back to VBUS.

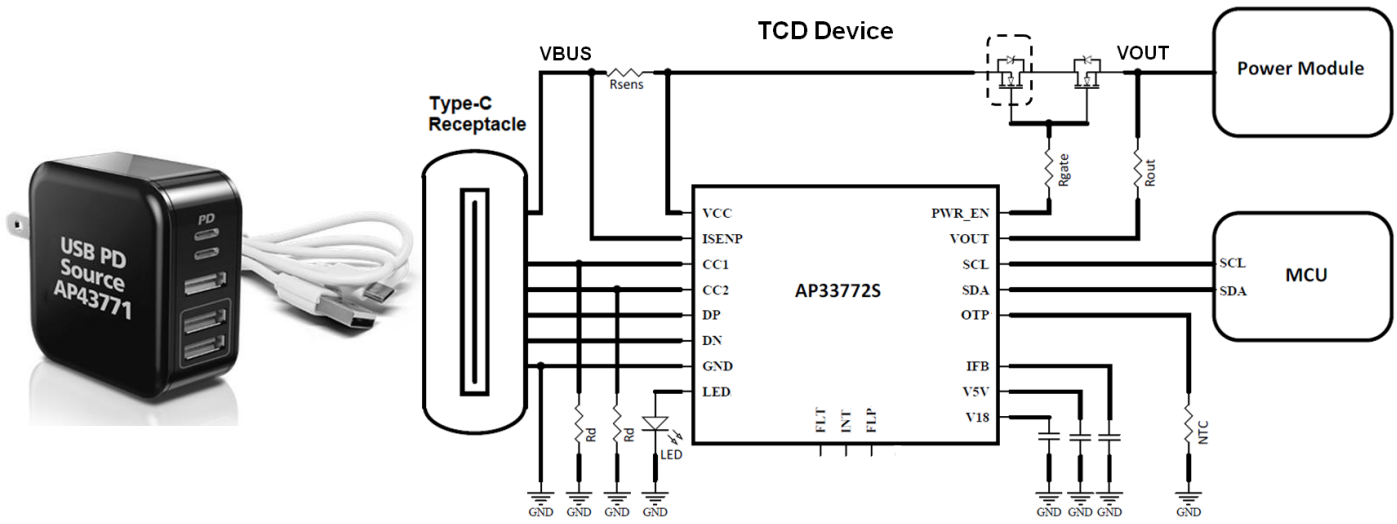


Figure 1. Typical System Configuration of AP33772S PD3.1 Sink Controller in a TCD

Pin Descriptions

Pin No.	Pin Name	Type (Note 4)	Pin Function
1	ISENP	AHV	Current sense positive node
2	NC	—	No connection
3	GND	GND	Ground
4	SDA	DIO	I2C Data
5	SCL	DIO	I2C Clock
6	FLP	DO	Flip indicator of Type-C plug. LOW: CC1 detected. HIGH: CC2 detected
7	FLT	DI	VBUS MOS switch control input. HIGH: VOUT is disconnected from VBUS. LOW: normal
8	LED	DO	LED indicator pin
9	INT	DO	Interrupt pin is used to inform external MCU. LOW: normal. HIGH: interrupt happened.
10	NC	—	No connection
11	NC	—	No connection
12	V18	DP	1.8V LDO output for internal use, need to connect a 100nF cap to GND. This pin cannot drive external load.
13	OTP	AIO	100μA current source is output. An NTC resistor is used to monitor temperature variation.
14	NC	—	No connection.
15	IFB	AI	For current measurement, a 100nF cap to Ground is suggested.
16	CC2	AIO	Type-C configuration channel 2 (CC2)
17	CC1	AIO	Type-C configuration channel 1 (CC1)
18	DN	AIO	DN of Type-C connector
19	DP	AIO	DP of Type-C connector
20	V5V	AP	5V LDO output if VCC is on. A 1μF cap is required to connect this pin to GND. Alternative 5V power input for internal 5V core circuit if VCC is off.
21	NC	—	No connection
22	VOUT	AHV	Terminal for VOUT monitoring
23	PWR_EN	AHV	To control external NMOS switch ON (High) or OFF (Low).
24	VCC	AHV	The power supply of the IC. A 1μF cap is required to connect this pin to GND pin.
—	EPAD	GND	Exposed pad is suggested to connect to Ground

Table 1. Pin Descriptions of AP33772S Sink Controller

Note 4:

AHV – Analog High Voltage pin.
AP – Power for Analog Circuit and Analog I/O pins, 5.0V operation.
AI – Analog Input pin.
DP – Power for Digital Circuit operation.
AIO – Analog Input/Output pin with 5.0V operation. However, DP/DN & CC1/CC2 pins are 3.3V operation.
DI – Digital Input pin. All are 5.0V operation.
DO – Digital Output pin. All are 5.0V operation.
DIO – Digital Input/Output pin. All are 5.0V operation.

Functional Block Diagram

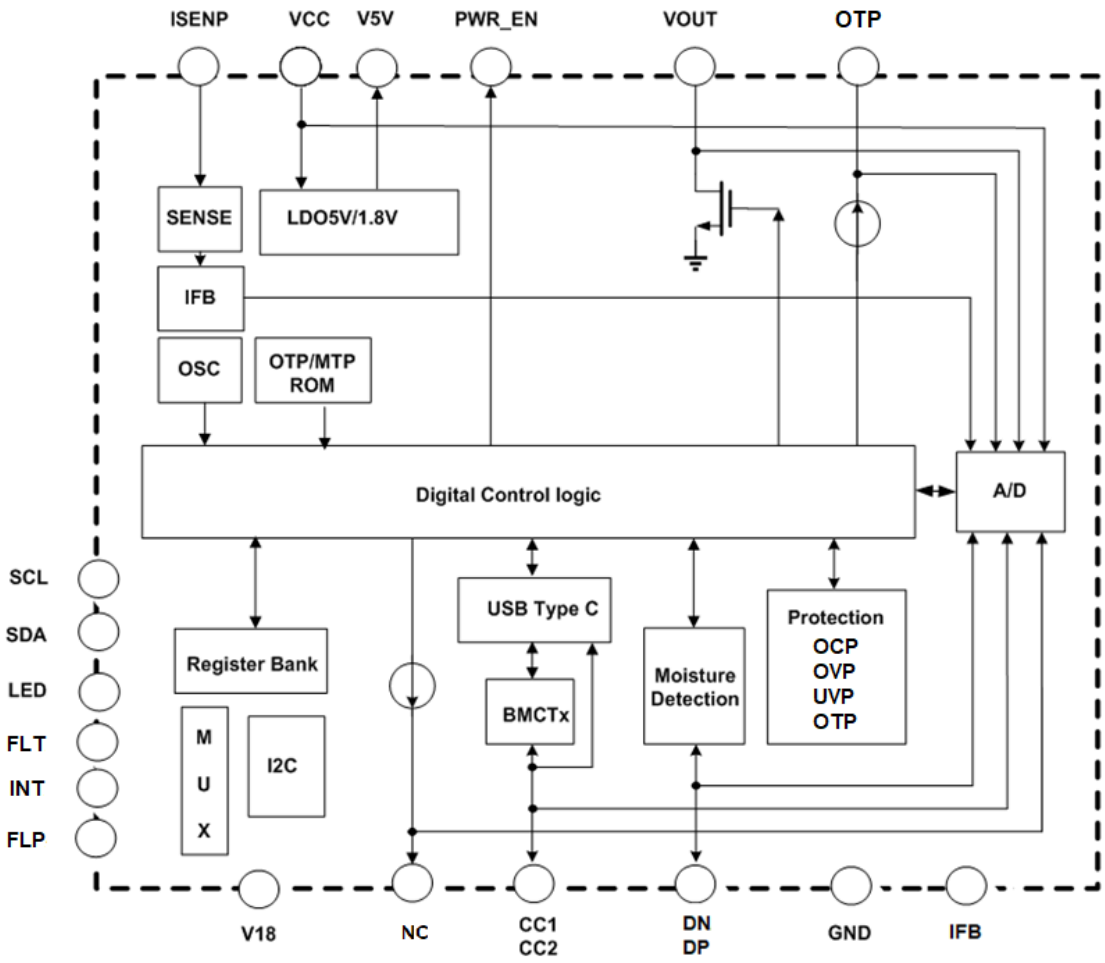


Figure 2. The Functional Block Diagram of AP33772S PD3.1 Sink Controller

Absolute Maximum Ratings (Note 5)

Symbol	Parameter	Rating	Unit
V_{VCC}	Input Voltage at VCC Pin	-0.3 to 34	V
V_{V5V}	Input Voltage at V5V Pin	-0.3 to 7	V
V_{V18}	Input Voltage at V18 Pin	-0.3 to 5	V
V_{FLT}, V_{FLP}, V_{INT}, V_{OTP}, V_{LED}	Input Voltage at FLT, FLP, INT, OTP, LED Pins	-0.3 to 7	V
V_{VOUT}, V_{ISENP}	Input Voltage at VOUT, ISENP Pins	-0.3 to 31	V
V_{PWR_EN}	Input Voltage at PWR_EN Pin	-0.3 to 38	V
—	Voltage from PWR_EN to VCC Pin	-16 to 4	V
V_{CC1}, V_{CC2}	Input Voltage at CC1, CC2 Pins	-0.3 to 34	V
V_{DP}, V_{DN}	Input Voltage at DP, DN Pins	-0.3 to 7	V
V_{SCL}, V_{SDA}	Input Voltage at SCL, SDA Pins	-0.3 to 7	V
T_J	Operating Junction Temperature	-40 to +150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{LEAD}	Lead Temperature (Soldering, 10s)	+300	°C
θ_{JA}	Thermal Resistance (Junction to Ambient) (Note 6)	28	°C/W
θ_{JC}	Thermal Resistance (Junction to Case) (Note 6)	16	°C/W
ESD	Human Body Model	2	kV
ESD	Charged Device Model	750	V

Notes: 5. Stresses greater than those listed under "*Absolute Maximum Ratings*" can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "*Recommended Operating Conditions*" is not implied. Exposure to "*Absolute Maximum Ratings*" for extended periods can affect device reliability.
6. Test condition: Device mounted on FR-4 substrate PC board, 2oz copper, with the minimum footprint.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{VCC}	Power Supply Voltage at VCC Pin	3.3	31	V
V_{V5V}	Input Voltage at V5V Pin	4.37	5.33	V
V_{DP}, V_{DN}	Input Voltage at DP, DN Pins	2.75	3.25	V
V_{SCL}, V_{SDA}	Input Voltage at SCL, SDA Pins	4.37	5.33	V
T_J	Operating Junction Temperature Range	-40	+125	°C

Electrical Characteristics (@ T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCC SECTION						
V_{ST}	Startup Voltage	—	2.5	2.8	3.5	V
V_{UVLO}	Minimum Operating Voltage	—	2.3	2.7	3	V
V_{VCC_HYS}	VCC Hysteresis (V_{ST}-V_{UVLO})	—	0.05	—	—	V
I_{VCC_OPR}	Operating Supply Current	V_{VCC} = 5V	—	3.3	6	mA
CC1/CC2 SECTION						
V_{L_RD3A}	Low Voltage Threshold Used to Distinguish R_D Attached or Detached for 3A Delivery	—	—	1.35	—	V
V_{H_RD3A}	High Voltage Threshold Used to Distinguish R_D Attached or Detached for 3A Delivery	—	—	2.0	—	V
CURRENT SOURCE SECTION						
I_{OTP}	OTP Current Source (Note 8)	—	—	100	—	μA
I_{OTP_Range}	OTP Current Source Range (Note 8)	—	-8	—	+8	%
FLT, FLP, INT, OTP, LED, and I2C SECTION						
V_{GPIOO}	FLT, FLP, INT, OTP, LED Pins Output Voltage Range (Note 8)	V_{VCC} = 5V	4.37	4.85	5.33	V
V_{GPIOI_HI}	FLT, FLP, INT, OTP, LED Pins Input High Voltage (Note 8)	V_{VCC} = 5V	1.4	—	—	V
V_{GPIOI_LO}	FLT, FLP, INT, OTP, LED Pins Input Low Voltage (Note 8)	V_{VCC} = 5V	—	—	0.4	V
I_{GPIO}	FLT, FLP, INT, OTP, LED Pins Sink/Source Capability (Note 8)	—	2	—	—	mA
V_{I2CO}	SDA, SCL Power Supply Range (Note 8)	V_{VCC} = 5V		4.85		V
V_{I2C_HI}	SDA, SCL Input Low Voltage (Note 8)	V_{CC} = 5V	1.4	—	—	V
V_{I2C_LO}	SDA, SCL Input Low Voltage (Note 8)	V_{CC} = 5V	—	—	0.4	V
F_{SCL}	SCL Clock Frequency (Note 8)	—	—	—	400	kHz
PROTECTION FUNCTION SECTION						
V_{OVP5V}	OVP_5V Enable Voltage (Notes 7, 8)	—	—	7	—	V
V_{OVP20V}	OVP_20V Enable Voltage (Notes 7, 8)	—	—	22	—	V
V_{OVP28V}	OVP_28V Enable Voltage (Notes 7, 8)	—	—	31	—	V
$t_{DEBOUNCE\_OVP}$	OVP Debounce Time (Note 9)	—	—	90	—	ms
t_{OV_DELAY}	Delay from OVP Threshold Trip to NMOS Gate Turn-Off (Note 8)	—	—	—	50	ms
T_{OTP}	Internal OTP Temperature	—	—	135	—	°C
T_{OTP_HYS}	OTP Hysteresis	—	—	10	—	°C
V5V SECTION						
V_{V5V}	V5V Output Range	—	4.37	4.85	5.33	V
I_{V5V}	V5V Source Capability	—	—	30	—	mA
ADC SECTION						
V_{FS}	Full Swing Range	—	—	2.048	—	V
—	Resolution	—	—	8	—	Bit
—	DNL	—	—	1	—	LSB

Notes: 7. 110% OVP setting @PDO > 18V. PDO+2V OVP setting @PDO ≤ 18V.
8. Guaranteed by design.
9. OVP blanking time during V_O transition from high output voltage to low output voltage, such as 9V to 5V, or 12V to 5V.

Functional Description

Overview

The AP33772S, a highly integrated USB Type-C PD3.1 sink controller, supports EPR/AVS up to 28V and provides SPR/PPS up to 21V. The device is targeted for DC power request and control for flexible Type-C Connector-equipped Devices (TCDs) with an embedded host MCU (Micro Controller Unit) and I2C interface pins (SCL, SDA).

Cable Attachment and Power On Initialization

After plugging the cable from a powered PD source adapter into the AP33772S-equipped TCD device, both Rds are connected to the Configuration Channel pins (CC1/CC2). According to the definition of Type-C, only one of the Rds can be pull down, and then the CC/VCONN configuration and flip polarity are established. Once the cable attachment is completed, the source adapter enables VBUS with 5V, and starts VCONN power supply to enable cable e-Marker for cable information detection. As soon as the flow is completed, the PD source adapter starts broadcasting PD source capabilities to the PD sink through CC pin, which is connected to the AP33772S internal Bi-phase Mark Code (BMC) block.

Meanwhile, the AP33772S starts to do power on initiation as soon as its VCC pin is powered from the 5V VBUS. After its internal MCU default configuration and registers are set up, the AP33772S will play as a I2C slave device and wait for the external host MCU to load the TCD configuration parameters to the internal I2C registers of the AP33772S, and then to update the AP33772S internal configuration accordingly.

During the negotiation, the source capabilities are stored in the AP33772S internal registers, and waiting for the reading from the external MCU through I2C interface. A total of 13 PDO registers are used to store the source capabilities of PD adapter, including 7 for SPR and 6 for EPR as Figure 3 below.

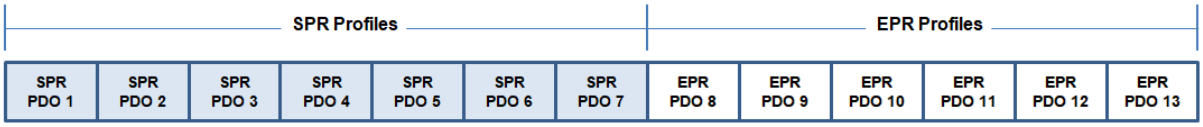


Figure 3. A Total of 13 PDO Registers Are Used to Store the Source Capabilities of PD Adapter

Once the source capability is received, the AP33772S will reply with a CRC good command and first request a default 5V from the source adapter. The AP33772S is now powered by the 5V profile from the source adapter, and waiting for host MCU to deliver requests for a new PDO power profile or other control commands through the I2C interface.

I2C Interface and Control

I2C interface (SCL, SDA pins) and INT pin are used as the communication channels between the AP33772S and the host MCU of the TCD device. During the power on initialization, the host MCU needs to deliver the system configuration parameters to the AP33772S for its internal set up. After the system set up, the host MCU can timely update the power profiles from the source adapter capability. Meanwhile, the system MCU can monitor the AP33772S internal registers and then give a control of the system operation through I2C commands accordingly.

All of the I2C commands used in the AP33772S are summarized in Table 18. The functions include:

1. PDO information getting and New PDO request (i.e. Table 2, 3)
2. Protection threshold setting (i.e. Table 4, 5, 6, 7, 8)
3. System configuration setting (i.e. Table 3, 9, 10)
4. System data acquisition
5. System status inquiry (i.e. Table 11, 12, 13)
6. Cable compensation and legacy support (i.e. Table 14, 15, 16)

Source PDO Information Getting

Before selecting a new PDO profile, the host MCU should get the total PDO register information that has been placed in the AP33772S I2C registers through the I2C read commands. The AP33772S provides a 26-byte I2C command SRCPDO (0x20), which can read all the 13 PDOs at one time. In addition, there are 13 commands provided for host MCU to read each PDO information individually, where SRC_SPR_PDO1 (0x21) ~ SRC_SPR_PDO7 (0x27) and SRC_EPR_PDO8 (0x28) ~ SRC_EPR_PDO13 (0x2D) are used for SPR PDOs and EPR PDOs respectively.

The AP33772S will echo each PDO read command with a 2-byte data which include the PDO type (SPR, EPR, Fixed, PPS, AVS), voltage range (minimum, maximum), and current maximum.

Functional Description (continued)

Request a New Source PDO

The host MCU can select a suitable PDO to fit in the system application request, and then deliver it to the AP33772S through I2C command PD_REQMSG (0x31). It is a 16-bit word used to send the request message of PDO index, Operating Current and Output Voltage settings at runtime as shown in Table 2 below, where:

1. PDO_INDEX can assign the source PDO index.
2. CURRENT_SEL can set the operating current value of RDO.
3. VOLTAGE_SEL can set the output voltage value of PPS / AVS RDO, but it has no meaning for selecting fixed PDO.

PD_REQMSG	Bit	Attribute	Pwr-On	Description
PDO_INDEX	12:15	WO	0h	[0001] to [0111] : For SPR PDO1 to PDO7, [1000] to [1101] : For EPR PDO8 to PDO13, if its corresponding PDO is detected. Others = Reserved
CURRENT_SEL	8:11	WO	0h	Operating Current Select [0000] to [1111] = 1.00A to 5.00A
VOLTAGE_SEL	0:7	WO	0h	VOLTAGE_SEL has no meaning for Fixed PDO selected If set B[15] = 0 (select SPR) : output voltage in 100mV/unit for PPS APDO selected If set B[15] = 1 (select EPR) : output voltage in 200mV/unit for AVS APDO selected

Table 2. The I2C Command PD_REQMSG (0x31) Is Used to Refresh Existing Sink RDO

After the AP33772S receiving PD_REQMSG command, it will generate a new RDO of voltage and current and then starts to negotiate with PD source. Once the negotiation is completed, both the registers of STATUS and PD_MSGRLT are updated accordingly.

Meanwhile, the AP33772S also provides a simple command to request Maximum current and Maximum voltage of the selected source PDO by setting only the PDO_INDEX to the desired source PDO and keep CURRENT_SEL = 0xF and VOLTAGE_SEL = 0xFF.

For example, if source PDO3 is valid then the host MCU can write PD_REQMSG with 0x3FFF, and the AP33772S will request the Maximum current and Maximum voltage of source PDO3.

Support EPR / AVS

After the first negotiation with PD source which supports EPR Mode, the AP33772S will try to enter EPR Mode when PDCONFIG (0x05) is set to 1 at EPR_MODE bit, as Table 3 below. If successfully entering EPR Mode, the AP33772S stores the EPR Source Capability in SRC_EPR_PDOx registers (0x28 to 0x2D) and enables EPR request.

PDCONFIG	Bit	Attribute	Pwr-On	Description
—	7:4	RW	0h	Reserved
—	3	RW	0h	Reserved
—	2	RW	0h	Reserved
PPS_AVS_EN	1	RW	1h	0/1 : Disable/Enable sink PPS and AVS capability
EPR_MODE_EN	0	RW	1h	0/1 : Disable/Enable EPR mode

Table 3. The I2C Command PDCONFIG (0x05) Is Used to Enable Sink EPR Mode

Integrated Power Protection

Based on high-voltage process, the AP33772S offers short-protection between CC1/CC2 pins to adjacent high-voltage pin up to 34V. In addition, the built-in firmware of the AP33772S offers comprehensive safety protection schemes, including OTP, OCP, OVP, and UVP. Besides, moisture detection between DP and DN pins is provided. When the power protection occurs, the associated VOUT MOS switch is turned off to disconnect VBUS from VOUT.

Functional Description (continued)

Over Temperature Protection (OTP) and Thermal De-rating

The host MCU could access the estimated temperature of a potential hot spot by accessing the I2C command TEMP (0x13) register. A NTC thermistor is used to connect to OTP pin and ground nearby the potential hot spot.

The I2C command OTPTHR (0x1A) register, as shown in Table 4 below, is used to set OTP threshold, and is 78h (+120°C) by default. If the TEMP value rises over the OTPTHR value after the de-bouncing time, the OTP happens, and STATUS Bit [6] is set to High. The associated output enable MOS switch will be turned off.

OTPTHR	Bit	Attribute	Pwr-On	Description
OTPTHR	7:0	RW	78h	OTP threshold, Unit: °C The temperature threshold triggers the OTP function, the default value for OTPTHR is 78h (+120°C).

Table 4. The I2C Command OTPTHR (0x1A) Is Used to Set OTP Threshold

Furthermore, the AP33772 defines I2C command DRTHR (0x1B) register, as shown in Table 5 below, as threshold temperature to trigger the power de-rating functions. If source PDO is PPS APDO, and when TEMP value rises above DRTHR after the de-bouncing time, the input current will be reduced by 50% through sending out a new RDO to negotiate with the PD source device. The AP33772 monitors the temperature at the potential hot spot continuously. After some time duration, it will recover the charging power if TEMP value is +10°C below DRTHR.

DRTHR	Bit	Attribute	Pwr-On	Description
DRTHR	7:0	RW	78h	De-Rating threshold, Unit: °C The temperature threshold triggers Power De-Rating procedure, the default value for DRTHR is 78h (+120°C).

Table 5. The I2C Command DRTHR (0x1B) Is Used to Set De-Rating Threshold

OCP Threshold Setting

The AP33772S supports OCP to control the output load condition by monitoring the output current through detection of IR drop on the 5mΩ Rsense resistor. Once the TCD device draws more current than the OCP threshold level after de-bounce time, the AP33772S enters FAULT states by turning off the VOUT MOS Switches.

Table 6 bellow shows the correspondence between OCPTHR and OCP Threshold Current, where the OCPTHR stands for $\mathbf{I_{OCPTHR}}$, OCP threshold current defined by user via I2C command OCPTHR (0x19). The user defined OCPTHR value is an 8-bit register with 50mA/LSB and 00h by default.

After successful negotiation with the PD source, if the OCPTHR value is still 00h, the OCP Threshold Current would be 110% of the I_{MAX}, maximum current of the selected PDO/APDO. If the OCPTHR value has been updated through I2C command, the OCP Threshold Current would be 110% of $\mathbf{I_{OCPTHR}}$ value.

OCPTHR	OCP Threshold Current
OCPTHR = 0	$\mathbf{I_{MAX}}$*** 110%** (Note 10)
OCPTHR ! = 0	$\mathbf{I_{OCPTHR}}$*** 110%**

Table 6. Correspondence between OCPTHR and OCP Threshold Current

Note 10: $\mathbf{I_{MAX}}$: Maximum Current of PDO/APDO.

OVP Threshold and Adjustment

The AP33772S triggers the OVP protection when VBUS voltage is higher than OVP threshold voltage. The Table 7 bellow summarizes the correspondence between V_{VREQ}, V_{OVPOS} and OVP threshold voltage, where V_{VREQ} is the voltage requested after successful power negotiation with the PD source adapter, and V_{OVPOS} is the OVP offset, programmable via I2C command OVPTHR (0x18). If VBUS voltage is higher than OVP threshold after the de-bounce time limit, the AP33772S enters the FAULT state, where the VOUT MOS Switches are turned off.

Functional Description (continued)

Mode	Criteria	OVP Threshold Voltage
SPR Mode	(V_{VREQ} + V_{OVPOS}) ≤ 20V	V_{VREQ} + V_{OVPOS}
	(V_{VREQ} + V_{OVPOS}) > 20V	V_{VREQ} * 110%
EPR Mode	(V_{VREQ} + V_{OVPOS}) ≤ 40V	V_{VREQ} + V_{OVPOS}
	(V_{VREQ} + V_{OVPOS}) > 40V	V_{VREQ} * 110%

Table 7. Correspondence between V_{VREQ}, V_{OVPOS} and OVP Threshold Voltage

UVP Threshold Adjustment

The AP33772S triggers the UVP protection when VBUS voltage is lower than UVP threshold Voltage. The Table 8 bellow shows the correspondence between under voltage protection level, UVPTHR, and UVP threshold voltage. The default value of UVPTHR is 80%, which can be modified via I2C command UVPTHR (0x17). If VBUS voltage is lower than UVP threshold after de-bounce time, the AP33772S enters FAULT states, where the VOUT MOS switches are turned off.

UVPTHR	UVP Threshold Voltage
1	V_{VREQ} * 80%
2	V_{VREQ} * 75%
3	V_{VREQ} * 70%

Table 8. Correspondence between V_{VREQ}, UVPTHR and UVP Threshold Voltage

Moisture Detection

The AP33772S supports the moisture detection through DP/DN pins. As soon as the Type-C connector is plugged in, the impedance between DN/DP pins to ground is evaluated by internal ADC digitization and firmware calculation. If the impedance level is below the pre-determined threshold, the VOUT MOS switch is turned off to disconnect VBUS from VOUT, and the LED is flickered with the “MOISTURE” pattern accordingly. If the impedance check is normal, the AP33772S starts to negotiate with the source.

VOUT Enable Switch and FAULT Control

Taking VBUS voltage as input, the built-in charge-pump circuit generates a high voltage gate driver (PWR_EN) to drive an external high-side NMOS switch. A suitable small resistance is suggested to connect the PWR_EN to the NMOS gate. Once the PDO negotiations are successful between source and sink, and the V_{VREQ}, the requested voltage, is greater than $V_{VSELMIN}$, the PWR_EN enables the NMOS switch and connects VBUS to VOUT. Otherwise, the NMOS switch will be turned off, and VBUS is disconnected from VOUT.

Meanwhile, the NMOS VOUT enable switch is also used for power protection. Whenever output overvoltage, undervoltage, overcurrent, or over temperature occurs, the AP33772S enters the FAULT state, where the VOUT MOS Switches are turned off to protect the electrical appliances from possible damage. Also, for the system flexibility, the dedicated FLT (FAULT) pin input can be pulled to logic HIGH to disconnect VOUT from VBUS directly. To escape from the latch off state, the host MCU will need to load new RDO to start a PDO negotiation process to resume charging operation.

Protection Mode Configuration

To fit the comprehensive application scenarios, the power protection modes in the AP33772S are configurable through the I2C command CONFIG (0x04) as shown in Table 9 below.

CONFIG	Bit	Attribute	Pwr-On	Description
DR_EN	7	RW	1h	0/1: Disable/enable DR (De-Rating) function
OTP_EN	6	RW	1h	0/1: Disable/enable OTP function
OCP_EN	5	RW	1h	0/1: Disable/enable OCP function
OVP_EN	4	RW	1h	0/1: Disable/enable OVP function
UVP_EN	3	RW	1h	0/1: Disable/enable UVP function
VDC_EN	2	RW	1h	0/1: Disable/enable VDC (Voltage Drop Compensation)
—	1	RW	0h	Reserved
—	0	RW	0h	Reserved

Table 9. The CONFIG Command Is Used to Configure the Power Protection Schemes

Functional Description (continued)

Interrupt Signal

The AP33772S supports a level-triggered interrupt signal through INT pin to the host MCU. The I2C command MASK (0x02) defines enable or disable of each interruptible event as shown in Table 10 below. The interrupt initialization is required before use. When the defined interruptible event happens, the AP33772S will set the INT pin output to level HIGH if the relevant event of the MASK register is enabled.

MASK	Bit	Attribute	Pwr-on	Description
—	7	RW	0h	Reserved
OTP_MSK	6	RW	0h	1: OTP status mask
OCP_MSK	5	RW	0h	1: OCP status mask
OVP_MSK	4	RW	0h	1: OVP status mask
UVP_MSK	3	RW	0h	1: UVP status mask
NEWPDO_MSK	2	RW	0h	1: NEWPDO status mask
READY_MSK	1	RW	1h	1: READY status mask
STARTED_MSK	0	RW	1h	1: STARTED status mask

Table 10. The MASK Register Defines Enable or Disable of Each Interruptible Event

System Data Acquisition

During the normal operation, the host MCU can monitor the PDO negotiation result (VREQ and IREQ), and its VOUT timely status (VOUT voltage and current) through I2C commands, where VREQ (0x14) and IREQ (0x15) are used to read the voltage and current requested, while VOLTAGE (0x11) and CURRENT(0x12) are used to read VOUT status. Meanwhile, the I2C command TEMP (0x13) is used to read the system temperature.

System Status and Operating Mode Inquiry

The system MCU can monitor the PD system status through I2C interface, and give a control of the TCD device. The Status command (0x01) is a 8-bit register, and used to store the AP33772S status as Table 11 below.

Meanwhile, the user can read out the PD operating modes through I2C command OPMODE (0x03), as shown in Table 12 below, where CC Flip information, cable voltage drop compensation, and power source type are provided.

STATUS	Bit	Attribute	Pwr-On	Description
—	7	RC	0h	Reserved
OTP	6	RC	0h	1:OTP status
OCP	5	RC	0h	1: OCP status
OVP	4	RC	0h	1: OVP status
UVP	3	RC	0h	1:UVP status
NEWPDO	2	RC	0h	1: New source PDOs received (Valid when PDMOD = 1)
READY	1	RC	0h	1: Ready to receive I2C request/command
STARTED	0	RC	0h	1: System started. Allow system configuration (register) to be updated within 100ms

Table 11. The STATUS Command Is Used to Monitor AP33772S Operating Status

OPMODE	Bit	Attribute	Pwr-On	Description
CCFLP	7	RO	0h	0 : CC1 is connected to CC line or unattached mode 1 : CC2 is connected to CC line
DR	6	RO	0h	0 : Normal mode 1 : DR (De-rating) mode
VDC	5	RO	0h	0 : Normal mode 1 : VDC (Voltage Drop Compensation) mode
—	4	RO	0h	Reserved
—	3	RO	0h	Reserved
—	2	RO	0h	Reserved
PDMOD	1	RO	0h	1: PD source connected
LGCYMOD	0	RO	0h	1: Legacy source connected (non-PD)

Table 12. The OPMODE Command Is Used to Monitor if PD or Legacy Source is Connected

Functional Description (continued)

LED Indication

The AP33772S controls LED lighting through LED pin. The Table 13 bellow summarizes the LED indication and VOUT result in each State.

State	LED Indication	VOUT	Comments
INIT	NA	OFF	VBUS/Rp attached and AP33772S initialization
CHARGING	4-sec Breathing	ON	Successful negotiation or enter Non-PD Mode and start charging
MISMATCH	Full Light	OFF	VSELMIN mismatch (VREQ < VSELMIN)
MOISTURE	2-sec Flicker	OFF	DN abnormal impedance detected
FAULT	0.6-sec Flicker	OFF	OVP, OCP, UVP or OTP occurs

Table 13. LED Indication for Different Negotiation Results

Cable Voltage Drop Compensation

The default value of voltage drop compensation threshold (VDCTHR) is 6%, which can be modified by writing the I2C VDCTHR command (0x1C).

After the AP33772S completes the negotiation and enables the VOUT MOS switch, the AP33772S monitors the VOUT voltage level when VDC_EN is set to 1. If the VOUT Voltage (VOLTAGE) fails to reach more than 6% below the Requested Voltage (VREQ), the AP33772S enables Automatic Type-C Cable Voltage Drop Compensation mechanism shown as Table 14 bellow.

Source PDO	Compensation Criteria	Compensation Manner	Voltage Compensation Upper Limit
Fixed PDO	$V_{VOUT} < V_{VREQ} * 0.94$ (Note 13)	PDO Position +1 (Next Higher Voltage PDO)	4.0V (Note 11)
PPS/AVS APDO	$V_{VOUT} < V_{VREQ} * 0.94$ (Note 13)	Voltage + 0.1V each Voltage Drop Compensation iteration	1.3V (Note 12)

Table 14. Type-C Cable Voltage Drop Compensation Criteria

Notes:
11. Only allow PDO 5V to be raised to PDO 9V and neglect the next higher PDO (15V and 20V), to prevent potential damage to subsequent circuits from battery charging.
12. The Type-C to Type-C compliance cables have typically end-to-end resistance of 250mΩ of any length. The maximum voltage drop compensation allowed is 1.3V - from source-end to sink-end of a Type-C to Type-C cable should be within 1.25V for maximum current of 5A.
13. Enables voltage drop compensation when $V_{VOUT} < V_{VREQ} * (1 - 6\%)$.

Functional Description (continued)

According to the source PDO (Fixed PDO or PPS PDO), the AP33772S chooses different compensation method. The Table 15 bellow shows the examples of Type-C to Type-C cable voltage drop compensation situations.

Source PDO	V_{VREQ}	Before Compensation		After Compensation	
		Original Request Voltage	V_{VOUT}	Adjusted Request Voltage (V_{AReq})	V_{VOUT}
Fixed_5V	5V	Fixed_5V	< 4.7V	Fixed_5V	< 4.7V
Fixed_5V / Fixed_9V	5V	Fixed_5V	< 4.7V	Fixed_9V	9V-Cable Voltage Drop (1.3V Max) (Note 14)
Fixed_5V / Fixed_9V / PPS_3.3V to 11V	5V	PPS_5V	< 4.7V	PPS_5V + Voltage Drop (1.3V Max) (Note 15)	≥ 4.7V
Fixed_5V / Fixed_9V / PPS_3.3V to 11V	5V	PPS_5V	< 4.7V	PPS_5V+1.3V	< 4.7V

Table 15. Type-C Cable Voltage Drop Comensation Criteria Under Different PDO Conditions

Notes: 14. If the cable voltage drop from the source-end to the sink-end is 1.0V, adjusted V_{AReq} would be 9V and V_{VOUT} would be 8V.

15. If the cable voltage drop from the source-end to the sink-end is 1.0V, adjusted V_{AReq} would be 5.7V for V_{VOUT} to reach 4.7V.

Legacy Type-A Charger Support

When the energy source is from a legacy Type-A charger with Type-A to Type-C cable connection to the TCD, the AP33772S enters the Non-PD Mode after PD negotiation fails. When VSELMIN is greater than VREQ, the associated VOUT MOS Switches are turned off. The Table 16 bellow shows the Non-PD Mode state of the AP33772S.

Non-PD Mode State		
V_{VREQ}	$V_{VSELMIN}$	V_{VOUT}
V_{VREQ} = 5V	$V_{VSELMIN}$ = 5V	ON
V_{VREQ} = 5V	$V_{VSELMIN}$ ≥ 9V	OFF

Table 16. VOUT Voltage Status versus $V_{VSELMIN}$ under Non-PD Mode

Functional Description (continued)

Temperate Estimation

The AP33772S provides a temperature estimation through a current source output from OTP pin, and an external NTC thermistor. There will be an IR voltage drop on the NTC resistor. With the AP33772S internal ADC, the voltage can be measured and then the NTC resistance can be calculated. The AP33772S then estimates the temperature value based on the 4 user-input NTC resistance values (TR25, TR50, TR75 and TR100), as shown in Figure 4 below, where the “LINEAR INTERPOLATION” and “LINEAR EXTRAPOLATION” are used for the inner range and outer range respectively. The estimated temperature is updated to internal register for I2C command TEMP (0x13) reading.

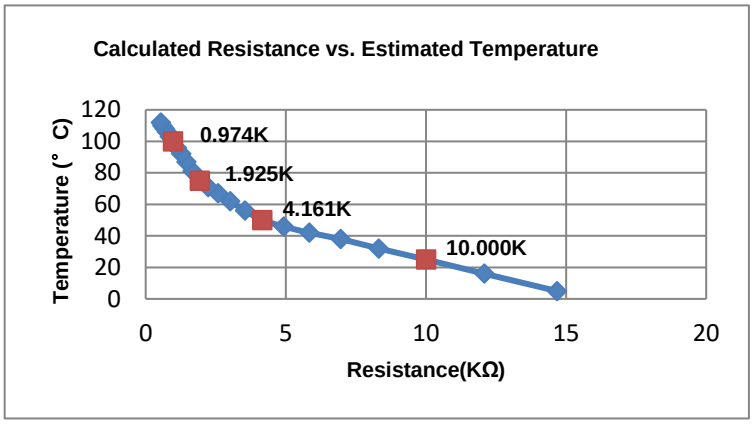


Figure 4. Calculated Resistance vs. Estimated Temperature Plot (RED Dot Shows Default Setting Values)

The host MCU must initialize the TR25, TR50, TR75 and TR100 registers before reading TEMP register or enabling OTP protection and power de-rating functions. Otherwise, the Murata NTC NCP03XH103 4-point data as Table 17 below are used as default. The user can change the default 4-point data through I2C commands: TR25 (0x0C), TR50 (0x0D), TR75 (0x0E), and TR100 (0x0F).

Register	Default Value	NTC Resistance (kΩ)	Temperature (°C)
TR25	2710h	10	25
TR50	1041h	4.161	50
TR75	0788h	1.928	75
TR100	03CEh	0.974	100

Table 17. The 4-Point NTC Resistances and Temperatures Are Used as Default in AP33772S

Functional Description (continued)

I2C Command Set Summary

The I2C commands used in the AP33772S are listed in Table 18 below.

Register	Command	Length	Pwr-On	Description
STATUS	0x01	1	00h	Status
MASK	0x02	1	03h	Interrupt enable mask
OPMODE	0x03	1	00h	Operation mode
CONFIG	0x04	1	FCh	System configuration options
PDCONFIG	0x05	1	03h	PD mode configuration options
SYSTEM	0x06	1	10h	System control and information
TR25	0x0C	2	2710h	Thermal Resistance @+25°C, Unit: Ω
TR50	0x0D	2	1041h	Thermal Resistance @+50°C, Unit: Ω
TR75	0x0E	2	0788h	Thermal Resistance @+75°C, Unit: Ω
TR100	0x0F	2	03CEh	Thermal Resistance @+100°C, Unit: Ω
VOLTAGE	0x11	2	0000h	The VOUT Voltage, LSB 80mV
CURRENT	0x12	1	00h	The VOUT Current, LSB 24mA
TEMP	0x13	1	19h	Temperature, Unit: °C The default value is 19h (+25°C)
VREQ	0x14	2	0000h	The latest requested voltage negotiated with the source, LSB 50mV
IREQ	0x15	2	0000h	The latest requested current negotiated with the source, LSB 10mA
VSELMIN	0x16	1	19h	The Minimum Selection Voltage, LSB 200mV The default value is 19h (5000mV).
UVPTHR	0x17	1	01h	UVP threshold, percentage(%) of VREQ The default value is 01h (80%).
OVPTHR	0x18	1	19h	OVP threshold, offset from VREQ. LSB 80mV The default value is 19h (2000mV).
OCPTHR	0x19	1	00h	OCP threshold, LSB 50mA
OTPTHR	0x1A	1	78h	OTP threshold, Unit: °C The default value is 78h (+120°C).
DRTHR	0x1B	1	78h	De-rating threshold, Unit: °C The default value is 78h (+120°C).
VDCTHR	0x1C	1	06h	VDC threshold, percentage (%) difference between VREQ and VOLTAGE. The default value is 06h (6%).
SRCPDO	0x20	26	All 00h	Get All PD Source Power Capabilities (PDO1 to PDO13)
SRC_SPR_PDO1	0x21	2	0000h	Source SPR PDO1
SRC_ SPR_PDO2	0x22	2	0000h	Source SPR PDO2
SRC_ SPR_PDO3	0x23	2	0000h	Source SPR PDO3
SRC_ SPR_PDO4	0x24	2	0000h	Source SPR PDO4
SRC_ SPR_PDO5	0x25	2	0000h	Source SPR PDO5
SRC_ SPR_PDO6	0x26	2	0000h	Source SPR PDO6
SRC_ SPR_PDO7	0x27	2	0000h	Source SPR PDO7
SRC_EPR_PDO8	0x28	2	0000h	Source EPR PDO8
SRC_EPR_PDO9	0x29	2	0000h	Source EPR PDO9
SRC_EPR_PDO10	0x2A	2	0000h	Source EPR PDO10
SRC_EPR_PDO11	0x2B	2	0000h	Source EPR PDO11
SRC_EPR_PDO12	0x2C	2	0000h	Source EPR PDO12
SRC_EPR_PDO13	0x2D	2	0000h	Source EPR PDO13
PD_REQMSG	0x31	2	0000h	Send request message with selected voltage, current and PDO index
PD_CMDMSG	0x32	1	00h	Send specific PD command message
PD_MSGRLT	0x33	1	00h	Result and status of PD request or command message

Table 18. The I2C Commands Provided in AP33772S PD3.1 Sink Controller Are Illustrated

Functional Description (continued)

I2C Command Format

The AP33772S supports I2C communication with external system MCU through SDA, SCL, and Interrupt pins after the power on reset. As an I2C slave device, the physical address of the AP33772S is 0x52. The I2C read and write operations are illustrated as below. All transactions begin with a Start and end with a Stop. A Start condition is defined as a HIGH to LOW transition of the SDA while SCL is HIGH. A Stop condition is defined as a LOW to HIGH transition of the SDA while SCL is HIGH. Start and Stop conditions are always generated by the I2C master, the host MCU of the TCD.

Data transfers follow the format shown below. After the Start condition, a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data read/write bit (R/W) - a 'zero' indicates a data write (W), a 'one' indicates a data read (R). A data transfer is always terminated by a Stop condition generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated Start condition (Restart) and address another slave without first generating a Stop condition. Each byte has to be followed by an acknowledge bit (A). The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line to indicate data received during the acknowledge clock pulse.

I2C Format for Write Data:

I2C Format for Read Data:

The memory representation of multi-byte data types on the AP33772S is Little Endian Byte Order. The least significant byte (the "little end") of the data is placed at the byte with the lowest address. For example, if the integer is stored as 4 bytes, then a variable X with value of 0x12345678 will be stored as Figure 5 below:

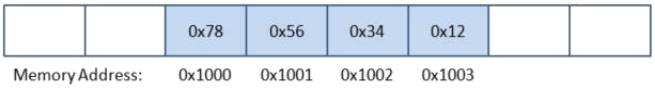
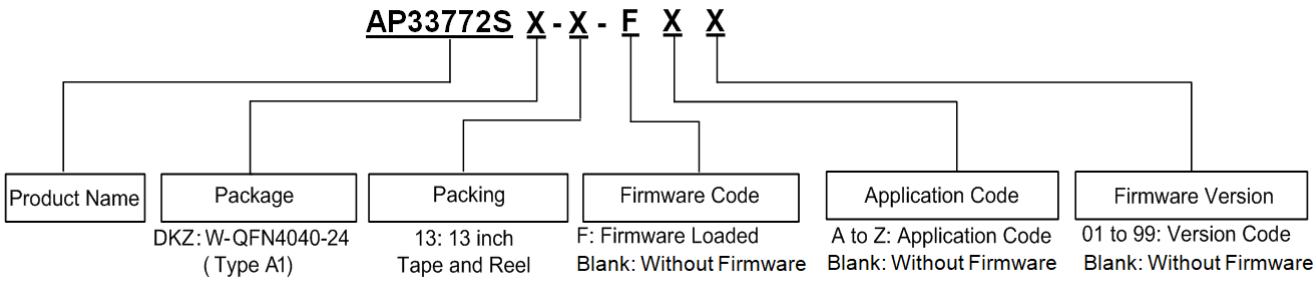


Figure 5. The Little Endian Byte Order Is Used in The AP33772S

Ordering Information

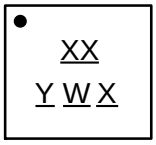


Part Number	Package	Identification Code	Packing	
			Qty.	Carrier
AP33772SDKZ-13-FA01	W-QFN4040-24 (Type A1)	6Y	3000	13” Tape & Reel

Marking Information

W-QFN4040-24 (Type A1)

(Top View)

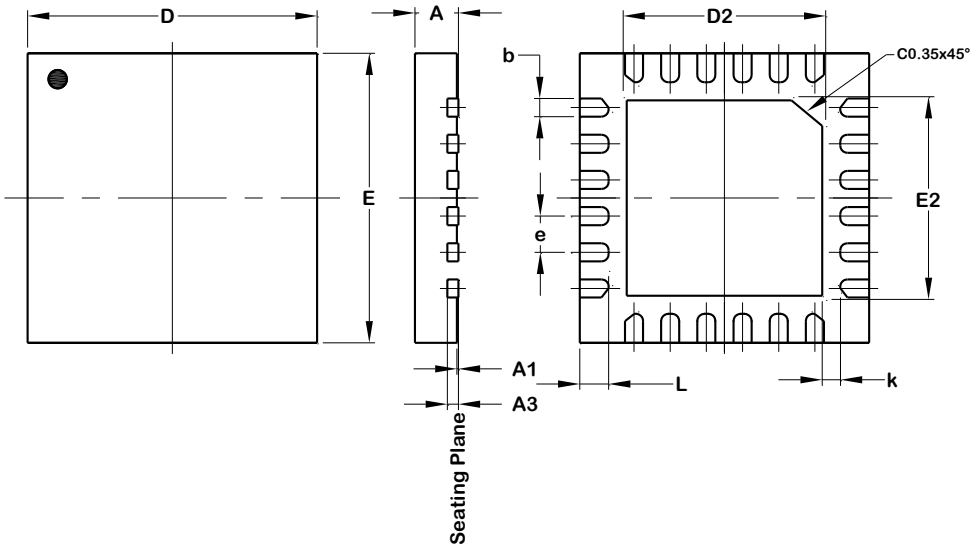


XX : Identification Code
Y : Year : 0 to 9
W : Week : A to Z : 1 to 26 Week;
a to z : 27 to 52 Week; z Represents
52 and 53 Week
X : Internal Code

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN4040-24 (Type A1)

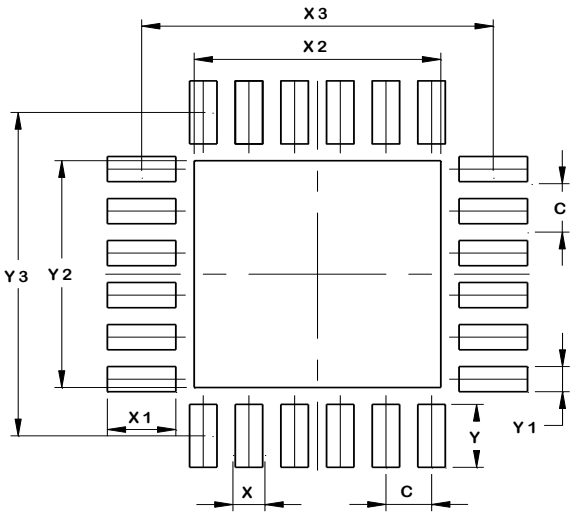


W-QFN4040-24 (Type A1)			
Dim	Min	Max	Typ
A	0.70	0.80	0.75
A1	0.00	0.05	0.02
A3	0.203 REF		
b	0.18	0.30	0.25
D	4.00 BSC		
D2	2.65	2.75	2.70
E	4.00 BSC		
E2	2.65	2.75	2.70
e	0.50 BSC		
k	0.20	--	--
L	0.35	0.45	0.40
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN4040-24 (Type A1)



Dimensions	Value (in mm)
C	0.500
X	0.300
X1	0.750
X2	2.700
X3	3.850
Y	0.750
Y1	0.300
Y2	2.700
Y3	3.850

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish—Matte Tin Plated Leads, Solderable per J-STD-202 (e3)
- Weight: 0.041 grams (Approximate)

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