

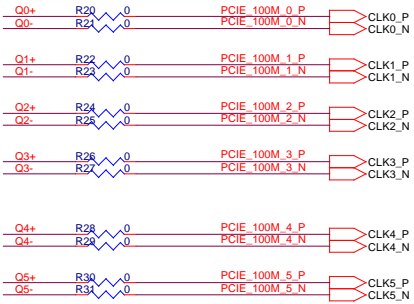
R1, R2, SMBUS Address set

* C1=C2=8pF for CL=8pF crystal, other CL value crystal use C1=C2=2xCL-8

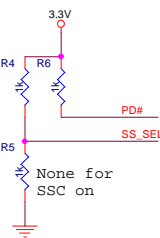
25M CMOS for LAN Ref. CLK

Put close to pin <300mil

Put close to pin <300mil



6 Low Power HCSL Output



SSC_SEL "H" = -0.5% SSC
SSC_SEL "L" or "M" = SSC off
Use SMBUS to set -0.25%

App Note:

1. All VDD pin needs 0.1u +1uF decoupling cloase to pin
2. VDDA, VDDOSC use small R+C filtering for better DC/DC ripple noise rejection
3. This is LP-HCSL type output: serial 0 ohm is optional, but it can be replace in 5 to 15 ohm for fine tune board RX end each clock skew due to different trace length
4. Since OSC pin cap.=5pF so select CL=8pF crystal can C1=C2=8pF, other CL value crystal C1=C2=2xCL-5-3, 3 is PCB C_stray pF
5. Note SSC_EN and SMBUS address pins are power on latch once set;
6. Make LVDS clock, it needs AC coupling and then RX side use pull-up/down Rs to bias LVDS level, refer to datasheet;
7. OEx# pins have internal pull-down
8. Connect epad to GND plane in 8 vias

Title		
Pi6CG33601C Application schematic		
Size	Document Number	Rev
B	Diodes Inc. Clock IC Application engineering	2
Date:	Thursday, June 20, 2019	Sheet 1 of 1