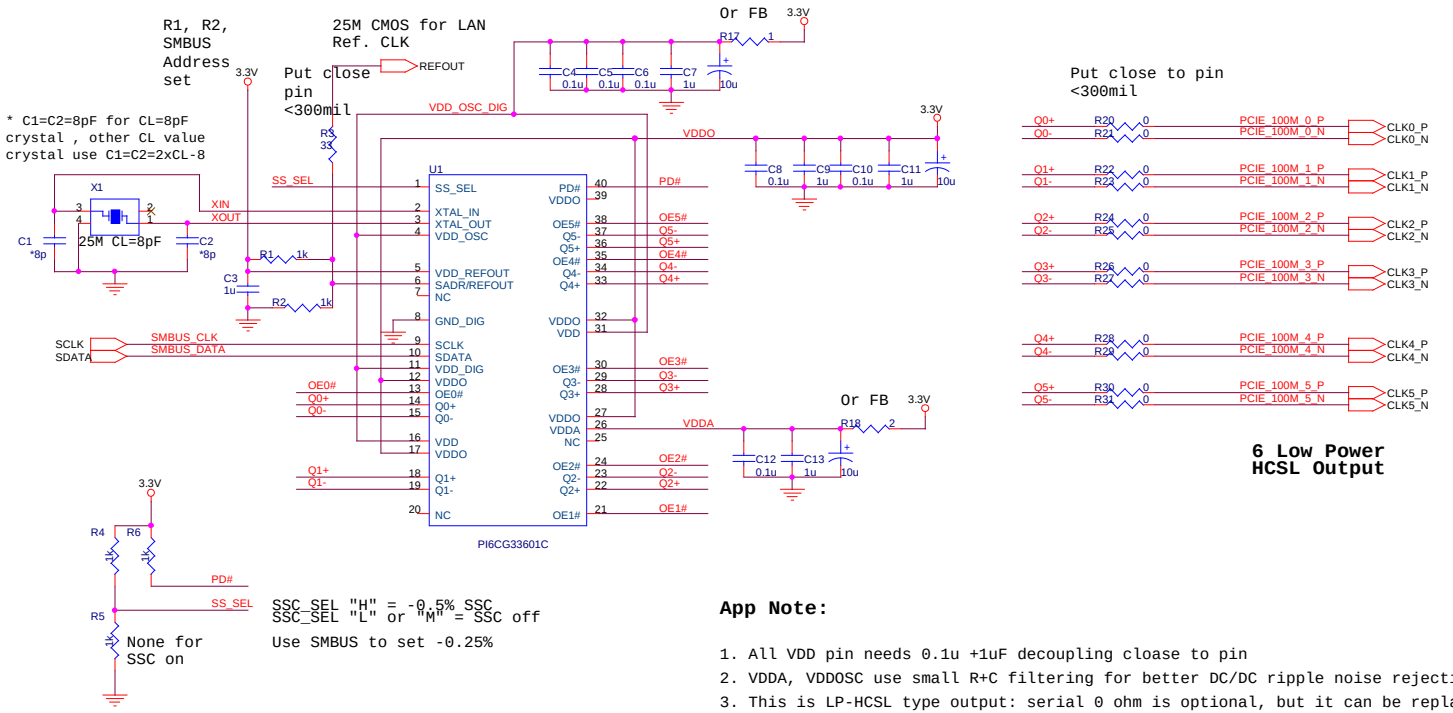

App Note:

1. All VDD pin needs 0.1u +1uF decoupling cloase to pin
2. VDDA, VDDOSC use small R+C filtering for better DC/DC ripple noise rejection
3. This is LP-HCSL type output: serial 0 ohm is optional, but it can be replace in 5 to 15 ohm for fine tune board RX end each clock skew due to different trace length
4. Since OSC pin cap.=5pF so select CL=8pF crystal can C1=C2=8pF, other CL value crystal C1=C2=2xCL-5-3, 3 is PCB C_stray pF
5. Note SSC_EN and SMBUS address pins are power on latch once set;
6. Make LVDS clock, it needs AC coupling and then RX side use pull-up/down Rs to bias LVDS level, refer to datasheet;
7. OEx# pins have internal pull-down
8. Connect epad to GND plane in 8 vias

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