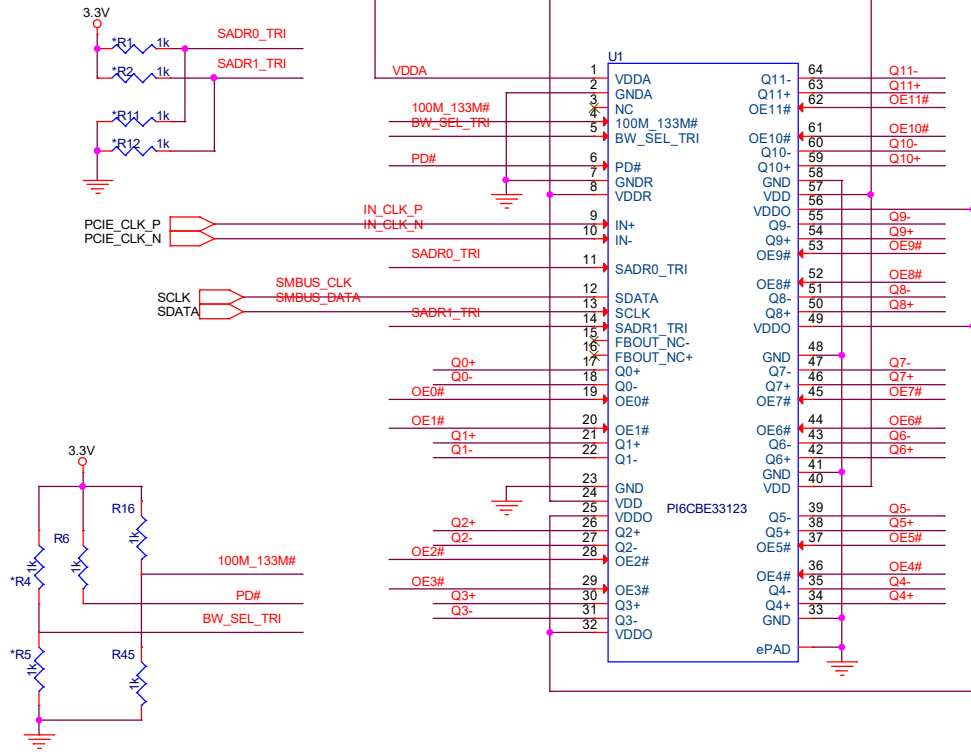


Set SADR0/1 logic in R1/R11
R2/R12, refer to datasheet



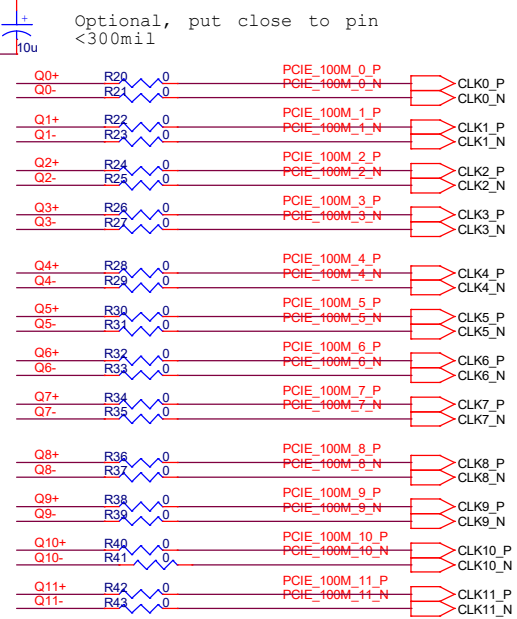
100M_133M#:
Set "0" for 133.33MHz app.
Set "1" for 100MHz app.

BW_SEL_TRI:
Set PLL BW logic in R4/R5
"0"=L_BW, "M"=Bypass, "1"=H_BW

OE0#
Make individual OE# pull-up/down to enable/disable each output
.
.
.
OE11#

App Note:

1. Each VDD pin needs 0.1u +1uF decoupling close to pin.(e.g.:VDD, VDDR, VDDA...etc)
2. VDDA use small R=1-2 ohm or FB(ferrite bead)+C=10uF filtering for better DC/DC ripple noise rejection
3. This is LP HCSL type output: serial 27ohm R , but it can be replace in 27 to 33 ohm for the optimal fine tune the board RX end waveform or different trace length if needed
4. Note, SMBUS address and BW_SEL_TRI pins are power on latch once set;
5. OE# pins have internal pull-down
6. Connect epad in 8 to 12 vias to GND plane
7. To Make LVDS output clock, it needs AC coupling and then RX side use pull-up/down Rs to bias in LVDS level, refer to datasheet;
8. Note, BW_SEL_TRI pin is power on latch once set



12 Low Power HCSL Output

Title			
PI6CBE33123 Application schematic			
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