

## Zetex SPICE Models

### Understanding Model Parameters and Applications Limitations

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#### Introduction

SPICE was originally developed as a simulation tool for Integrated Circuit design (SPICE being an acronym for Simulation Program with Integrated Circuit Emphasis) by the University of California in the 1970s. It was quickly improved into the SPICE2 version from which all commercial "Spice" programs are derived. It has since been enhanced (in terms of faster more robust algorithms and graphics handling capabilities for circuit input, and ease of analysing simulation output) and marketed by a number of companies for use within the PC environment - commercial versions being PSPICE, HSPICE, IsSPICE, SPICEAGE, Microcap etc.

Though originally intended for IC design, the availability of low cost computing, and the push towards robust design has introduced many other circuit and system designers to the advantages offered by analog circuit simulation. This has led to the requirement for device models for the active components under consideration, and so now many semiconductor companies provide appropriately targeted SPICE models as part of the technical support function.

These models can be extremely useful when used as a design tool, but care must be exercised. Any simulation software text will warn against sole reliance on the software's predictions. Models are (by definition) a compromise, and are essentially based on a device's common features. An appreciation of the model derivation, the model parameters, and it's inherent limitations should be sought, and would assist in the interpretation of simulation results and their application to the real world.

Zetex have created SPICE models for a range of semiconductor components. Many of these models are for the higher performance Bipolar and MOSFET transistors, but models for RF transistors, variable capacitance diodes, switching diodes and standard small signal parts are also available. These models are available through any Zetex sales office or agent.

Appendix A includes a printout of the introductory text file included in version 2 of the Zetex SPICE models disc. This file provides some background to how the model files are organised, and a brief overview of the model parameters for each type of device model.

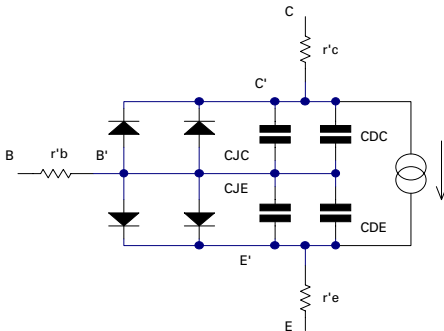
This application note is a guide to the understanding and use of Zetex SPICE models. It includes sections on how some of these models are derived - the measurements/optimisation necessary, how to customise models for those cases where a model is not available, and the limitations to be aware of.

## Measurement of Model Parameters

The bipolar transistor circuit model used by the SPICE software is a modified version of the Gummel-Poon model formulated in 1970. The schematic of this model is shown in Figure 1. For a comprehensive description of the model, including physical definitions of the model components, please refer to Appendix B, references 1 and 2.

Figure 2 shows a typical model for a Zetex bipolar transistor.

Lines beginning with an asterisk indicate a non-executable comment; so device details, date of creation, line spaces, and copyright messages all start with this symbol.



**Figure 1**  
**Gummel-Poon Bipolar Transistor Model.**

The line beginning “.MODEL ....” uses a standard SPICE command that defines a model to the software. Following this command are the device name, it’s polarity, and a list of the model parameters - the “+” sign being used for concatenation to the original command. The text file reproduced in appendix A gives some brief details as to the effects each parameter has on the model’s behaviour.

The measurements necessary to derive the bipolar transistor model parameter values can conveniently be separated into dc and ac parameters as shown in table 1. The dc parameters are further separated into those for forward and reverse operation. The parasitic resistance components, and the saturation current IS being common for both forward and reverse modes. The descriptions of the forward parameters given below is equally applicable to the reverse parameters. (Appendix B reference 3).

dc		ac
forward	reverse	
	IS	CJC
NF	NR	CJE
BF	BR	MJC
IKF	IKR	VJC
VAF	VAR	MJE
ISE	ISC	VJE
NE	NC	TF
	RB	TR
	RE	
	RC	

**Table 1**  
**Bipolar Transistor Model Parameters.**

```
*ZETEX   ZTX688B   Spice model   Last revision 8/11/90
*
.MODEL ZTX688B NPN IS = 1.09E-12 NF = 0.9935 BF = 1180 IKF= 5.2 VAF= 25
+ ISE=1.3E-13 NE =1.35 NR =0.992 BR =790 IKR=.5 VAR=5 ISC=0.174E-12
+ NC =1.399 RB = .3 RE =.036 RC = .034 CJC= 104E-12 MJC= .29 VJC= .46
+ CJE=280E-12 TF = .93E-9 TR =1.05E-9
*
```

**Figure 2**  
**General Format of Zetex (Bipolar Transistor) SPICE Models.**

An explanation of the function of the dc parameters is most easily accomplished with reference to a chart - sometimes referred to as the "Gummel Plot". Figure 3 shows a Gummel plot, which illustrates the variation in collector and base currents with base-emitter voltage - a requirement being that the device is on the edge of saturation, satisfied by  $V_{BC} = 0$ , (or  $V_{CE} = V_{BE}$ ). The collector current  $I_C$  (ideally) follows the Shockley equation that defines the current through a P-N junction:

$$I = I_s \left[ e^{\frac{qV_f}{KT}} - 1 \right]$$

where

$I_s$  - the transistor saturation current and is dependent on the size of the base-emitter area

$k$  - Boltzmann's constant =  $1.38 \times 10^{-23}$  J/K

$q$  - electronic charge =  $1.602 \times 10^{-19}$  C

$T$  - temperature in Kelvin, (300K is a common assumption)

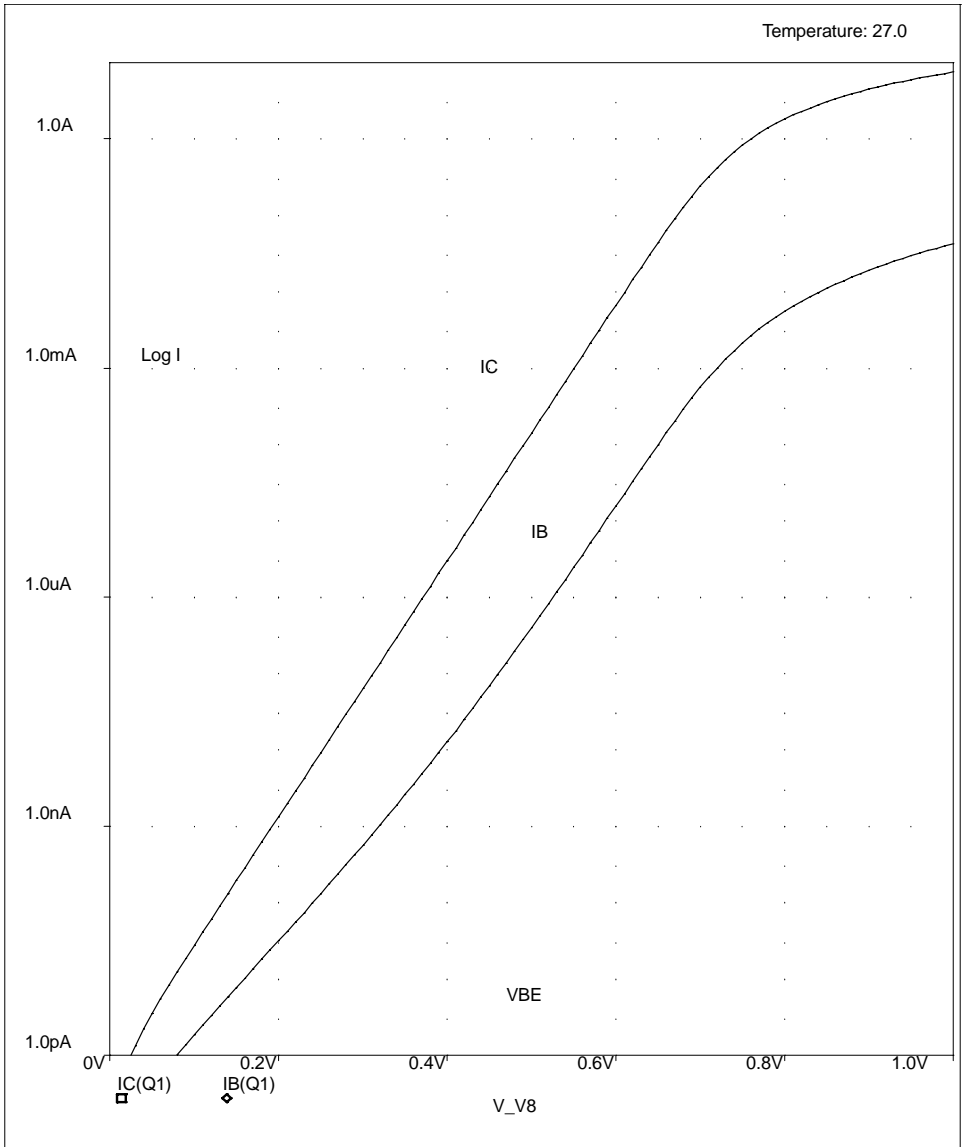
$V_f$  - is the voltage across the junction.

With reference to the chart,  $I_s$  is the y-axis intercept of the collector current curve at  $V_{BE} = 0$ , and  $NF$  defines the slope of the line (referred to  $q/kT$ ), and within

SPICE defaults to unity. At high currents, the collector current differs from that predicted by the equation due to resistances, and high level injection effects. These effects are accommodated within SPICE by allowing base-emitter de-biasing by the parasitic emitter resistance (or collector resistance for the reverse mode), and by the collector "knee" current parameter,  $IKF$ . ( $IKF$  is defined as the collector current at which the current gain =  $BF/2$ , see below).

The base current ( $I_B$ ) plot would ideally be parallel to the collector current, the plot separation being  $I_s/BF$ , however there are a number of physical effects that are addressed by other parameters.

At low values of collector current, surface leakage and recombination effects introduce an additional slope to the plot of  $I_B$ , causing the line to intercept the y axis at a higher position than would be the case if  $I_B$  was always a fixed fraction of  $I_C$ . These effects are described by two additional SPICE parameters;  $ISE$  - the y axis intercept for the  $I_B$  curve at  $V_{BE}=0$ , and  $NE$  - representing the slope of the affected region. These parameters introduce a fall in  $h_{FE}$  at low collector current. (Appendix B, reference 4 gives some useful illustrations on how these parameters affect transistor curves).



**Figure 3**  
**I<sub>C</sub> and I<sub>B</sub> Vs V<sub>BE</sub> Transconductance Chart - "Gummel Plot" (FMMT617). (Note 1).**

The Gummel Plot is produced either by careful curve tracer measurement, and/or by an arrangement of Source-Measure Units. The latter being particularly effective for low current measurements, and the former for the high current range. If more than one measurement system is used to produce Gummel data, then care must be exercised to ensure that temperature and accuracy differences do not produce offsets. The Gummel Plot measurement is usually automated, and the data collected into a PC where a logarithmic regression routine is used to determine IS, NF, ISE and NE.

The slope of the  $I_C$  versus  $V_{CE}$  output characteristics, (hoe in h-parameter parlance) is due to base width modulation effects as described by J.M. Early - and sometimes termed the Early effect, (please refer to Figure 4). The *Early voltage* is the point on the x axis at which the extrapolated curves would appear to intercept. This voltage (which possesses no sign) is known as VAF to the SPICE software, and allows the SPICE equations to predict the  $I_C$  value from the basic Shockley equation, at any value of  $V_{CE}$ . This allows the model to behave as expected in the linear region.

The VAF (VAR) parameters are determined by measuring  $I_C$  ( $I_E$ ) at several values of  $V_{CE}$  ( $V_{EC}$ ), and using linear regression to find the voltage axis intercept. A range of base currents are used, such that the resultant collector currents represent the usual operating range.

The ac parameters are the collector-base and base-emitter capacitances, and the forward and reverse base transition time

parameters. The capacitance parameters CJ, MJ, and VJ are determined by measuring the capacitance against reverse voltage (known as C-V data) for each junction, and then either using an iterative routine based on the equation below, or the P-N junction capacitance entry screen within the PSPICE PARTS package, or similar parameter extraction program.

$$C = \frac{CJ0}{\left(1 - \frac{V_R}{\phi}\right)^M}$$

where

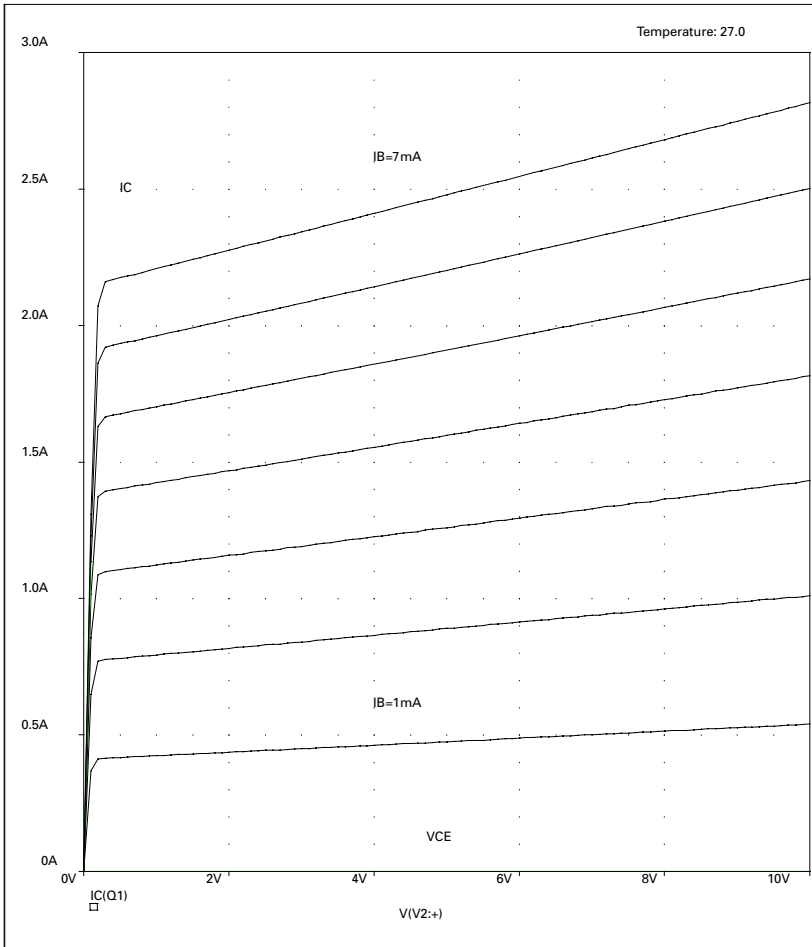
CJ0 - is the zero bias value

$\phi$  - is the junction barrier potential (known as VJC or VJE to SPICE)

M - is the grading coefficient (known as MJC or MJE to SPICE).

$V_R$  - is the applied reverse bias.

The transit time parameters can be found by an iterative approach based on a measurement of the  $F_T$  profile (transition frequency against collector current), and switching times for a particular range of conditions. The forward transit time TF is adjusted such that simulations of small signal RF gain measurements concur with  $F_T$  measurements (Appendix B reference 5) and turn-on times. The reverse transit time TR is determined by consideration of turn-off times, particularly bipolar storage time,  $t_s$ .



**Figure 4**  
 **$I_C$  Vs  $V_{CE}$  Output Characteristics Plot, Illustrating the "Early Effect" (FMMT617).** (Note 1).

Once a preliminary set of SPICE parameters have been derived via the measurements outlined above, the draft model is verified in various simulation circuits that reproduce the measurement conditions, and adjustments made to appropriate parameters as required.

### Model limitations

Please refer to Appendix A, which is a printout of the introductory text file on the Zetex SPICE model disc, and includes some comments on limitations.

In addition:

1. An important effect to consider for medium to high voltage device models is the **“Quasi-saturation Effect”** (Appendix B, reference 3). This effect is apparent as a two stage slope in the transistor’s saturation region, and an abrupt fall in  $h_{FE}$  at medium to high collector currents. This feature has been addressed within later versions of PSPICE, which includes additional parameters to model this region of operation. Zetex SPICE models are intended to be of general application, so these additional parameters are not included within the SPICE models. Some

experimentation is possible, using piecewise-linear (PWL) techniques with current sources within SPICE subcircuits, to enable different values of series resistance.

**NOTE:** It is recommended that simulations with high voltage models operating near to, or at their maximum operating current are thoroughly validated.

2. **Device package.** The SPICE fundamental device models are not aware of the package used to encapsulate the product, so resistance (other than that measured and accounted for within RC, RE etc), inductance and stray capacitance will not be included within the model. If these components are important within a particular application, then it is possible to create a subcircuit within SPICE that could incorporate the device model with additional passive components to represent parasitics.

Eg. Inductance for RF transistors and variable capacitance diodes, resistance for ESR components of RF diodes, and leakage resistance for MOSFETs. (Please refer to Figure 5 for an example of a variable capacitance diode with options

```
* ZETEX ZC830A Spice Model Last revision 4/3/92
*
.MODEL ZC830A D IS= 5.355E-15 N= 1.08 RS= 0.1161 XTI =3
+ EG= 1.11 CJO= 19.15E-12 M= 0.9001 VJ= 2.164 FC= 0.5
+ BV= 45.1 IBV= 51.74E-3 TT= 129.8E-9
* + ISR= 1.043E-12 NR= 2.01 (INCLUDE FOR LATER SPICE VERSIONS)
*
*NOTES: FOR RF OPERATION ADD PACKAGE INDUCTANCE OF 2.5E-9H AND SET
*RS=0.68 FOR 2V, 0.60 FOR 5V, 0.52 FOR 10V OR 0.46 FOR 20V BIAS.
*
```

**Figure 5**  
**Zetex ZC830A Variable Capacitance Diode SPICE Model, Illustrating Parasitic and ESR Components.**



provided for ESR and package inductance).

It also follows from the above that for dc or low frequency operation, and for those cases where a device model is not available for the package of interest, it may be worth considering models for electrically similar parts in other packages.

**3. Breakdown voltage.** The SPICE bipolar transistor models do not possess a breakdown voltage for any combination of terminals. This feature can be added within a subcircuit as above, by including a diode across the relevant terminals, with BV set to the minimum breakdown voltage specified on the transistor's datasheet. However, this will only indicate that there is current flow under overvoltage or transient conditions - it will **not** of course model the effects this would have on a device. This includes effects such as  $h_{FE}$  degradation due to reverse emitter-base current, heating and secondary breakdown effects, catastrophic breakdown of the gate oxide of MOSFETs, oscillation, and noise generation (at low values of avalanche current).

**4. Safe Operating Area.** Partially covered by the comments above on breakdown voltage, safe operating area (SOA) is not addressed by the SPICE model. So the designer would need to consider the usual SOA issues such as: maximum pulse currents (in reality limited by device gain  $h_{FE}/g_{FS}$  and the bond wire fusing current); thermal resistance of the basic silicon/package combination; and secondary breakdown loci. This can be

done with reference to the models' circuit behaviour and the datasheet charts, but for final design validation full breadboard analysis is recommended.

**5. Parametric variation.** The models do not include Monte Carlo parameters so statistical analysis of circuit performance due to lot and device variation is not available.

**NOTE: The model parameters are derived using nominal or mid-band value components.**

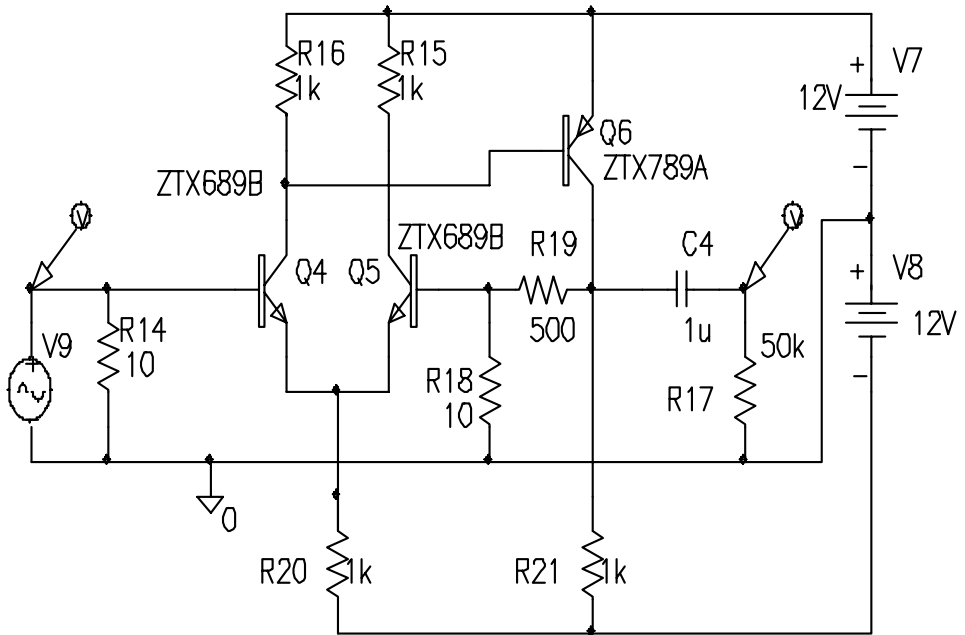
## Application Examples

This section presents several basic simulation circuits to demonstrate some of the functions that can be evaluated using Zetex SPICE models. These circuits represent some of the more basic, typical applications that can benefit from using Zetex components, and may serve as a basis for further experimentation.

It is recommended that any design is thoroughly checked in hardware before committing the design to production, to avoid falling prey to any software generated optimism, or effects due to **model** limitations of the Zetex parts and other circuit components.

**Discrete Component "Operational Amplifier".** This form of circuit is very popular within the audio industry for low noise pre-amplification of mV level signals, particularly from low impedance sources such as moving coil transducers. The advantage of a discrete implementation is that it allows the designer to employ relatively large area, high gain input devices. These devices present a low value of base spreading





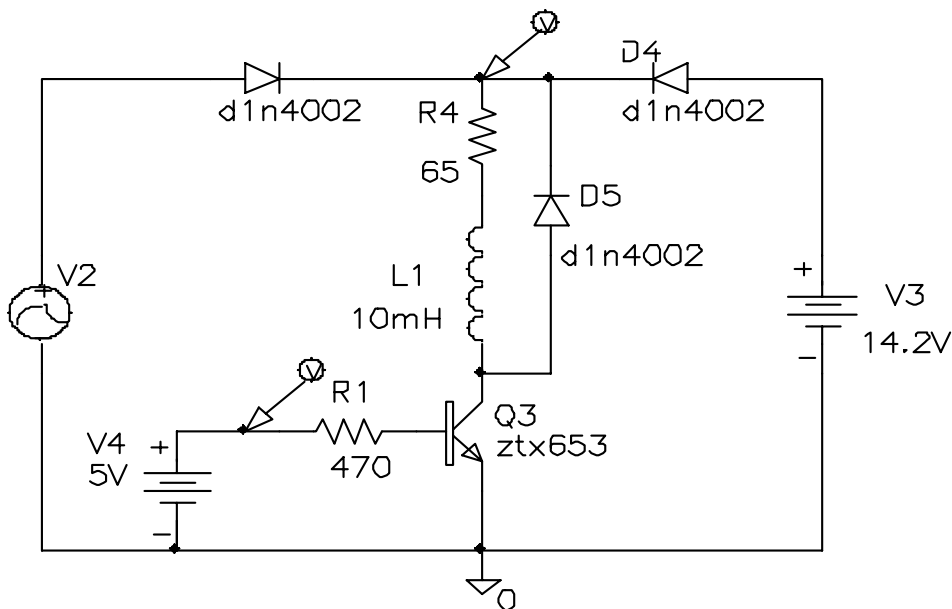
**Figure 6**  
**Discrete Component "Op-amp" using Matrix Geometry Transistors for Minimal Thermal Noise Generation.** (Note 1).

resistance to the input circuit, thereby minimising the amount of thermal noise generated. (Figure 6).

**Automotive Relay Driver.** Discrete transistors and Darlington's have widespread appeal as a cost effective relay or solenoid driver. A first pass analysis of such a circuit may suggest that the operating conditions experienced by the device, (that is the

level of performance demanded by the load under *nominal conditions*) are fairly benign. However, when transient events (such as generated by the many inductive loads sharing a common supply line) and environmental factors are considered, it is evident that the transistor driver deserves some attention.

As an example, the circuit shown in

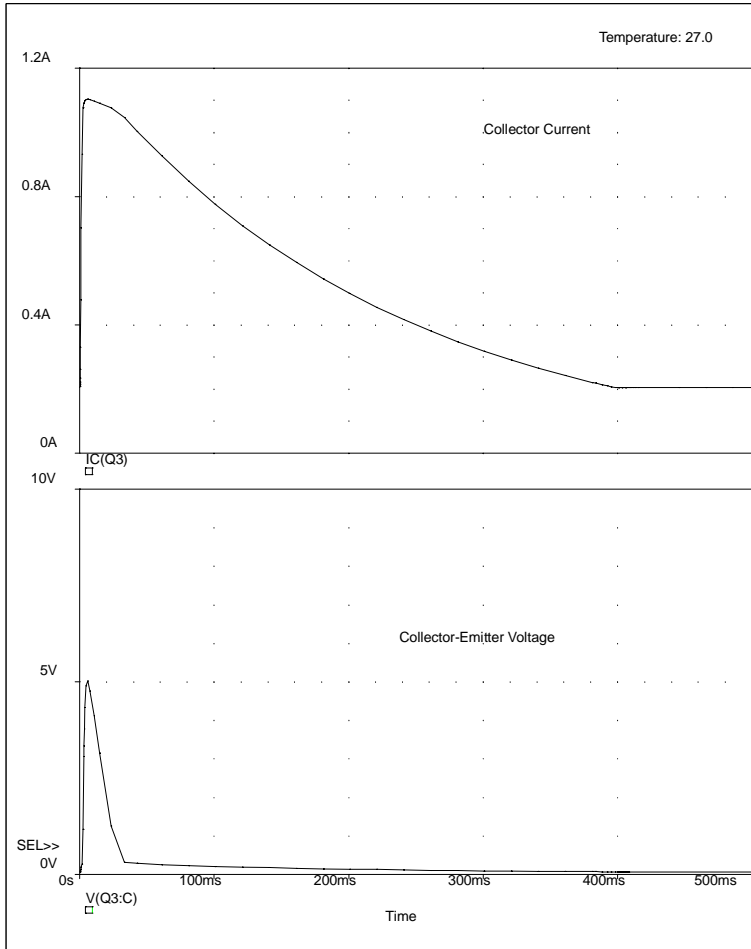


**Figure 7**  
**Automotive Relay Driver Circuit for Analysis of Transistor Behaviour under Transient Conditions.** (Note 1).

Figure 7 models the effect of a positive line transient on the operation of a simple relay driver while in the on-state. The resultant SPICE derived traces are given in Figure 8, which shows the collector current and collector-emitter voltage conditions imposed on the transistor. It can be seen that for the given bias condition, the transistor is unable to remain in the saturated state during the first few milli-seconds of the transient, but as the transient induced current falls, the transistor has sufficient  $h_{FE}$  to turn-on to a low  $V_{CE(sat)}$ . The period in which the device is within the linear operation region must be carefully considered, with respect to thermal and secondary breakdown compliance.

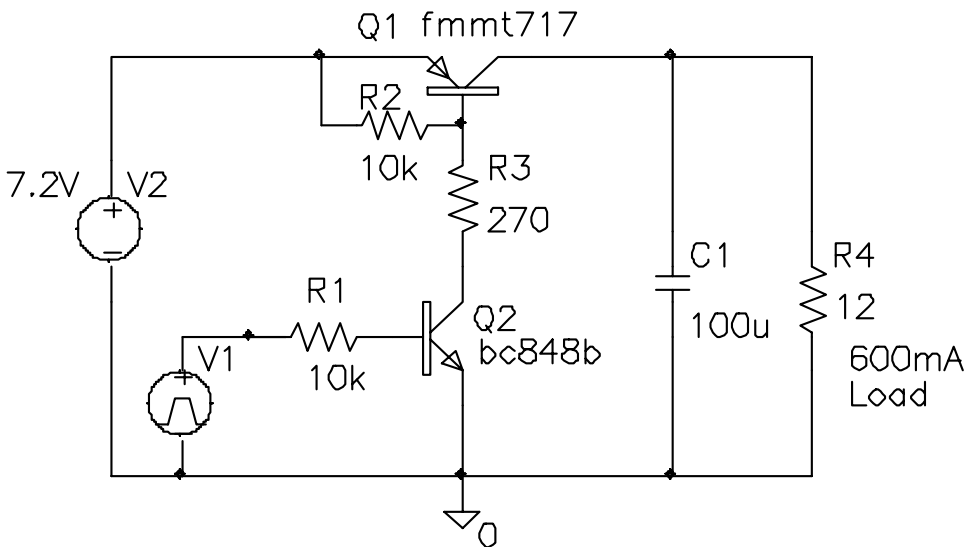
SPICE could further be used to verify the transient power generated, and to model the effects of different base drives.

**Positive Line Switch.** High gain low

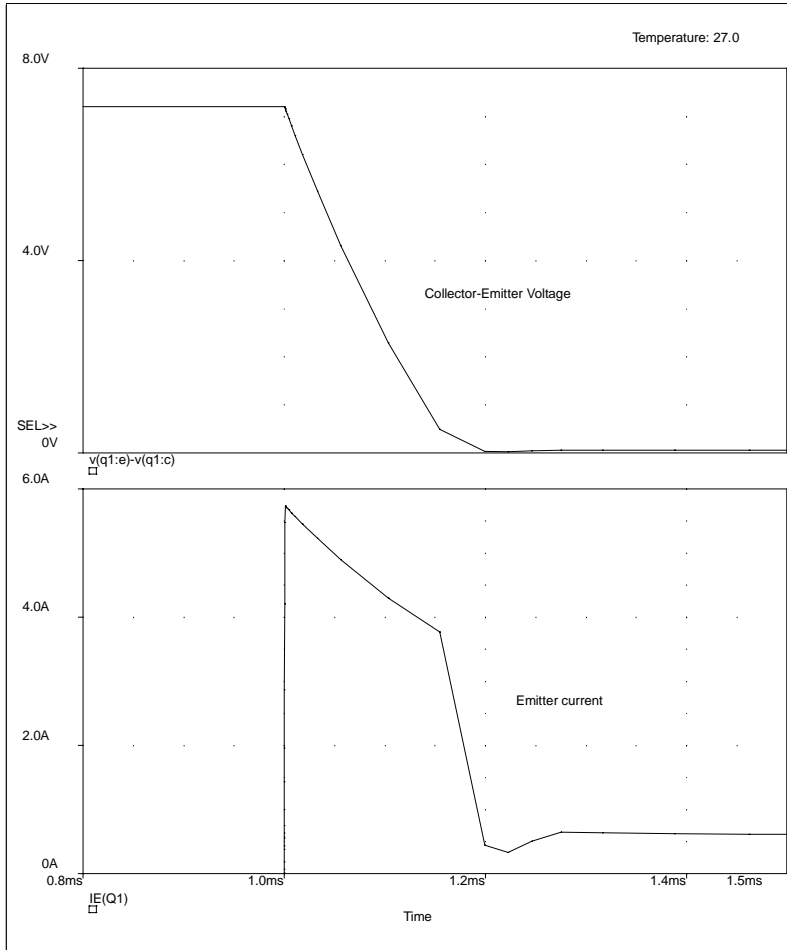


**Figure 8**  
**Automotive Relay Driver Circuit - SPICE Prediction of  $I_C$  and  $V_{CE}$  when subject to a + 80V, 230ms "Load Dump" Transient (Device "on" prior to Transient). (Note 1).**

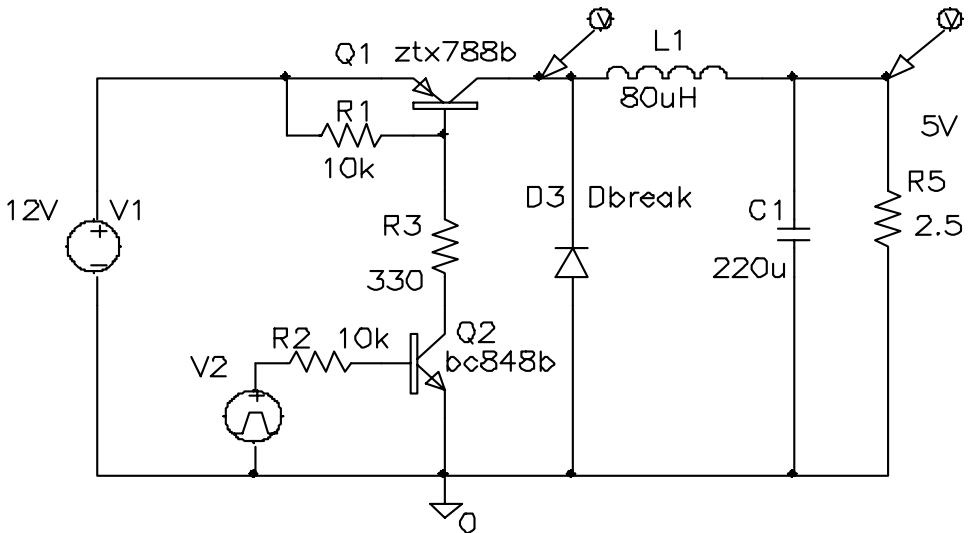
$V_{CE(sat)}$  Bipolar transistors are an excellent choice for this function (otherwise known as high side drivers, circuit block switches etc) as they allow a much more compact and cost effective design than competing MOS options. The generic form of the circuit shown in Figure 9, shows an FMMT717 SuperSOT (optimised SOT23) Bipolar transistor operating as a high side 600mA switch -as used for a mobile telephone transmit switch for example. Figure 10 shows the conditions experienced by the device at initial switch-on as the 100 $\mu$ F capacitor charges.



**Figure 9**  
Positive Line Switch using Zetex FMMT717 SuperSOT SOT23 PNP Bipolar Transistor, as a 600mA Load Supply Switch. (Note 1).



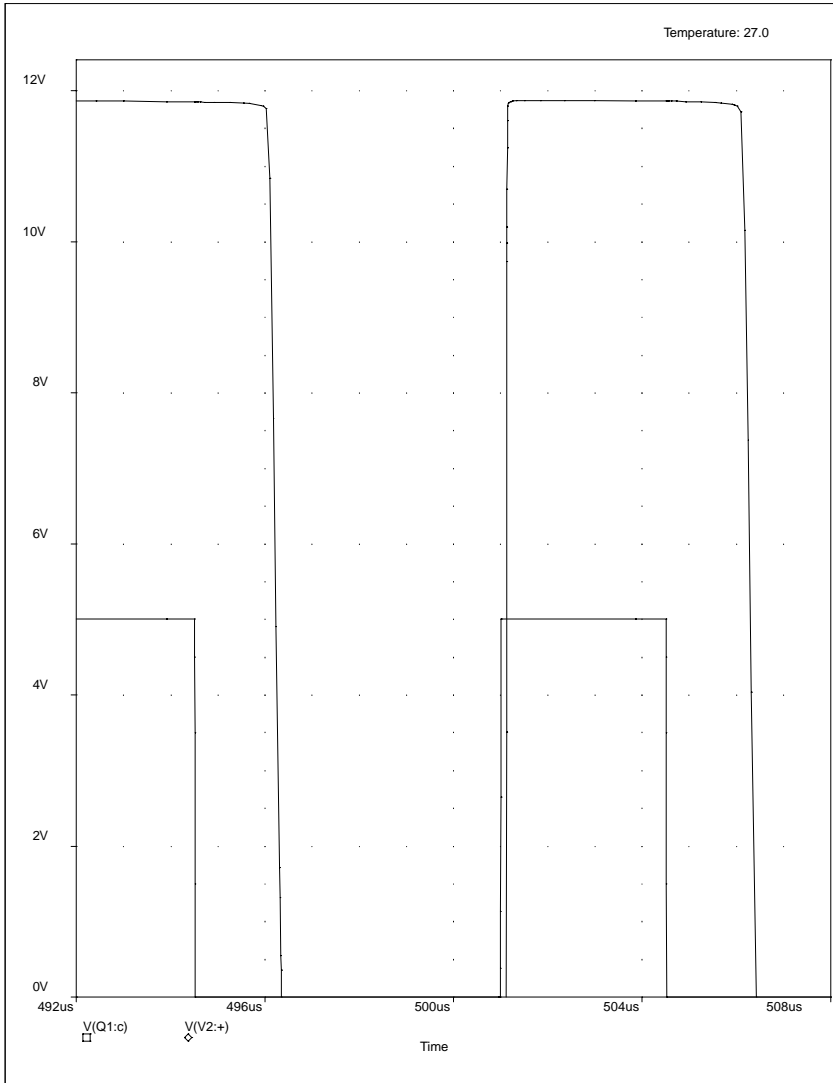
**Figure 10**  
**Positive Line Switch - SPICE Prediction of IC and VCE at Turn-on, showing Capacitive**  
**Charging Current in C1. (Note 1).**



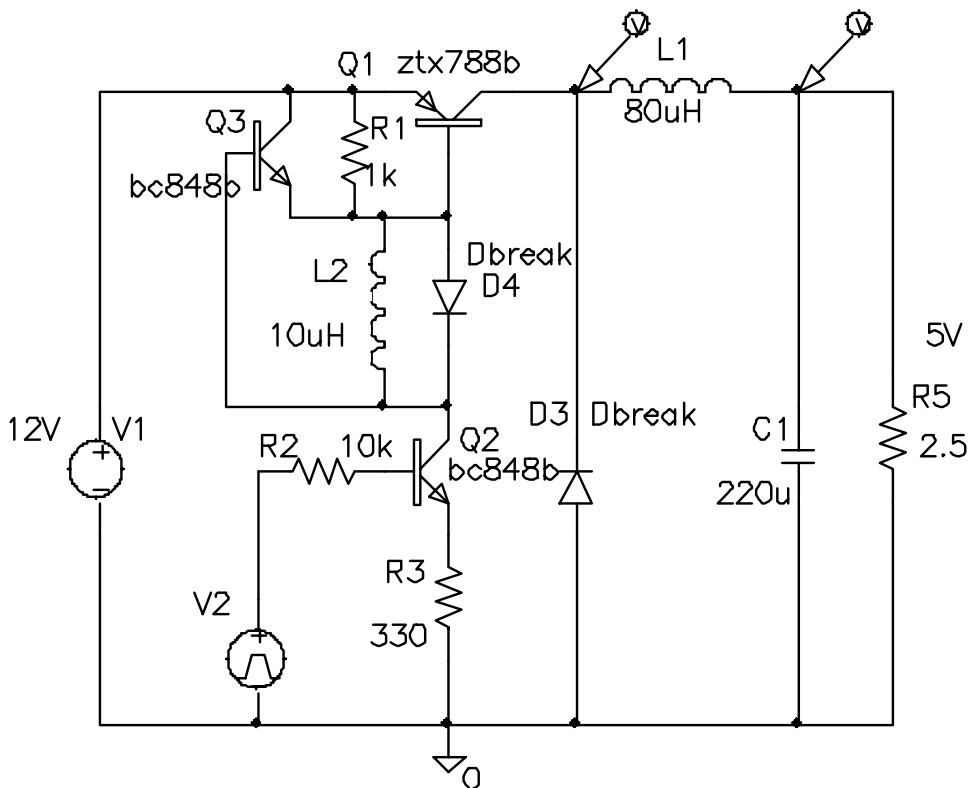
**Figure 11**  
**DC-DC Step-Down Converter using ZTX788B as a Switch Element in a 12V to 5V Circuit Operating at 100kHz. (Note 1).**

**Switch Element in DC-DC Step-Down Converter.** Figure 11 shows the general form of the "Buck" or step-down converter using a ZTX788B PNP transistor - this being an E-Line (TO92 style) Super- $\beta$  transistor, having a  $BV_{CEO}$  of 15V and a 3A continuous current rating. The circuit performs a 12V to 5V conversion at 100kHz, and supplies a 2A load. Figure 12 shows the waveforms recorded at the pulse source V2, and at the collector of the transistor, both with respect to 0V. The effect of the bipolar transistor storage time ( $t_s$ ) can be seen as a delay between the V2 transition to 0V, and the fall of the collector voltage. This storage time can be reduced to

some extent by optimising the base bias, and base-emitter resistors for a particular load current (perhaps also by sacrificing on-state loss by operating the transistor close to the edge of saturation) but this may not always be possible or preferred.



**Figure 12**  
**DC-DC Step-Down Converter - SPICE Prediction of ZTX788B Switching Waveforms.**  
Traces show PWM drive (5V level) and Collector-to-0V Waveforms. Note Storage Time Effects. (Note 1).

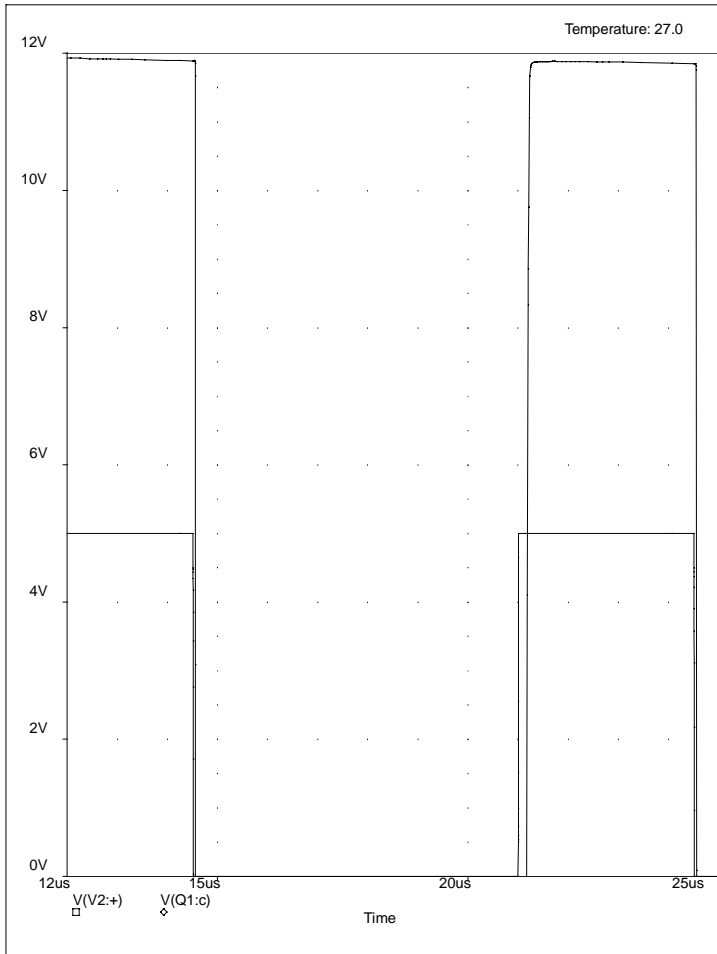


**Figure 13**  
**DC-DC Step-Down Converter using ZTX788B with Active Turn-Off Topology in a 12V to 5V Circuit operating at 100kHz. (Note 1).**

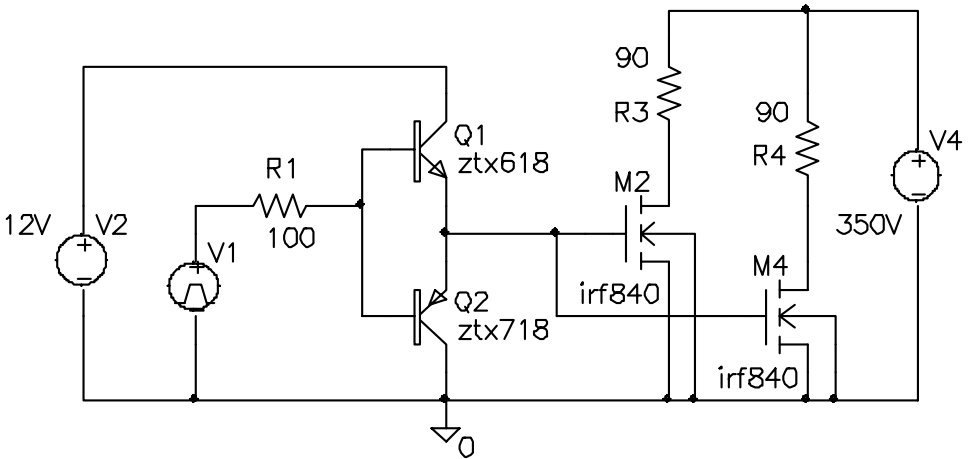
An alternative is to consider changing the passive turn-off (achieved by resistor R1) to an active turn-off method. Figure 13 shows one option of providing active turn-off to the base of the Bipolar transistor, and although this has resulted in the addition of a few components, this implementation is more cost effective than would be the case with a TO220 MOSFET based

design. The effect of the modification is apparent in Figure 14, which shows a combined storage and fall time of 40ns - comparable with MOSFETs, and also producing minimal switching loss.



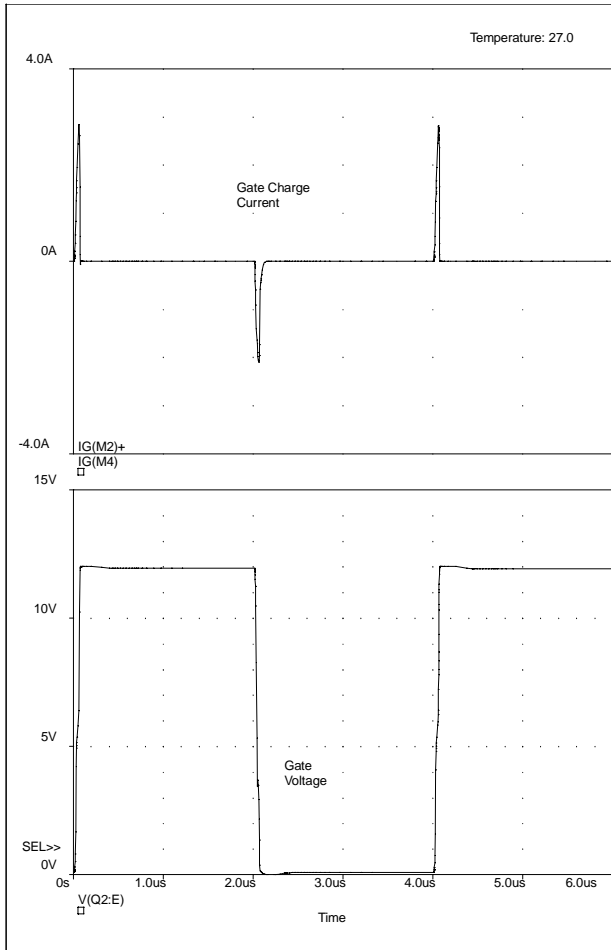


**Figure 14**  
**DC-DC Step-Down Converter - SPICE Prediction of ZTX788B Switching Waveforms.**  
**Traces show PWM Drive and Collector-to-0V Waveforms. Bipolar Transistor Turn-off**  
**Time = 50ns. (Note 1).**



**Figure 15**  
**Complementary Emitter Follower MOSFET Gate Driver using ZTX618/718.** (Note 1).

**Complementary Emitter Follower MOSFET Gate Driver.** A high current buffer is often required to supply the high transient currents demanded by Power MOSFETs operating at high switching speeds, say within off-line converters. This buffer is used to interface the power devices to the PWM controller IC which may have limited current source/sink capability. Figure 15 shows a conceptual circuit of a typical gate driver pair using the high gain 3A DC rated transistors ZTX618 and ZTX718. Figure 16 shows the gate voltage waveform, and the total gate charging current for a pair of power MOSFETs.



**Figure 16**  
**Complementary Emitter Follower MOSFET Gate Driver - SPICE Prediction of Gate Voltage and Current Waveforms. Gate Turn-On = 50ns. (Note 1).**

## Appendix A Reproduction of "Zetex.txt" Introductory text from Zetex SPICE models disc version 2.

ZETEX SEMICONDUCTORS

SPICE DISC VERSION 2V0 Oct 1995

Zetex is the largest UK owned specialist semiconductor manufacturer.

Zetex products are based on Bipolar and MOSFET technologies offered in a variety of package assemblies suitable for either through-hole or surface mount applications.

The product range includes:

- High current, very low VCE(sat) bipolar transistors
- Darlington transistors
- Small signal transistors
- RF and switching transistors
- Switching, reference and variable capacitance diodes
- MOSFETs
- Power management linear ICs
- A 20V linear ASIC process
- Opto-electronic products.

Zetex's 60,000 square feet production area features cleanrooms operating to class 10 and class 100, with SPC, ESD, PPM, FMEA, and FIT programs in place to ensure consistent product quality. The facility is approved to BS EN ISO 9001 (which covers both development and production functions), and products are routinely supplied to many international standards including BS9300, CECC 50000, and IECQ 750000, as well as many customer specific approvals conferred by major OEMs. All this is supported by a dedicated sales and marketing team including full technical and applications assistance.

For more information on the company and its products, please contact your nearest sales office.

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Zetex Spice Models

Introduction

Welcome to version 2 of the Zetex disc of Spice device models. This release contains Spice models for 108 Zetex device parents that source approximately 280 device types. These types include switching and varicap diodes, bipolar (high current low VCE(sat)), small signal bipolar, RF bipolar, bipolar Darlington and MOSFET transistors. This range is continuously under expansion as new products are introduced and retrospective models are generated for existing products.

This latest version of the Spice disc also includes a symbol library that allows the models to be used with the Windows versions of PSpice. Further information on the symbol library, including installation instructions, will be found in an additional text file in the root directory of this disc. This file is called ZETEXSYM.TXT.

The Spice models supplied on this disc are accessible in three ways:

- 1) The directory ZTXMODS contains a separate Spice model file for each Zetex device type for which a model is presently available. New model releases between major revisions of the Spice disc will be stored in the NEWMODS directory.
- 2) The directory ZTXLIBS contains the file ZMODELS.LIB in which all available Zetex device models are collected into a single file. New model releases between major revisions of the Spice disc will be stored within the ZNEWMODS.LIB library.
- 3) The directory ZTXWIN contains a symbol library (ZETEXM.SLB) that enables Windows versions of PSpice to use the Zetex SPICE models.

#### ZTXMODS and NEWMODS Model Files

Each of these files is a Spice model for a single Zetex device. They can be loaded into your simulation simply by employing the Spice command `<.INCLUDE Device_name.MOD>`. Only the device types specifically required by the circuit under simulation need be included in this way. All diode models and all but one of the bipolar transistor models are simple `<.MODEL>` files. However, the model for the FM597Q, all Darlington transistors and all MOSFET models are multi-component subcircuits and so are supplied as `<.SUBCKT>` files.

The diode models should be included in circuit files using the normal Spice reference: `<Dnum Anode_node Cathode_node Device_name>`.

Bipolar transistor models should be included using `<Qnum Collector_node Base_node Emitter_node Device_name>`.

All other models should be referenced as subcircuits, ie in the form `<Xnum Collector_node Base_node Emitter_node Device_name>` for the FM597Q and all Darlington transistors, and as `<Xnum Drain_node Gate_node Source_node Device_name>` for all MOSFET models.

#### The ZMODELS.LIB and ZNEWMODS.LIB Library Files

To save disc and directory space, some users may prefer to use the model libraries. For later Spice versions the ZMODELS.LIB and ZNEWMODS.LIB libraries are available. These are simply collections of all Zetex Spice models exactly as they appear in the individual

model directories. By using the statement `<.LIB ZMODELS.LIB>` and `<.LIB ZNEWMODS.LIB>`, Spice will be able to access any model within the libraries without the need for multiple `<.INCLUDE>` statements.

Note that all subcircuits, be they in the library files or the individual model files use the same connection sequence as Spice uses for single element models, thus easing their use.

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## Model Parameters and Limitations

### Bipolar Models

All bipolar transistor and Darlington models are based on the Spice modified Gummel-Poon model. Following is a typical model for a single transistor:-

ZETEX ZTX109 Spice model Last revision 4/90

\*

```
.MODEL ZTX109 NPN IS=1.8E-14 ISE=5.0E-14 NF=.9955 BF=400 BR=35.5  
+IKF=.14 IKR=.03 ISC=1.72E-13 NC=1.27 NR=1.005 RB=.56 RE=.6 RC=.25  
+VAF=80 VAR=12.5 CJE=13E-12 TF=.64E-9 CJC=4E-12 TR=50.72E-9  
MJC=.33
```

\*

A brief guide to the effect of each model element :-

IS and NE controls  $I_{cbo}$  and where  $h_{FE}$  falls with high  $I_c$ .  
ISE and NE control the fall in  $h_{FE}$  that occurs at low  $I_c$ .  
BF controls peak forward  $h_{FE}$ .  
BR controls peak reverse  $h_{FE}$  ie collector and emitter reversed.  
IKF controls where  $h_{FE}$  falls at high collector currents.  
IKR controls where reverse  $h_{FE}$  falls at high emitter currents.  
ISC and NC controls the fall of reverse  $h_{FE}$  at low currents.  
RC, RB and RE add series resistance to these device terminals.  
VAF controls the variation of collector current with voltage  
when the transistor is operated in its linear region.  
VAR the reverse version of VAF.  
CJC, VJC and MJC control  $C_{cb}$  and how it varies with  $V_{cb}$ .  
CJE controls  $C_{be}$ .  
TF controls  $F_t$  and switching speeds.  
TR controls switching storage times.

The standard bipolar transistor Spice model includes a parameter that allows BF, the  $h_{FE}$  parameter, to vary with temperature. This

---

parameter is called XTB and defaults to zero, Eg. no temperature dependence. If hFE temperature effects are of interest, then the following values may be used to provide an estimate, or a starting point for further investigation. It is suggested that the appropriate data sheet hFE profile is examined, and a Spice test circuit created that simulates the device in question and generates a set of hFE curves. Two or three such iterations should normally be sufficient to define a value for XTB in each case.

Polarity	XTB
NPN	1.6
PNP	1.9

Please remember that these notes are only a rough guide as to the effect of model parameters. Also, many of the parameters are interdependent so adjusting one parameter can affect many device characteristics.

At Zetex, we have endeavoured to make the models perform as closely to actual samples as possible but some compromises are forced which can result in simulation errors under some circumstances. The main areas of error observed so far have been:-

1. Spice is often over optimistic in the hFE a transistor will give when operated above it's data sheet current ratings. This is particularly true for a high voltage transistor operated at a low collector-emitter voltage.
2. Spice can be pessimistic when predicting switching storage time when current is extracted from the base of a transistor to speed turn-off.

#### Darlington Models

These are subcircuits using a standard transistor model. A Darlington model looks like:-

```
*ZETEX BCX38B Darlington Spice Subcircuit Last revision 4/9/90
*
.SUBCKT BCX38B 1 2 3
*           C B E
Q1 1 2 4 SUB38B
```



```
Q2 1 4 3 SUB38B 12.75  
*
```

```
.MODEL SUB38B NPN IS=1.1E-14 ISE= etc  
+ etc  
.ENDS BCX38B
```

Note that because Zetex Darlington's are monolithic, the two transistors used are identical in all respects other than size. (The number at the end of the Q2 line multiplies the size of the SUB38B transistor by 12.75 - the ratio of the areas of the input and output transistors for this device).

#### MOSFET Models

None of Spice's standard MOSFET models fit the characteristics of vertical MOSFETs too well. Consequently the models of Zetex MOSFETs supplied on this disc have been made using subcircuits that include additional components to improve simulation accuracy.

A typical MOSFET model:-

```
*ZETEX ZVN4106 MOSFET Spice Subcircuit Last revision 11/91  
*  
.SUBCKT ZVN4106 3 4 5  
*Nodes D G S  
M1 3 2 5 5 MOD1 L=1 W=1  
RG 4 2 343  
RL 3 5 6E6  
D1 5 3 DIODE1  
.MODEL MOD1 NMOS VTO=2.474 RS=1.68 RD=0.0 IS=1E-15 KP=-.296  
+CGSO=23.5P CGDO=4.5P CDB=35.5P PB=1 LAMBDA=267E-6  
.MODEL DIODE1 D IS=1.254E-13 N=1.0207 RS=0.222  
.ENDS ZVN4106  
*
```

In the NMOS model,

VTO defines  $V_{gs(th)}$ .

RS and RD add series terminal resistance.

IS controls the behaviour of the model's body diode.

KP controls  $G_m$

LAMBDA controls variation of drain current with drain-source

---

voltage when operated in the linear region.

CGDO controls Crss.

CGSO controls Ciss.

CBD controls Coss.

Added to Spice's standard NMOS model are a gate resistor to control switching speeds, a drain-source resistor to control leakage and a drain-source diode to accurately reflect the performance of the MOSFET's body diode.

The MOSFET models mirror the performance of the real devices well in most areas. One area not covered however is the way that Crss and Coss varies with drain-source voltage. Thus if the models are used at a drain-source voltage well away from data sheet capacitance definition voltages, and capacitance is critical, then the values used for CGSO and CGDO may need adjustment.

#### Diode Models

Diodes from Zetex's Switching and Varicap range are presently modelled on this disc. They use a standard Spice diode model and a typical file appears as follows:-

```
*ZETEX ZC830A Spice Model Last revision 4/3/92
```

```
*
```

```
.MODEL ZC830A D IS=5.355E-15 N=1.08 RS=0.1161 XTI=3
```

```
+ EG=1.11 CJO=19.15E-12 M=0.9001 VJ=2.164 FC=0.5
```

```
+ BV=45.1 IBV=51.74E-3 TT=129.8E-9
```

```
* + ISR=1.043E-12 NR=2.01 (INCLUDE FOR LATER SPICE VERSIONS)
```

```
*
```

```
*NOTES: FOR RF OPERATION ADD PACKAGE INDUCTANCE OF 2.5E-9H AND SET
```

```
*RS=0.68 FOR 2V, 0.60 FOR 5V, 0.52 FOR 10V OR 0.46 FOR 20V BIAS.
```

```
*
```

In this model,

IS controls forward and reverse current against voltage.

N controls forward current against voltage.

RS controls forward voltage at high current.

CJO, M and VJ control variation of capacitance with voltage.

BV and IBV control reverse breakdown characteristics.

TT controls switching reverse recovery characteristics.

ISR and NR (if activated) control reverse biased leakage.

For operation at RF (which would be the norm for a varicap diode) it is recommended that a 2.5nH series inductor be added as an extra circuit element to correct for the inherent package inductance. Also, to give the varicap diode it's correct Q, the model value for RS should be changed to the appropriate figure suggested in the NOTES for the expected reverse bias.

The switching diode models may include a constant value capacitor rather than the parameters CJO etc if chip and packaging strays greatly exceed true junction capacitance values.

---

#### Further Information

Zetex's library of Spice models is being continuously updated so if the model you require does not appear on this disc, please contact us at the address given below or through your local Zetex office. If you have any problems with the models supplied here, you may use the same address to request applications assistance.

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## Appendix B

### References

1. "An Integral Charge Control Model of Bipolar Transistors", Gummel and H.C. Poon, Bell Syst. Tech. J., Vol. 49, May 1970.
2. "Modeling the Bipolar Transistor" CAD for Electronic Circuits , Volume 1, Ian E. Getreu. Elsevier Scientific Publishing Company. ISBN 0-444-41722-2.
3. "MicroSim PSPICE A/D Circuit Analysis Reference Manual", Analog Devices, Pages 170-178.
4. "SPICE- A Guide to Circuit Simulation & Analysis Using PSPICE" , Paul W. Tuinenga. Prentice-Hall, Inc. ISBN 0-13-747270-6.
5. "Measuring Small Signal Common Emitter Current Gain of Transistors at High Frequencies" ASTM Standard, Vol. 10.04 Electronics, F632-79.

**Note 1:** Circuit diagrams and waveforms reproduced from PSpice "Schematics" and "Probe" screens, with permission of MicroSim Corporation.