

High Frequency DC-DC Conversion using High Current Bipolar Transistors

400kHz Operation with Optimised Geometry Devices

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Introduction

DC-DC conversion is one of the fundamental circuit functions within the electronics industry and addresses a wide field of market sectors, applications and supply requirements. A general trend, (to pursue cost, size and reliability advantages) has been to reduce the size of the DC-DC converter systems, and as the inductive elements of such a system are quite often the bulkiest components, increases in switching frequency provide one method to allow this. Switching frequencies therefore have increased from tens of kHz to hundreds of kHz, which has forced a revision of the enabling switching devices.

It is an often assumed maxim that bipolar transistors are useful for DC-DC conversion functions up to perhaps 50kHz, and for service beyond this frequency, that MOSFETs provide the only solution. The purpose of this application note is to demonstrate that bipolar transistors possessing superior geometries - thereby providing a higher current capability per die area, can and are operated to reasonably high switching frequencies with minimal loss. This often allows a more compact

design (due to the higher silicon efficiency of bipolar technology) and lower cost.

Background

To obtain the most efficient performance from bipolar transistors at high switching frequencies, an appreciation of the basic switching mechanisms and base charge analysis is useful. Appendix A provides an introduction to bipolar transistor switching behaviour, and appendix B provides references for mathematical treatments.

There are various methods for increasing the maximum switching speed of bipolar transistors. Some of these rely on preventing saturation of the device, thus vastly reducing the stored charge, while other methods remove the charge at turn-off. Figures 1, 2 and 5 show a number of common speed-up networks. Figures 1a through 1d show various options for preventing saturation, and effectively reduce/limit base drive when the collector terminal has fallen to a specific level. (Figure 1a is often termed a Schottky transistor, and is often used for IC transistors, and

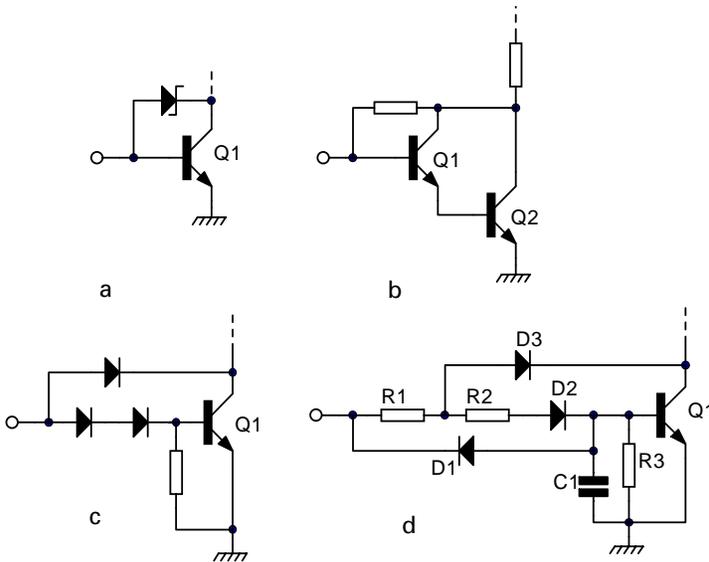


Figure 1.
Non-saturating Bipolar Transistor Speed-up Methods.

Figures 1c and 1d are variants of the so called Baker clamp circuit).

These methods (the Baker clamp being preferred for high power applications) of course do not allow the transistor's collector-emitter voltage to saturate to a very low level, and so the resultant on-state loss may be high and therefore prohibit the use of smaller packaged, though adequately current capable devices. Figures 2 and 5 show two methods that allow true saturation by permitting sufficient forward base drive, while removing charge quickly at turn-off. Design of such networks is non-critical, and by suitable choice of components allow high levels of base overdrive with no penalty to turn-off time duration.

Figure 2 shows a method of speeding up PNP devices to enable replacement of large P-Channel MOSFETs - this particular circuit being designed for fast charging of battery packs by Benchmark Microelectronics. Figures 3 and 4 show the relevant waveforms, for a standard passive turn-off method (base-emitter pull-up resistor) and the speed-up circuit of Figure 2 - the combined storage and fall times being reduced from 1.2 μ s to 80ns. Importantly, the major switching loss contributor - the fall time, has been significantly reduced to 40ns, which is comparable to, or better than P-Channel MOSFET performance. This allows cost effective replacement of large packaged devices.

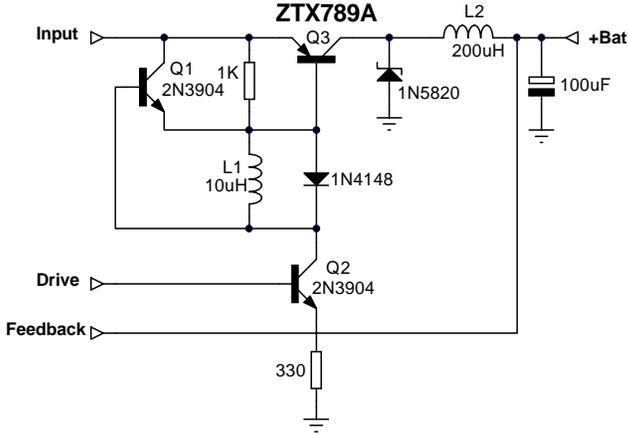


Figure 2.
PNP Transistor Speed-up Circuit to Allow Replacement of P-Channel MOSFETs within High Current Converters. (The circuit shown is suitable for output currents up to 1.5A; other variants are capable of operation to 5A output).

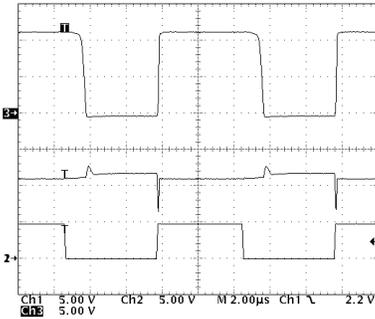


Figure 3.
Turn-off Waveforms for PNP Step-down Converter using Passive Turn-off.
Upper Trace - Collector-to-0V, 5V/div;
Middle Trace - PNP base-to-0V;
Lower Trace - PWM IC Output, 5v/div.
Timebase at 2µs/div.

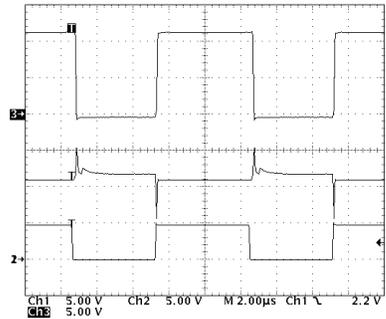


Figure 4.
Turn-off Waveforms for PNP Step-down Converter (of Figure 2) using Active Turn-off.
Upper Trace - Collector-to-0V, 5V/div;
Middle Trace - PNP base-to-0V;
Lower Trace - PWM IC Output, 5v/div.
Timebase at 2µs/div.

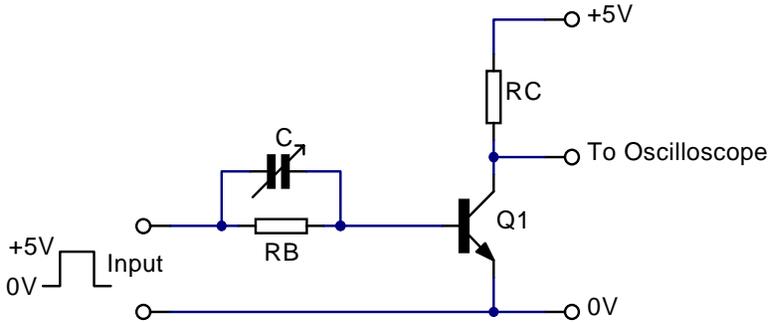


Figure 5.
Capacitive Speed-up method/Circuit to Determine Minimum Value of Turn-Off Charge of a Bipolar Transistor.

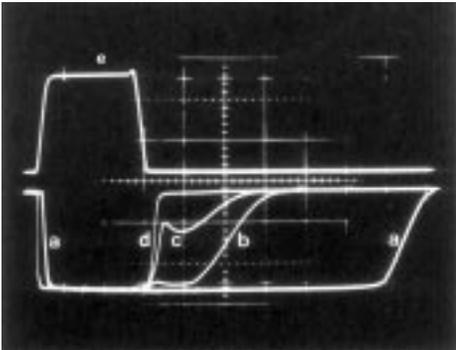


Figure 6.
Turn-Off Waveforms, and Effect of Varying Parallel ("Speed-Up") Capacitance.
Upper trace - Input waveform;
lower traces - (a) $C=0$, (b) $C=100\text{pF}$,
(c) $C=120\text{pF}$, (d) $C=130\text{pF}$ (stored charge just removed).

Horizontal scale= 200ns/div , Vertical scale= 2V/div . ZTX300, $I_B=1\text{mA}$, $I_C=10\text{mA}$.

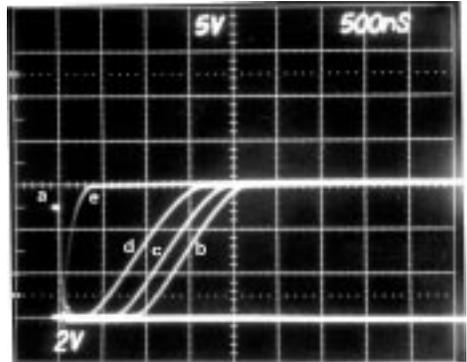


Figure 7.
Turn-Off Waveforms, and Effect of Varying Parallel ("Speed-Up") Capacitance.
Trace (a) - Input waveform;
turn-off traces - (b) $C=0$, (c) $C=470\text{pF}$, (d) $C=820\text{pF}$, (e) $C=1.5\text{nF}$ (stored charge removed).

Horizontal scale= 500ns/div , Vertical scales: Input= 2V/div ; collector= 5V/div . ZTX1048A, $I_B=10\text{mA}$, $I_C=500\text{mA}$.

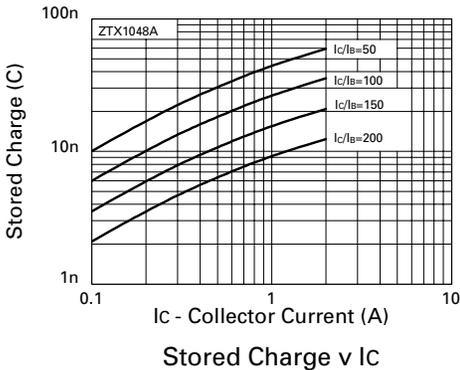


Figure 8.
Turn-off Charge Required as a Function of Collector Current and Forced Gain, for the ZTX1048A Bipolar Transistor.

Figure 5 shows the standard speed-up capacitance method, although in practice a finished design would use a fixed value capacitor. A similar circuit can also be used to determine the capacitance required for a particular bias condition. In practise the variable capacitance (or value of parallel capacitance) is adjusted such that the sum of stored charge and junction capacitance charge is just removed - allowing for device variation, temperature and bias tolerance.

The oscillographs in Figures 6 and 7 show the effect of increasing the capacitor value from zero (Eg. open circuit) to a value adequate to neutralise the stored charge. Figure 6 is for a small signal device, while Figure 7 is for the ZTX1048A - a transistor utilising the Zetex Matrix geometry, and a Super- β emitter process to produce a 4A DC rated part in the TO92 style E-Line package. Figure 8 summarises a set of such

measurements for the ZTX1048A - for example, at a collector current of 1A and a forced gain of 200, a turn-off charge of 900pC is required to neutralise stored charge and eliminate storage time effects.

[Note 1: Appendix A also includes some ancillary material on the minimum amount of trigger charge necessary for pulse circuits].

Power Conversion Circuits

To demonstrate the performance advantages possible when the bipolar transistor's turn-off charge is addressed, this section considers such modifications to a basic step-down DC-DC converter. The circuit shown in Figure 9 was used to provide a means of evaluation, and is of fairly standard implementation, apart from the choice of the FMMT718 SuperSOT SOT23 PNP transistor. This circuit, with minimal design optimisation, can produce the efficiency against load current characteristic shown in Figure 10. This chart also shows how the bias conditions for the pass device can be modified to increase the current capability of the circuit, albeit with some compromise to conversion efficiency at lower load currents. Curves 1, 2 and 3 illustrate this effect for base currents of 9.4mA, 43mA and 170mA respectively. Figure 11 shows how the efficiency varies with input voltage for the $I_B=43mA$ option. Higher output current designs are possible with larger die transistors from the Zetex range, such as the ZTX788B, ZTX789A, ZTX790A, ZTX948 and ZTX949. For a comprehensive listing please refer to Semiconductor Data Books one and two.

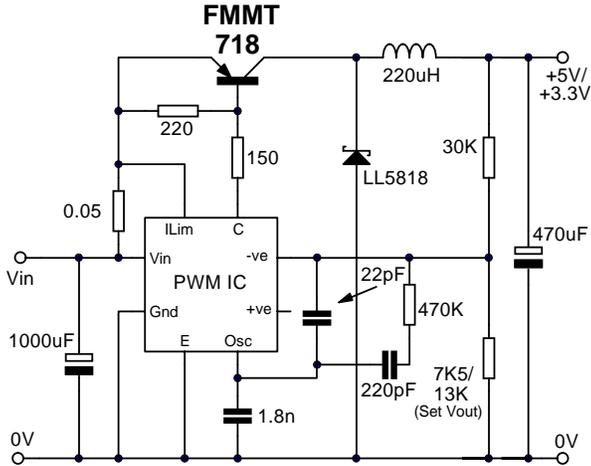


Figure 9.
Basic Step-Down DC-DC Converter using the LM3578 and the FM718.
(With values shown, $F_{op}=50\text{kHz}$, $I_B=43\text{mA}$, peak efficiency=88%).

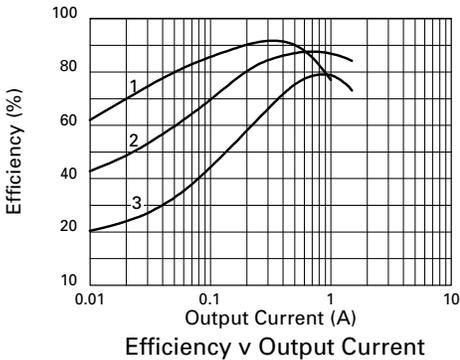


Figure 10.
Efficiency against Load Current for the Converter of Figure 9, with I_B as a parameter.
Curve 1 - $I_B=9.4\text{mA}$; Curve 2 - $I_B=43\text{mA}$;
Curve 3 - $I_B=170\text{mA}$. $F_{op}=50\text{kHz}$; $V_{in}=7\text{V}$;
 $V_{out}=5\text{V}$.

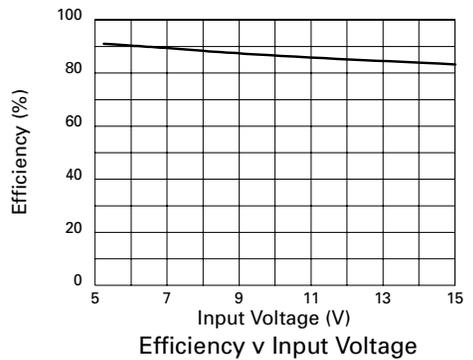


Figure 11.
Efficiency against Input Voltage for the Converter of Figure 9. ($I_B=43\text{mA}$; $I_{out}=1\text{A}$).

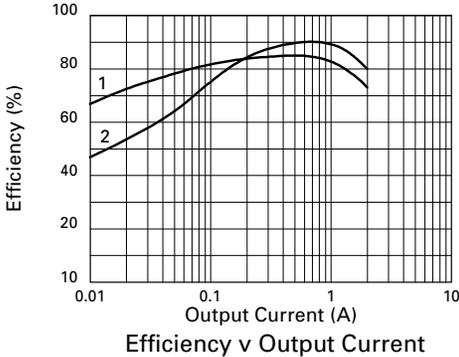


Figure 12.
Efficiency against Load Current for the Converter of Figure 9.
 $I_B=43mA$; $F_{op}=90kHz$; $V_{in}=7V$; $V_{out}=5V$.
Effect of Variation of Inductor Value.
Curve 1 - $25\mu H$, Curve 2 - $180\mu H$.

Optimisation, and some scope for higher frequency operation is possible with this basic converter. Figure 12 shows the effect of varying the inductors value, with the switching frequency set to 90kHz. Turn-on time was recorded at 55ns, and turn-off at 1.5µs.

To investigate options for higher switching frequencies requires a change to the PWM controller IC. Figure 13 shows a circuit based on the TI5001 device. This IC is capable of operation up to a switching frequency of 400kHz, and can sink a maximum of 20mA into the VO pin.

The initial circuit was configured to operate at 150kHz, with the FM718 base current set to 9mA by a 560Ω base resistor (R1) - effectively a forced gain of 222 at 2A. Turn-on and turn-off times were measured at 200ns and 1.44µs

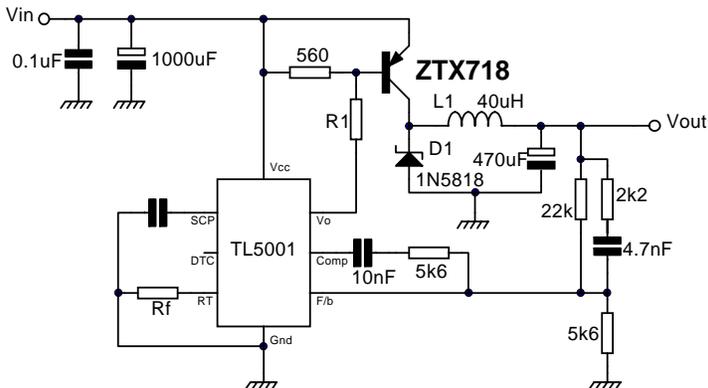


Figure 13.
Basic Step-Down DC-DC Converter using the TI5001 and the FM718. (With values shown, $F_{op}=150kHz$, $I_B=9mA$, peak efficiency=81%).

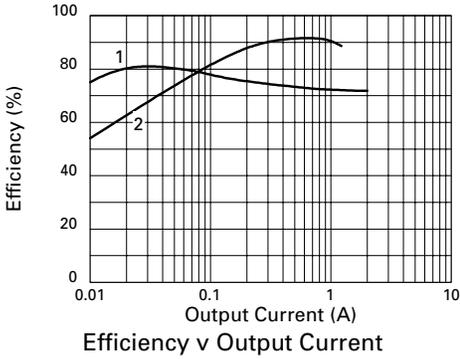


Figure 14.
Efficiency against Load Current for the
Converters of Figure 13 and 16.

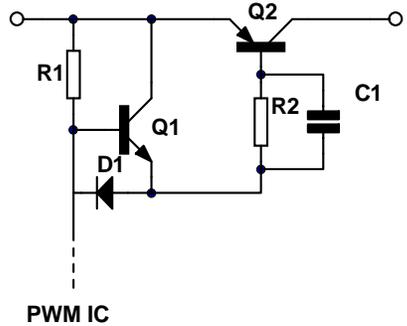


Figure 15.
Bipolar Transistor Turn-off Circuit to allow
Capacitive Turn-off Charge Neutralisation
with PWM Controller IC.

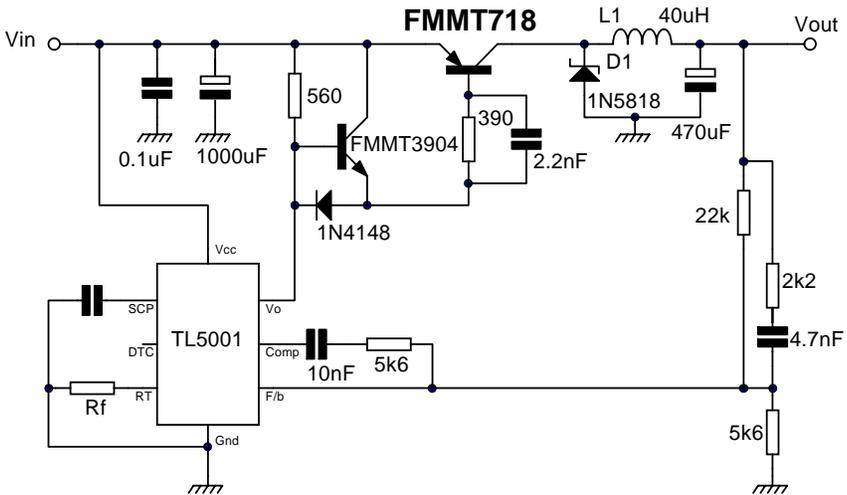


Figure 16.
Basic Step-down DC-DC Converter using the TL5001/FM718 Combination with
Capacitive Turn-off Circuit.

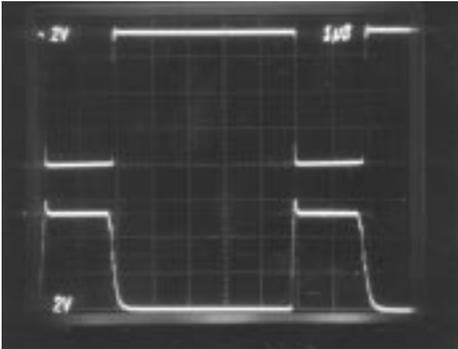


Figure 17.
Switching Waveforms for the circuit of Figure 16, operating at 150kHz. Upper trace; 2V/div, Collector-to-0V. Lower trace; 2V/div, Base-to-0V. $V_{in}=7V$, $V_{out}=5V$, $I_L=220mA$.

respectively. The chart shown in Figure 14 (curve 1) illustrates the resultant efficiency versus load profile. The circuit's conversion efficiency peaks at 81% at 23mA output, but falls thereafter to 71% at 2A, due mainly to switching losses, though in some part to increasing $V_{CE(sat)}$ at higher currents. The latter factor could be addressed in part by considering the load requirements, and optimising for the relevant condition, but the switching losses would remain.

By considering the base turn-off charge and effecting a suitable turn-off circuit (Figure 15) the circuit shown in Figure 16 was produced. This shows a significant improvement in conversion efficiency at medium to higher currents; as shown in

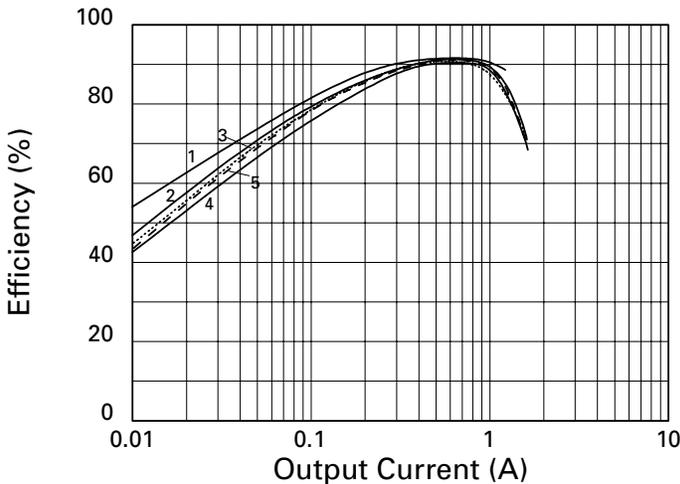


Figure 18.
Efficiency against Load Current for the Converter of Figure 16. Curve 1 - $F_{op}=150kHz$; curve 2 - 220kHz; curve 3 - 300kHz; curve 4 - 400kHz. $I_B=10mA$. Curve 5 - 400kHz and $I_B=5mA$. $V_{in}=7V$, $V_{out}=5V$.

Figure 14, curve 2. This shows a peak efficiency of 92%. Figure 17 shows the switching waveforms, including the collector-to-0V waveform - note the rapid turn-off edge; this was measured to be 25ns. The efficiency at lower currents has of course reduced, due to the extra current taken by the turn-off circuit. This efficiency profile can be modified for specific applications by sacrificing high current efficiency in favour of low current performance or vice-versa.

Further modifications were effected to assess performance at still higher switching frequencies. Figure 18 shows the efficiency/load current profiles for switching frequencies from 150kHz to 400kHz. Figure 19 shows the efficiency against input voltage for the 220kHz

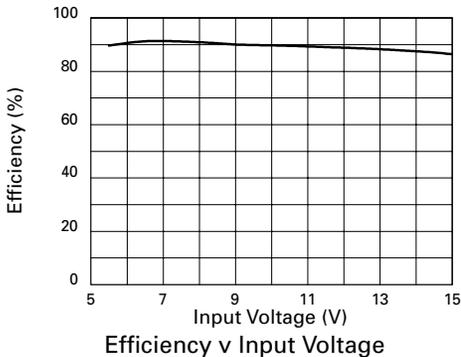


Figure 19.
Efficiency against Input Voltage for the Converter of Figure 16.
 $F_{op}=220kHz$; $V_{out}=5V$; load current=1A.

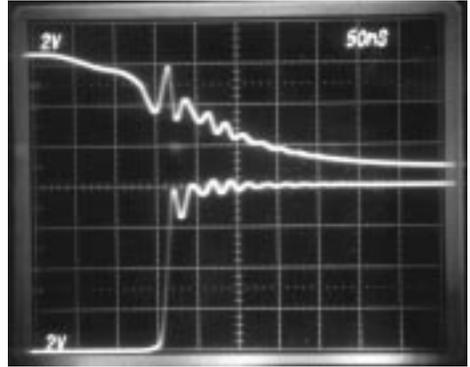


Figure 20.
Switching Waveforms for the Converter of Figure 16 operating at 400kHz. Turn-on edges. Risetime= 20ns. Upper trace - Base-to-0V, 2V/div. Lower trace - Collector-to-0V, 2V/div. Timebase at 50ns/div.

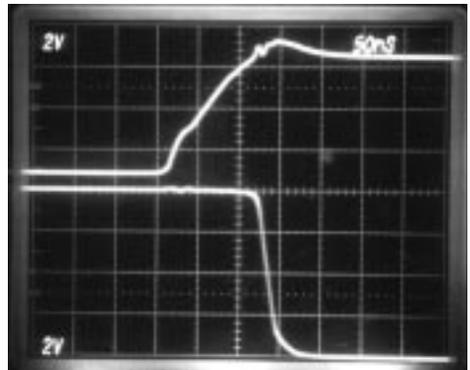


Figure 21.
Switching Waveforms for the Converter of Figure 16 operating at 400kHz. Turn-off edges. Falltime=30ns. Upper trace - Base-to-0V, 2V/div. Lower trace - Collector-to-0V, 2V/div. Timebase at 50ns/div.

version - the curve varying little over the measured range. Figure 18 curve 5, is again for a switching frequency of 400kHz, but with lower base drive ($R_B=680\Omega$) and a reduction to 1.5nF for the turn-off capacitor. The oscillographs shown in Figures 20 and 21 show the turn-on and turn-off switching waveforms for the 400kHz version. These show collector rise and fall times of 20ns and 30ns respectively.

Conclusions

This application note has demonstrated that with due attention to the base and collector charge phenomena in bipolar transistors, the operating switching frequency of those parts can be extended well beyond the currently accepted notional maximum of 40kHz, to several hundred kHz. Various speed-up methods have been summarised, and examples of those particularly suitable and complementary to high current capable transistors examined, and circuit examples presented.

Appendix A

Bipolar Transistor Switching Behaviour

In most switching circuits trigger capacitors are required to differentiate pulses and provide DC isolation between stages, and speed-up capacitors are needed to neutralise the stored charge and junction capacitances of the transistors. In most cases it is sufficient to choose values small enough not to interfere with the operation of the circuit at its maximum frequency. These capacitors do however have minimum values depending on the type of transistor used, the base and collector currents, and the amplitude of the waveforms involved.

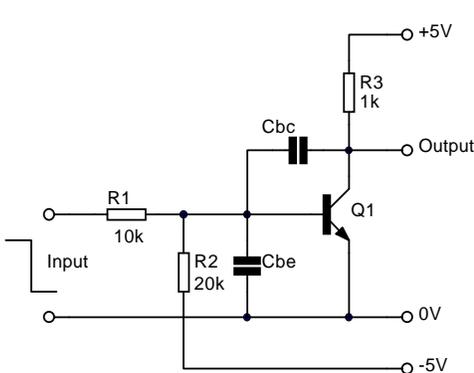


Figure 22.
Bipolar Transistor Switching Circuit for Illustration of Basic Switching Behaviour.

In order to understand the requirement for speed-up capacitors, consider the simple inverter circuit shown in Figure 22, and the resultant switching waveforms shown schematically in Figure 23.

Initially Q1 is cut off with its base-emitter (b-e) junction reverse biased to $-1.67V$ and its collector-base (c-b) reverse biased by $6.67V$. On the rising edge of the input pulse the potential at point A (V_{BE}) rises exponentially as the junction capacitances of the transistor charge, until the V_{BE} reaches $0.6-0.7V$ and the b-e junction starts to conduct significant current. The time before this occurs from the start of the input pulse is termed the delay time, t_d . As the base current (I_B) flows, charged carriers accumulate in the base region, and the collector current increases in proportion until it is

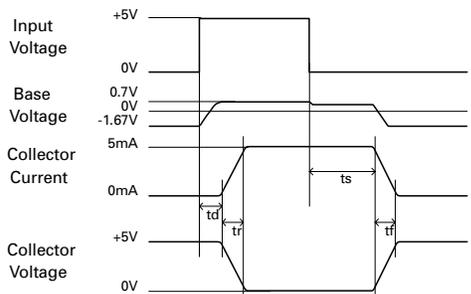


Figure 23.
Bipolar Transistor Switching Waveforms for the Inverter Circuit of Figure 22.

limited by the collector load resistance R_3 . The time taken for the collector current to rise from 10% to 90% of its final value is the rise time, t_r . As the collector voltage approaches zero, the c-b junction becomes forward biased and conducts the excess base current. The base now starts acting as an emitter and begins to inject charge carriers into the collector. This causes a considerable accumulation of charge in the collector region which must be removed, either by recombination or by reverse base current, before the device can begin to turn off. The time taken for this excess charge to be removed is called the storage time (t_s), and during this time the transistor remains saturated. At the end of the storage time all excess charge carriers have been removed and the base charge is simply that required to maintain collector current. As this charge is reduced further the collector current falls in sympathy until the device is cut off. The time taken for the collector current to fall from 90% to 10% is called the fall time, t_f .

Due to the low leakage of silicon transistors, it is not usually necessary to reverse bias the base to ensure DC stability. This does tend to reduce the delay time, but increases the storage and fall times as the stored charge can only be dissipated by recombination instead of by the reverse current provided by R_2 . This can be overcome by including a capacitor in parallel with the base drive resistor, of such value that the charge stored on it is sufficient to neutralise the total charge in the transistor. This value will be dependent on the transistor type, the base and collector currents and the amplitude of

the input or driving pulse. For practical applications it is necessary to determine the required capacitor values by measurement, preferably using a worst case version of the circuit. As a guide, minimum values of turn-off charge have been provided for small signal, switching and high current low $V_{CE(sat)}$ transistors, and are reproduced for various DC conditions within Appendix C. These charts were produced using test circuits similar to that shown in Figure 5. As carrier diffusion coefficients and recombination are temperature dependent, then storage time will also possess this dependence to some degree. Therefore in some circumstances allowance must be made, and component values adjusted accordingly.

The amount of trigger charge necessary for pulse applications can be considered in a similar manner, and for obtaining approximate values the circuit shown in Figure 24 can be employed. The values obtained are higher than for the "speed-up" case as the trigger capacitor not only has to remove the stored charge but also has to overcome the DC bias provided by R_B . In a practical circuit, there may well be additional components, which will absorb some fraction of the trigger charge. Therefore it will usually be necessary to use a higher value of capacitance than measurement (or provided curves) would suggest - it is advised to closely breadboard/model the actual circuit as closely as possible with worst case component values. Figure 25 shows an example oscillograph for the ZTX300 small signal device, and Figure 26 presents curves for the minimum trigger

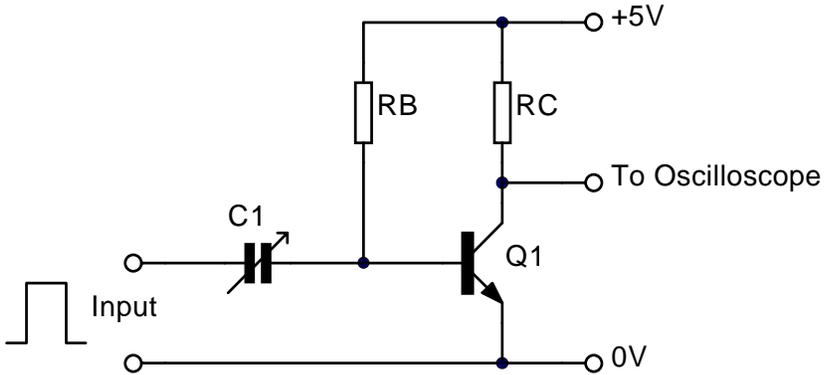


Figure 24.
Circuit to Determine Minimum Value of Trigger Charge for Bipolar Transistor.

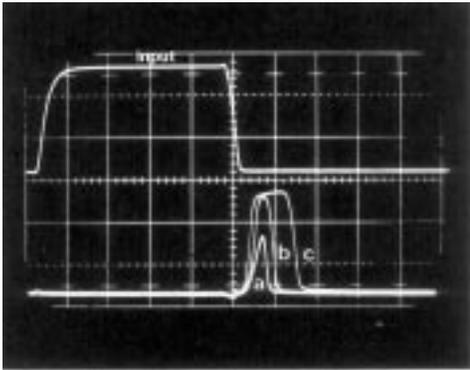
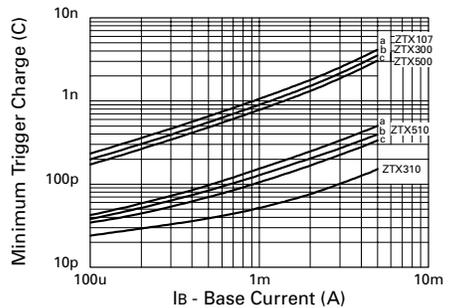


Figure 25.
Trigger Waveforms and Effect of Varying Trigger Capacitance. Upper trace - Input waveform; lower traces - output at collector, (a) Variable capacitor "C1" below critical value, (b) "C1" at critical value with collector voltage rising to 90% of final value, (c) "C1" above critical value. Horizontal scale=200ns/div, Vertical scale=2V/div. ZTX300, $I_B=1\text{mA}$, $I_C=10\text{mA}$.

charge necessary for small signal types ZTX107, ZTX300 and ZTX500, and switching transistors ZTX310 and ZTX510.



Min. Trigger Charge v I_B for Small Signal and Switching Transistors

Figure 26.
Minimum Trigger Charge for Small Signal and Switching Transistors. Forced Gains (I_C/I_B) of : a)10; b)20; c)40. No significant difference observed for different forced gains on the ZTX310 series.

Appendix B References

(References 1, 2 and 3 contain mathematical treatment of charge analysis with respect to switching characteristics of bipolar transistors - similar background can be found in most semiconductor physics books).

1. Switching Transistor Handbook, chapter five - "Transient Characteristics of Transistors". Motorola Inc., Technical Editor William D. Roehr.

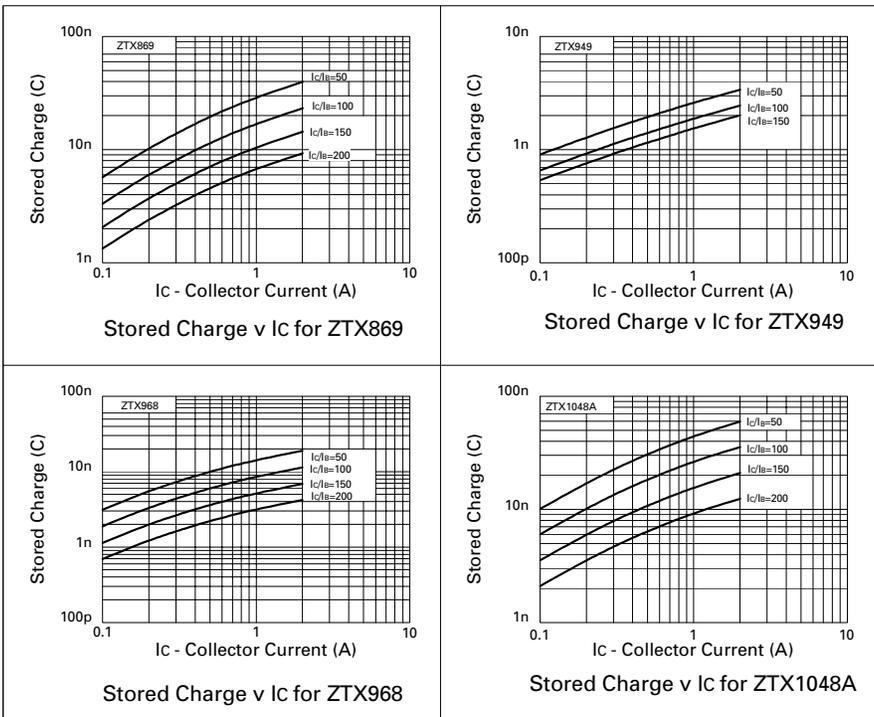
2. Pulse, Digital and Switching Waveforms, Chapter 20 - "Transient Switching Characteristics", Millman and Taub. McGraw-Hill Book Company.

3. Semiconductor Device Technology, section 2.2.26 BJT Modelling - Physical BJT Models, subsection 2) Charge Control BJT Model. Malcolm E. Goodge. MacMillan Press.

4. Switching and Linear Power Supply, Power Converter Design. Abraham I. Pressman. Hayden Press.

Appendix C

Characterisation Charts showing typical stored charge as a function of load current and bias level.



Appendix C (continued)

