Application Note
AP2001 Buck + Boost Converter

Contents

1. AP2001 Specification

1.1 Features

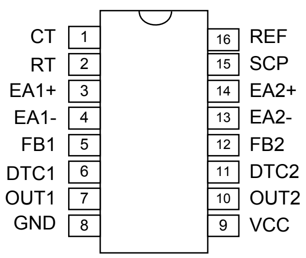
- Dual PWM Control Circuitry
- Operating Voltage can be up to 50V
- Adjustable Dead Time Control (DTC)
- Under Voltage Lockout (UVLO) Protection
- Short Circuit Protection (SCP)
- Variable Oscillator Frequency…500kHz max.
- 2.5V Voltage Reference Output
- 16-pin PDIP and SOP Packages

1.2 General Description

The AP2001 integrates Pulse-Width-Modulation (PWM) control circuit into a single chip, mainly designed for a power-supply regulator. All the functions include an on-chip 2.5V reference output, two error amplifiers, an adjustable oscillator, two dead-time comparators, UVLO, SCP, DTC circuitry, and dual Common-Emitter (CE) output transistor circuit. Recommend the output CE transistors as pre-driver for driving externally. The DTC can provide from 0% to 100%. Switching frequency can be adjustable by trimming RT and CT. During low V_{CC} situation, the UVLO makes sure that the outputs are off until the internal circuit is operating normally.

1.3 Pin Assignments

(Top View)

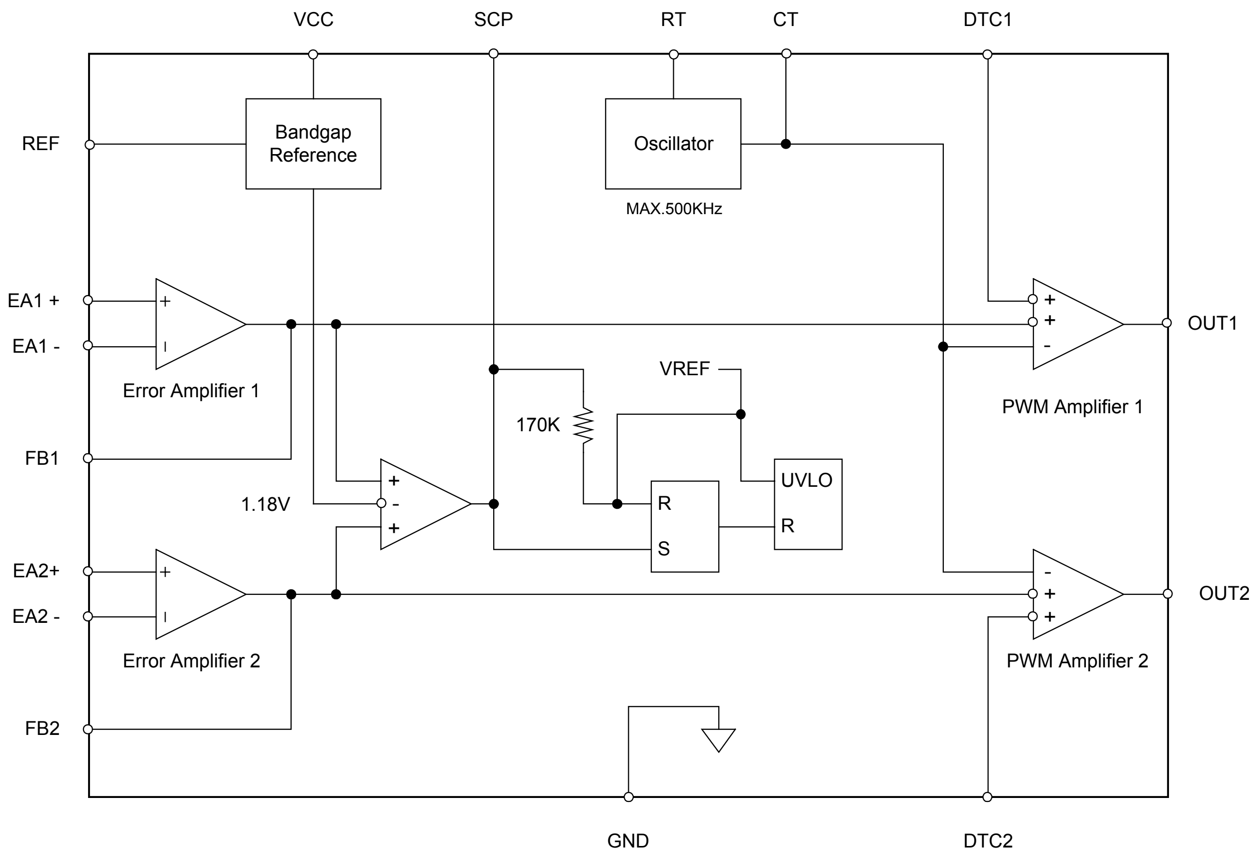


PDIP/SOP

1.4 Pin Descriptions

Name	Description
CT	Timing Capacitor
RT	Timing Resistor
EA+	Error Amplifier Input (+)
EA -	Error Amplifier Input (-)
FB	Feedback Loop Compensation
DTC	Dead Time Control
OUT	Pre-driver Output
GND	Ground
V_{CC}	Supply Voltage
SCP	Short Circuit Protection
REF	Voltage Reference

1.5 Block Diagram



1.6 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	Supply Voltage	40	V
V_I	Amplifier Input Voltage	20	V
V_O	Collector Output Voltage	40	V
I_O	Collector Output Current	21	mA
T_{OP}	Operating Temperature Range	-20 to +85	^oC
T_{ST}	Storage Temperature Range	-65 to +150	^oC
T_{LEAD}	Lead Temperature 1.6mm (1/16 inch) from Case for 10 Seconds	260	^oC

2. Hardware

2.1 Introduction

The Buck + Boost demo board supplies two constant DC output voltages that are 3.3V and 12V. This board can supply output power up to 10W for buck output (3.3V / 3A) and up to 3.6W for boost output (12V / 0.3A). Using a DC input voltage of 5V to 7V, full load efficiency varies from 80 percent to 86 percent depending on the input voltage. This type of converter converts an unregulated input voltage to 2 regulated output voltages where one is always lower than the input voltage and the other is always higher than the input voltage. The control method used in the board is fixed frequency, variable on-time Pulse-Width-Modulation (PWM). The feedback method used is voltage-mode control. Other features of the board include Under Voltage Lockout (UVLO), Short-Circuit Protection (SCP), and adjustable Dead Time Control (DTC).

2.2 Typical Application

The AP2001 may operate in either the CCM (Continuous Conduction Mode) or the DCM (Discontinuous Conduction Mode). The following applications are designed for CCM (Continuous Conduction Mode) operation. That is, the inductor current is not allowed to fall to zero. To compare the disadvantages and advantages for CCM and DCM, the main disadvantage of CCM is the inherent stability problems (caused by the right-half-plane zero and the double pole in the small-signal control to output voltage transfer function). However, the main disadvantage of DCM is that peak currents of switch and diode are larger than CCM when converting. Using power switch and output diode with larger current and power dissipation ratings should solve this issue of large peak current. The designer has to use larger output capacitors, and take more effort on EMI/RFI solution also. The designer could make a choice for each mode. For a low loading current, DCM is preferred for buck and CCM is preferred for boost. If the load current requirement is high, CCM is preferred for buck and DCM is preferred for boost.

- **Buck (Step Down)**

The Buck or Step-down converter converts a DC voltage to a lower DC voltage. *Figure 1* shows the basic buck topology. When the switch SW is turned on, energy is stored in the inductor L and it has constant voltage "$V_L = V_I - V_O$", the inductor current i_L ramps up at a slope determined by the input voltage. Diode D is off during this period. Once the switch, SW, turns off, diode D starts to conduct and the energy stored in the inductor is released to the load. Current in the inductor ramps down at a slope determined by the difference between the input and output voltages.

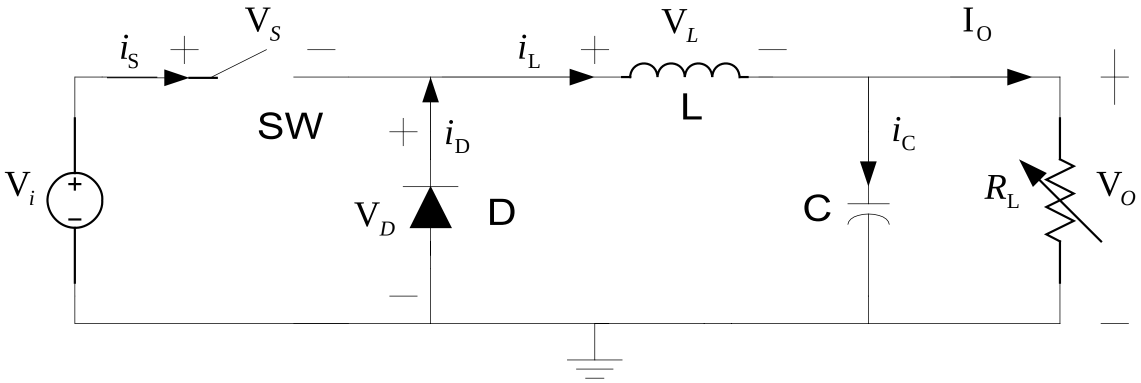


Figure 1. Typical Buck Converter Topology

- **Boost (Step-up)**

The Boost or Step-up converter converts a DC voltage to a higher DC voltage. *Figure 2* shows the basic boost topology. When the switch SW is turned on, energy is stored in the inductor L and the inductor current i_L ramps up at a slope determined by the input voltage. Diode D is off during this period. Once the switch, SW, turns off, diode D starts to conduct and the energy stored in the inductor is released to the load, it has constant voltage "$V_o = V_I + V_L$". Current in the inductor ramps down at a slope determined by the difference Between the input and output voltages.

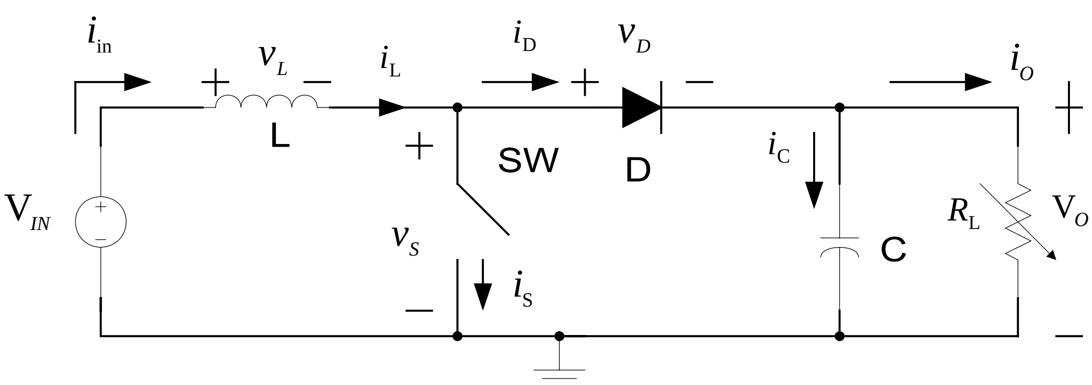


Figure 2. Typical Boost Converter Topology

2.3 Input / Output Connections

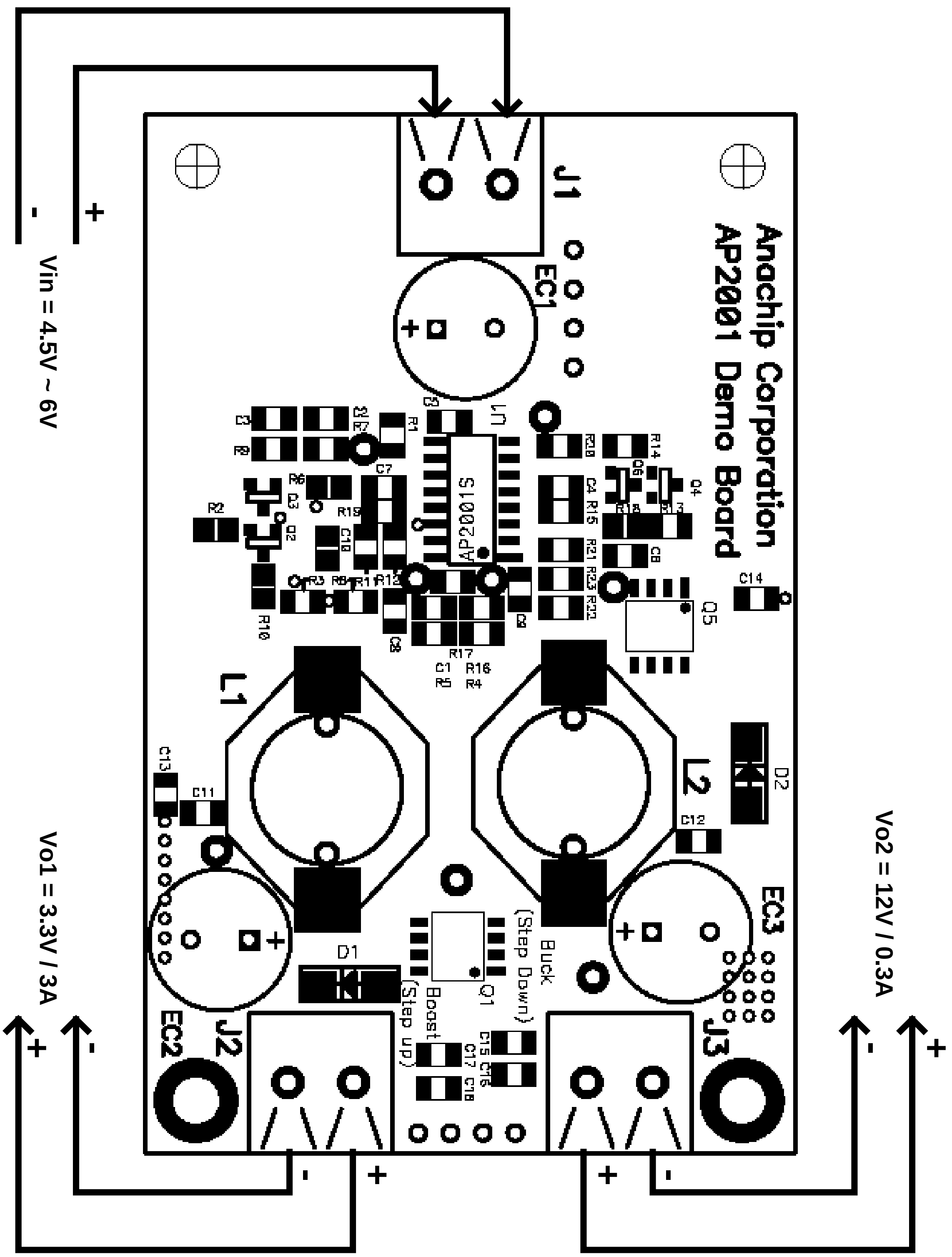


Figure 3. I/O Connections

2.4 Schematic

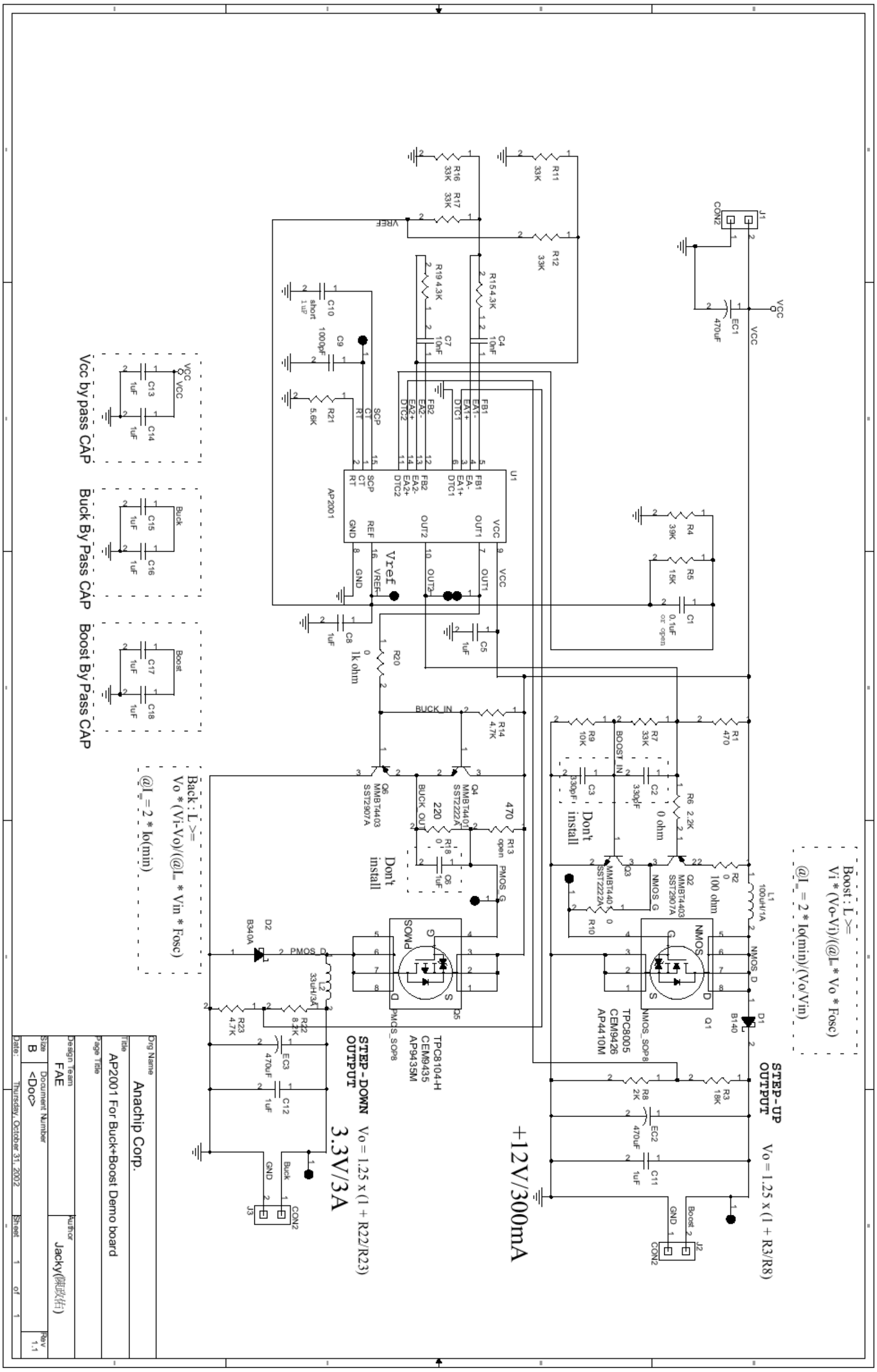


Figure 4. Demo Board Schematic

2.5 Board of Materials

No	Value	Qty	Part Reference	Description	Manufacturers	Part Number
1	0.1uF	1	C1	Ceramic Chip CAP. 0.1uF 25V ±10% K X7R 0805		
2	330pF	2	C2, C3	Ceramic Chip CAP. 330pF 25V ±10% K X7R 0805		
3	10nF	2	C4, C7	Ceramic Chip CAP. 2200pF 25V ±10% K X7R 0805		
4	1uF	10	C5, C6, C8, C11, C12, C13, C14, C15, C16, C17, C18	Ceramic Chip CAP. 1uF 25V ±10% K X7R 0805		
5	1000pF	1	C9	Ceramic Chip CAP. 1000pF 25V ±10% K X7R 0805		
6	short	1	C10	Short		
7	RB160L-40	1	D1	Schottky Diode 1A 40V	DIODES ROHM	B140 RB160L-40
8	B340A	1	D2	Schottky Diode 3A 40V	DIODES	B340A
9	470uF	3	EC1, EC2, EC3	Electrolysis Capacitors		
10	CON2	3	J1, J2, J3	2P PCB Terminal Block	DINKLE	ELK508V-02P
11	100uH/1A	1	L1	TOROID COILS 10uH 1A	Star Electronics	
12	33uH/3A	1	L2	TOROID COILS 33uH 3A	Star Electronics	
13	NMOS_SOP8	1	Q1	N-Channel MOSFET 30V 1A↑	Toshiba CET APEC	TPC8005 CEM9426 AP4410M
14	MMBT4403	2	Q2, Q6	PNP BJT -40V -0.6A SOT-23	ROHM DIODES	SST2907A MMBT4403
15	MMBT4401	2	Q3, Q4	NPN BJT 40V 0.6A SOT-23	ROHM DIODES	SST2222A MMBT4401
16	PMOS_SOP8	1	Q5	P-Channel MOSFET -30V -3A↑	Toshiba CET APEC	TPC8104-H CEM9435 AP9435M
17	470	1	R1	Chip Resistance 470 1/8W ±10% J 0805		
18	0	4	R2, R10, R18, R20	Chip Resistance 0 1/8W ±10% J 0805		
19	18K	1	R3	Chip Resistance 18K 1/8W ±10% J 0805		
20	39K	1	R4	Chip Resistance 39K 1/8W ±10% J 0805		

2.5 Board of Materials (continued)

No	Value	Qty	Part Reference	Description	Manufacturers	Part Number
21	15K	1	R5	Chip Resistance 15K 1/8W ±10% J 0805		
22	2.2K	1	R6	Chip Resistance 2.2K 1/8W ±10% J 0805		
23	33K	5	R7 R11 R12 R16 R17	Chip Resistance 33K 1/8W ±10% J 0805		
24	2K	1	R8	Chip Resistance 2K 1/8W ±10% J 0805		
25	10K	1	R9	Chip Resistance 22K 1/8W ±10% J 0805		
26	open	1	R13	Open		
27	4.7K	2	R14 R23	Chip Resistance 4.7K 1/8W ±10% J 0805		
28	4.3K	2	R15 R19	Chip Resistance 4.3K 1/8W ±10% J 0805		
29	5.6K	1	R21	Chip Resistance 5.6K 1/8W ±10% J 0805		
30	8.2K	1	R22	Chip Resistance 8.2K 1/8W ±10% J 0805		
31	AP2001	1	U1	Monolithic Dual Channel PWM Controller	Anachip	AP2001S

2.6 Board Layout

Board size is 80mm(W) x 50mm(L)

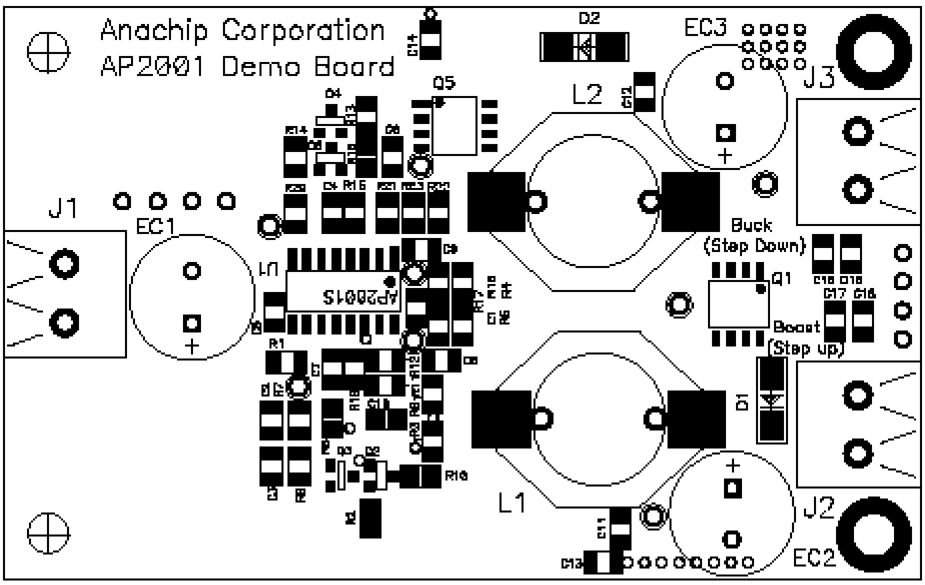


Figure 5. Silkscreen Layer

2.6 Board Layout (continued)

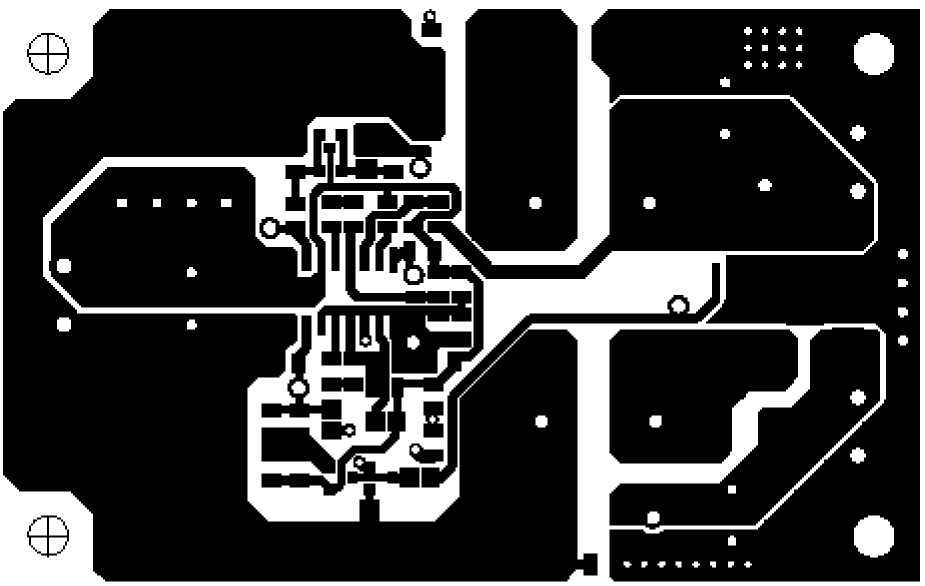


Figure 6. Top Layer

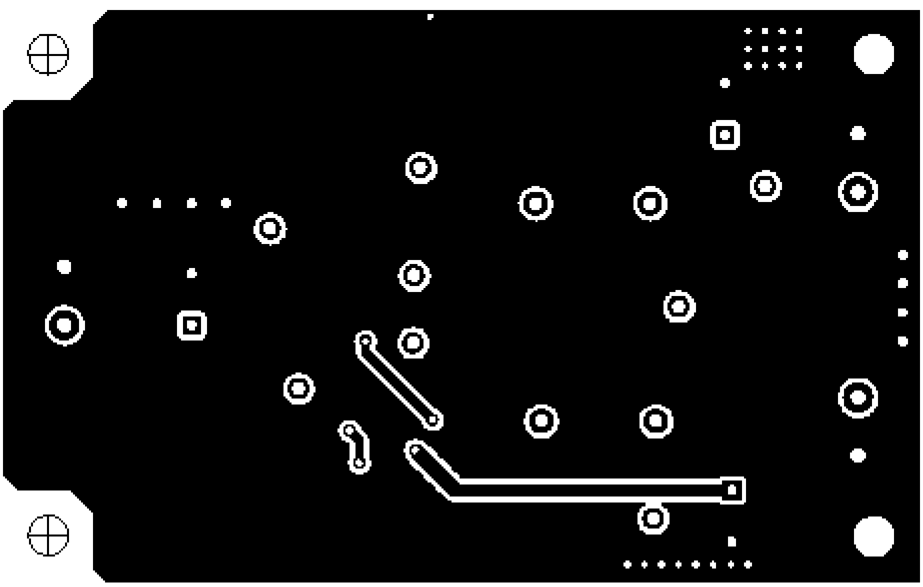


Figure 7. Bottom Layer

3. Design Procedure

3.1 Introduction

The AP2001 integrated circuit is dual PWM controller. It operates over a wide input voltage range. This together with its low cost makes it a very popular choice for use in PWM controllers. This section will describe the AP2001 design procedure. The operation and the design of the buck + boost converter will also be discussed in detail.

3.2 Operating Specifications

Specification	Min.	Typ.	Max.	Units
Input Voltage Range	5	6	7	V
Output (Buck/Boost) Voltage Range	3 / 11	3.3 / 12	3.6 / 13	V
Output Power Range	0	10 / 3.6	18 / 6.5	W
Output Current Range	300 / 50	3000 / 300	5000 / 500	mA
Operating Frequency	100	110	120	kHz
Output Ripple		50		mV
Efficiency	74	80	86	%

Table 1. Operating Specifications

3.3 Design Procedures

This section describes the steps to design continuous-mode buck and boost converter, and explains how to construct basic power conversion circuits including the design of the control chip functions and the basic loop. A switching frequency of 110 kHz was chosen.

3.3.1 Buck Converter

Example calculations accompany the design equations. Since this is a fixed output converter, all example calculations apply to the converter with an output voltage of 3.3V and input voltage set to 6V, unless specified otherwise. The first quantity to be determined is the converter of the duty cycle value:

$$\text{Duty ratio } D = \frac{V_o + V_d}{V_{in} - V_{ds(sat)}} = \frac{T_{on}}{T_s} \quad , \quad 0 \le D \le 1$$

Assuming the commutating diode forward voltage V_d = 0.5V and the power switch on voltage $V_{ds(sat)}$ = 0.1V, the duty cycle for V_{in} = 5, 6 and 7 is 0.78, 0.64 and 0.55, respectively.

3.3.1.1 Selection of the Buck Inductor (L)

A buck converter uses a single-stage LC filter. Choose an inductor to maintain continuous-mode operation down to 10 percent ($I_{o(min)}$) of the rated output load:

$$\Delta I_L = 2 \times 10\% \times I_o = 2 \times 0.1 \times 3 = 0.6A$$

The inductor “L” value is:

$$L \ge \frac{(V_{in} - V_{ds(sat)} - V_o) \times D_{min}}{\Delta I_L \times f_s} = \frac{(7 - 0.1 - 3.3) \times 0.55}{0.6 \times (110 \times 10^3)} = 30\mu H$$

So we can choose 33μH.

3.3.1.2 Selection of the Output Capacitor (C_{out})

Assuming that all of the inductor ripple current flows through the capacitor and the effective series resistance (ESR) is zero, the capacitance needed is:

$$C_{out} \geq \frac{\Delta I_L}{8 \times f_s \times \Delta V_o} = \frac{0.6}{8 \times (110 \times 10\text{^}3) \times 0.05} = 13.6\mu F$$

Assuming the capacitance is very large, the ESR needed to limit the ripple to 50 mV is:

$$ESR \leq \frac{\Delta V_o}{\Delta I_o} = \frac{0.05}{0.6} = 0.083\Omega$$

The output filter capacitor should be rated at least ten times the calculated capacitance and 30–50 percent lower than the calculated ESR. This design used a 470-μF/25V OS-Con capacitor in parallel with a ceramic to reduce ESR.

3.3.1.3 Selection of the Power Switch (MOSFET)

Based on the preliminary estimate, $R_{DS(on)}$ should be less than 0.10 V ÷ 3A = 33mΩ. The **CEM4435** (*CET*) is a -30V p-channel MOSFET with $R_{DS(on)}$ = 35mΩ. Power dissipation (conduction + switching losses) can be estimated as:

$$P_{MOSFET} = I_o\text{^}2 \times R_{ds(on)} \times D_{max} + [0.5 \times V_{in} \times I_o \times (t_r + t_f) \times f_s]$$

Assuming total switching time (t_r + t_f) is 300 ns, a 55°C maximum ambient temperature, and thermal impedance $R_{\theta JA}$ = 50°C/W, thus:

$$P_{MOSFET} = (3 \times 3 \times 0.035 \times 0.78) + [0.5 \times 5 \times 3 \times (0.3 \times 10\text{^}(-6)) \times (110 \times 10\text{^}3) = 0.5W$$

$$T_J = T_A + (R_{\theta JA} \times P_{MOSFET}) = 55 + (50 \times 0.5) = 80°C$$

3.3.1.4 Selection of the Rectifier (D)

The catch rectifier conducts during the time interval when the MOSFET is off. The **B340** (*DIODES*) is a 3A, 40V Schottky Rectifier in an SMC power surface-mount package. The power dissipation is:

$$P_D = I_o \times V_d \times (1 – D_{min}) = 3 \times 0.5 \times (1 – 0.55) = 0.675W$$

Assuming a 55°C maximum ambient temperature, and thermal impedance $R_{\theta JA}$ = 15°C/W, thus:

$$T_J = T_A + (R_{\theta JA} \times P_D) = 55 + (15 \times 0.675) = 65.125°C$$

3.3.1.5 Selection of the Input Capacitor (C_{in})

The RMS current rating of the input capacitor can be calculated from the following formula. The capacitor manufacturers datasheet must be checked to assure that this current rating is not exceeded.

$I_{in(rms)} = \sqrt{[D \times (I_{o(max)} + I_{o(min)}) \times (I_{o(max)} - I_{o(min)}) + (\Delta I_L\text{^}2)/3]} = \sqrt{[0.78 \times (3 + 0.3) \times (3 – 0.3) + 0.36/3]} = 2.67A$

This capacitor should be located close to the IC using short leads and the voltage rating should be approximately 2 times the maximum input voltage. The input capacitor value is “470UF/25V”.

3.3.2 Boost Converter

Example calculations accompany the design equations. Since this is a fixed output converter, all example calculations apply to the converter with output voltage 12V and input voltage set to 6V, unless specified otherwise. The first quantity to be determined is the converter duty cycle value:

$$\text{Duty ratio } D = \frac{V_o + V_d - V_{in(min)}}{V_o + V_d - V_{ds(sat)}} = \frac{T_{on}}{T_s} \quad , \quad 0 \le D \le 1$$

Assuming the commutating diode forward voltage V_d = 0.5 V and the power switch on voltage $V_{ds(sat)}$ = 0.1V, the duty cycle for V_{in} = 5, 6 and 7 is 0.60, 0.52 and 0.44, respectively.

3.3.2.1 Selection of the Boost Inductor (L)

The boost inductor, converter switching frequency, input and output voltages, and output power determine a boost converter’s operating mode. This converter operates in the CCM (Continuous Conduction Mode). In continuous mode, the inductor current is not allowed to fall to zero. The peak-to-peak inductor current ripple is listed below:

$$\Delta I_L = 2 \times I_{o(min)} \times \frac{V_o}{V_{in(min)}} = 2 \times 0.05 \times \frac{12}{5} = 0.24$$

The inductor “L” value is:

$$L \ge \frac{V_{in(min)} – V_{ds(sat)} \times D_{max}}{\Delta I_L \times f_s} = \frac{(5 – 0.1) \times 0.6}{0.24 \times (110 \times 10\text{^}3)} = 111.36\mu H$$

So we can choose 120µH.

3.3.2.2 Selection of the Output Capacitor (C_{out})

Assuming that all of the inductor ripple current flows through the capacitor and the effective series resistance (ESR) is zero, the capacitance needed is:

$$C_{out} \geq \frac{I_{o(max)} \times D_{max}}{f_s \times \Delta V_o} = \frac{0.3 \times 0.6}{110k \times 0.05} = 32.73\mu F$$

Assuming the capacitance is very large, the ESR needed to limit the ripple to 50 mV is:

$$Ipk = \frac{I_{o(max)}}{1 - D_{max}} + \frac{V_{in(max)} \times D}{2 \times f_s \times L} = \frac{0.3}{1 - 0.6} + \frac{7 \times 0.6}{2 \times 110k \times 120\mu} = 0.91A$$

$$ESR \leq \frac{\Delta V_o}{I_{pk}} = \frac{0.05}{0.91} = 55m\Omega$$

The output filter capacitor should be rated at least two to three times the calculated capacitance and 30 to 50 percent lower than the calculated ESR. This design used a 470-μF/25V OS-Con capacitor in parallel with a ceramic to reduce ESR.

3.3.2.3 Selection of Power Switch (MOSFET)

The design uses an n-channel power MOSFET to simplify the drive-circuit design and minimize component count. Based on these calculations, the drain current rating should be chosen for 0.91A. The drain-to-source breakdown rating should be appropriate for the 20V applied to the device during the off time. A surface mount packaging is also recommended. The CEM9426 (CET) power MOSFET is a 20V n-channel MOSFET in a power surface mount package (SO-8) with an $I_{D(MAX)}$ rating of 10A.

$$P_{MOSFET} = I_{pk}\text{^}2 \times R_{ds(on)} \times D_{max} + [0.5 \times V_{in(max)} \times I_{pk} \times (t_r + t_f) \times f_s]$$

Assuming total switching time ($t_r + t_f$) is 300 ns, a 55°C maximum ambient temperature, and thermal impedance $R_{\theta JA}$ = 50°C/W, thus:

$$P_{MOSFET} = 0.91 \times 0.91 \times 0.0135 \times 0.6 + [0.5 \times 7 \times 0.91 \times 0.3\mu \times 110k = 0.112W$$

$$T_J = T_A + (R_{\theta JA} \times P_D) = 55 + (50 \times 0.112) = 60.6°C$$

3.3.2.4 Selection of Power Rectifier (D)

The catch rectifier conducts during the time interval when the MOSFET is off. The **B140**(*DIODES*) is a 1A, 40V Schottky rectifier in an SMC power surface-mount package. The power dissipation is:

$$P_D = I_{pk} \times V_d = 0.91 \times 0.5 = 0.455W$$

Assuming a 55°C maximum ambient temperature, and thermal impedance $R_{\theta JA}$ = 15°C/W, thus:

$$T_J = T_A + (R_{\theta JA} \times P_D) = 55 + (15 \times 0.455) = 61.825°C$$

3.3.2.5 Selection of the Input Capacitor (C_{in})

In boost switching regulators, triangular ripple current is drawn from the supply voltage due to the switching action. This appears as noise on the input line. This problem is less severe in boost converters due to the presence of inductor in series with the input line. Select the input capacitor for:

$$I_{in(rms)} = \frac{I_{pk}}{\sqrt{(12)}} = \frac{0.91}{\sqrt{(12)}} = 0.263A$$

This capacitor should be located close to the IC using short leads and the voltage rating should be approximately 2 times the maximum input voltage. We select an input capacitor value of "470UF/25V".