ANP001

Application Note
Application of the AP34063 Switching Regulator Control Circuits

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Application Note
Application of the AP34063 Switching Regulator Control Circuits

This paper describes the principle of the AP34063 switching regulator subsystems. Three converter design examples and application circuits with test data are included.

1.0 Introduction

The AP34063 is monolithic switching regulator subsystems intended for as dc to dc converters. The device has highly efficient and simple switching power supplies. The use of switching regulator is becoming more pronounced over that of linear regulators because the size reductions in new equipment designs require greater conversion efficiency. Another major use of the switching regulator is that it has flexibility of output voltage. The output can be less than, greater than, or of opposite polarity to that of the input voltage.

2.0 Principle of Operation

The switching regulator consists of a static reference and a high gain error amplifier identical to that of the linear regulator. This system added a free running oscillator and a gated latch. The error amplifier again monitors the output voltage, compares it to the reference level and generates a control signal. If the output voltage is below nominal, the control signal will go to a high state and turn on the gate, thus allowing the oscillator clock pulses to drive the series-pass element alternately from cutoff to saturation. This will continue until the output voltage is pumped up slightly above its nominal value. At this time, the control signal will go low and turn off the gate, terminating any further switching of the series-pass element. The output voltage will eventually decrease to below nominal due to the presence of an external load, and will initiate the switching process again. The increase in conversion efficiency is primarily due to the operation of the series-pass element only in the saturated or cutoff state. When saturated, the voltage drop across the element is as small as the dissipation. When in cutoff, the current through the element and likewise the power dissipation are also small. The most common are the fixed frequency pulse width modulator and the fixed on-time variable off-time types, where the on-off switching is uninterrupted and regulation is achieved by duty cycle control. Generally speaking, the example given in Figure 1 does apply to AP34063.

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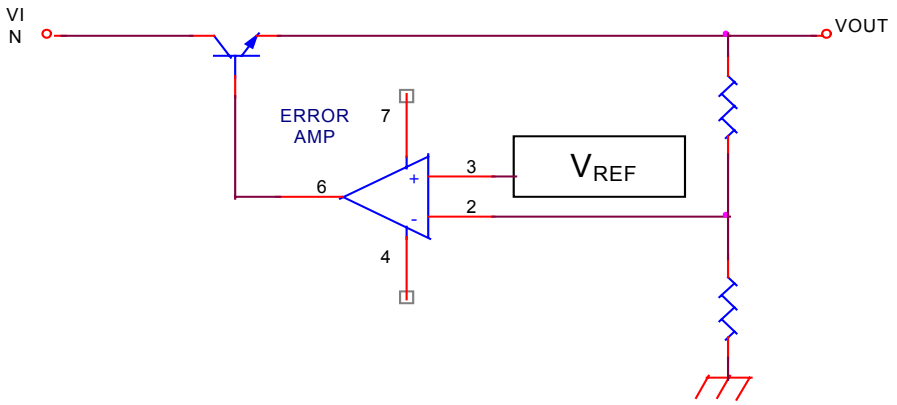
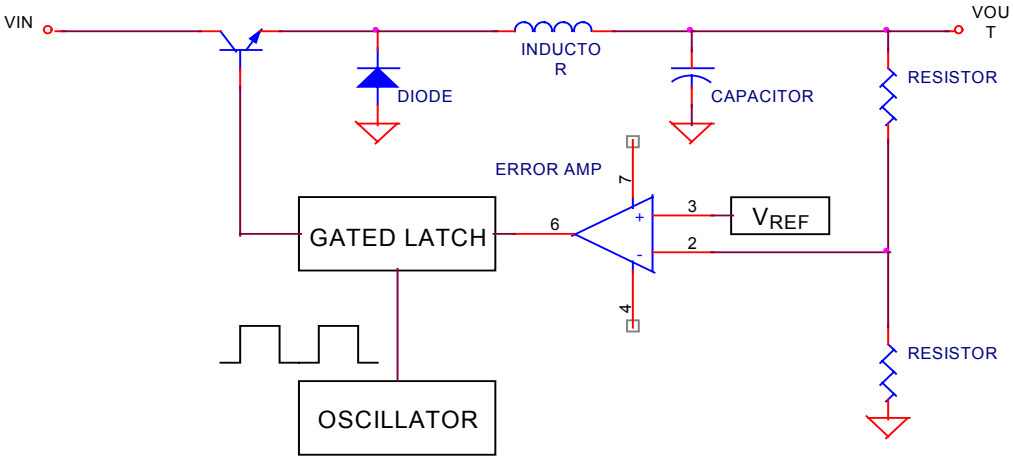


A. Linear Regulator



B. Switching Regulator

Figure 1. Step-Down Regulators

3.0 General Description

The AP34063 is a monolithic control circuit containing all the active functions required for dc to dc converters. This device contains an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active peak current limit circuit, driver, and a high current output switch. This series was specifically designed to be incorporated in step-up, step-down and voltage-inverting converter applications. These functions are contained in an 8 pin dual in-line package shown in Figure 2.

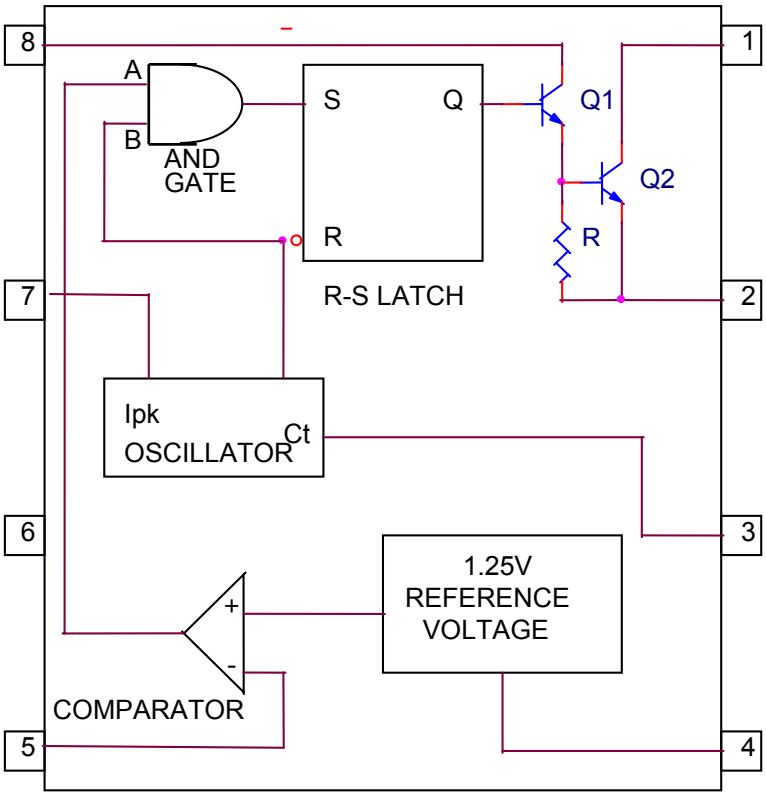


Figure 2. AP34063

4.0 Functional Description

The oscillator is composed of a current source and sink which charges and discharges the external timing capacitor C_T. The typical charge and discharge current are 35μA and 200uA respectively, yielding about 1 to 6 ratio. The ramp-up period is 6 times longer than ramp-down period as shown in Figure 3. The upper threshold is equal to the internal reference voltage 1.25V and the lower is close to 0.75V. The oscillator runs continuously at a rate controlled by the selected value of capacitor C_T.

During the ramp-up portion of the cycle, a “HIGH” present at the ‘A’ input of the AND gate. If the output voltage of the switching regulator is below nominal, a “HIGH” will also be present at the ‘B’ input. This condition will set the latch and cause the ‘Q’ output to go “HIGH”, enabling the driver and output switch to conduct. When the oscillator reaches its upper threshold, C_T will start to discharge and “LOW” will be present at the ‘A’ input of the AND gate. This logic level is also connected to an inverter whose output presents a “HIGH” to the reset input of the latch. This condition will cause ‘Q’ to go “LOW”, disabling the driver and output switch.

The output of the comparator can set the latch only during the ram-up of C_T and can initiate a partial or full on-cycle of output switch conduction. The comparator sets the latch, but it cannot reset the latch. The latch will remain set until C_T begins ramping down. Thus the comparator can initiate output switch conduction, but cannot terminate it and the latch is always reset when C_T begins ramping down. The comparator’s output will be “LOW” when the output voltage of the switching regulator is above nominal.

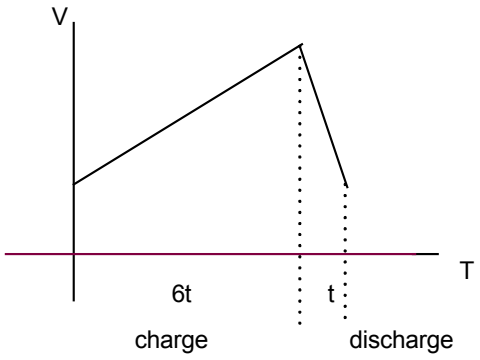


Figure 3. Ct Voltage Charge-Discharge Waveform

5.0 Step-Down Switching Regulator Design Example

A schematic of the basic step-down regulator is shown in Figure 4. The frequency chosen is a comprisal between switching losses and inductor size. Given are the following conditions:

V_{out} = 5.0V
I_{out} = 500mA
f_{min} = 50KHz
V_{in} = 12V~16V
$V_{ripple(p-p)}$ = 50mVp-p

5.0.1 Determine the ratio of switch conductor t_{on} versus diode conduction t_{off} time.

$$\frac{ton}{toff} = \frac{Vout + VF}{Vin - Vsat - Vout}$$
$$= \frac{5 + 0.8}{12 - 1.4 - 5} \quad \text{..... (1)}$$
$$= 1.036$$

5.0.2 The cycle of the LC network is equal to $t_{on(max)} + t_{off}$.

$$ton + toff = \frac{1}{fmin} = \frac{1}{50 \times 10^{3}} \quad \text{..... (2)}$$
$$= 20\ \mu s \text{ per cycle}$$

5.0.3 Using equation (1) and equation (2), we can obtain T_{on} and T_{off} time respectively.

$$toff = \frac{ton + toff}{\frac{ton}{toff} + 1}$$
$$= \frac{20 \times 10^{-6}}{1.036 + 1} \quad \text{..... (3)}$$
$$= 9.8\ \mu s$$

Since $ton + toff = 20\ \mu s$

$$ton = 20 - 9.8 = 10.2\ \mu s \quad \text{..... (4)}$$

5.0.4 The t_{on} is set by selecting a value for C_T

$$C_T = 4.0 \times 10^{-5} \times t_{on}$$
$$= 4.0 \times 10^{-5}(10.2 \times 10^{-6}) = 408\text{pF} \quad \text{..... (5)}$$

Use a standard 470pF capacitor.

5.0.5 The circuit works in Continuous-Conduction Mode (CCM), so the peak switch current in inductance is:

$$I_{pk} = 2I_{out}$$
$$= 2(500\text{mA}) \quad \text{..... (6)}$$
$$= 1\text{A}$$

5.0.6 By using the peak switch current and on time, a minimum value of inductance can be calculated.

$$L_{(min)} = \frac{V_{in(min)} - V_{sat} - V_{out}}{I_{pk}} \times t_{on} \quad \text{..... (7)}$$
$$= \left(\frac{12 - 1.4 - 5}{1}\right) \times 10.2 \times 10^{-6}$$
$$= 57\mu\text{H}$$

Since the minimum value of inductance is 57μH, we use 100μH for the inductance.

5.0.7 The current limit resistor R_{SC} can be determined by using the peak switch current when V_{in} = 24V.

$$I'_{pk} = \frac{V_{in} - V_{sat} - V_{out}}{L} \times t_{on}$$
$$= \left(\frac{16 - 1.4 - 5}{100 \times 10^{-6}}\right) \times 10.2 \times 10^{-6}$$
$$= 0.98\text{A}$$
$$R_{SC} = \frac{0.33}{I_{pk}}$$
$$= \frac{0.33}{0.98} \quad \text{..... (8)}$$
$$= 0.33\Omega$$

5.0.8 With knowledge of the peak switch current, minimum operation frequency, and the peak to peak voltage of the ripple, an ideal output filter capacitor can be obtained.

$$C_{out} = \frac{I_{pk}}{8V_{ripple(p-p)}f_{(min)}}$$

$$= \frac{1}{8(50\times10^{-3})(50\times10^{3})} \quad \text{..... (9)}$$

$$= 50\mu F$$

In order to suppress the output voltage of ripple under 40mV, we choose 470μF for this capacitor. If you want the lowest output voltage of the ripple, consider using the lowest ESR of capacitor you used now.

5.0.9 The output voltage is programmed by the R1, R2 resistors divider. The output voltage is:

$$V_{out} = 1.25\left(1+\frac{R2}{R1}\right) \quad \text{..... (10)}$$

Since the divider current can go as low as 100μA without affecting system performance, a minimum current divider R1 is equal to:

$$R1 = \frac{1.25}{100\mu A} = 12500\Omega = 12.5K\Omega$$

We choose R1 = 12KΩ.
Using equation (10), R2 can be solved:

$$R2 = R1\left(\frac{V_{out}}{1.25}-1\right)$$

$$= 12\times10^{3}\left(\frac{5}{1.25}-1\right)$$

$$= 36K\Omega$$

Using the above derivation, the design circuit is optimized to meet the assumed conditions.

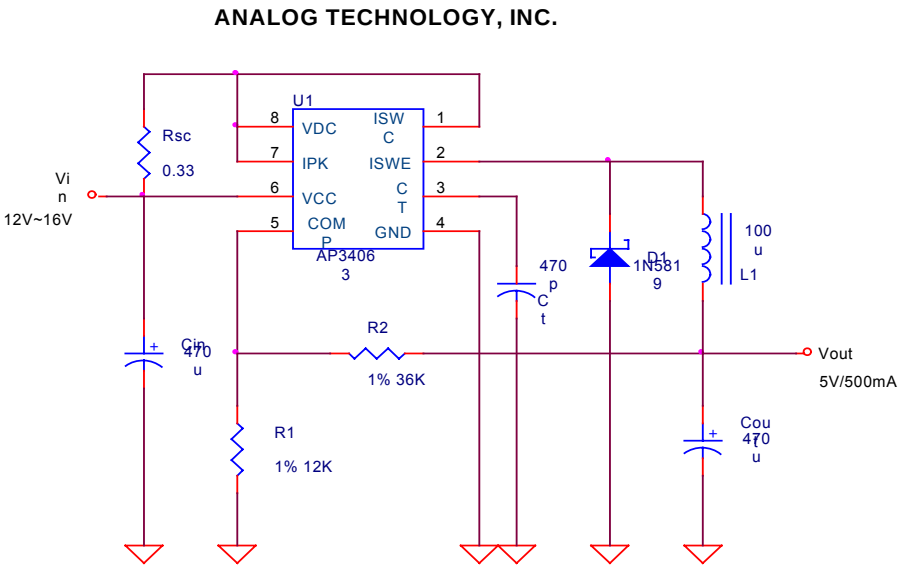


Figure 4

6.0 Step-Up Switching Regulator Design Example

A schematic of the basic step-down regulator is shown in Figure 5. Given are the following conditions:

V_{out} = 28V
I_{out} = 200mA
f_{min} = 50KHz
V_{in} = 9.0V~12.0V
$V_{ripple(p-p)}$ = 40mVp-p

6.0.1 Determine the ratio of switch conductor t_{on} versus diode conduction t_{off} time.

$$\frac{ton}{toff} = \frac{Vout + V_F - V_{in(min)}}{V_{in(min)} - Vsat}$$

$$= \frac{28 + 0.8 - 9}{9 - 0.8} \qquad \text{..... (11)}$$

$$= 2.41$$

6.0.2 The cycle of the LC network is equal to $t_{on(max)} + t_{off}$.

$$t_{on} + t_{off} = \frac{1}{f_{min}} = \frac{1}{50 \times 10^3} \quad \text{..... (12)}$$
$$= 20\,\mu s \text{ per cycle}$$

6.0.3 Using equation (11) and equation (12), we can obtain T_{on} and T_{off} time respectively.

$$t_{off} = \frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$$
$$= \frac{20 \times 10^{-6}}{2.41 + 1} \quad \text{.....(13)}$$
$$= 5.87\,\mu s$$

Since $t_{on} + t_{off} = 20\,\mu s$

$$t_{on} = 20 - 5.87 = 14.13\,\mu s \quad \text{..... (14)}$$

6.0.4 The t_{on} is set by selecting a value for C_T

$$C_T = 4.0 \times 10^{-5} \times t_{on}$$
$$= 4.0 \times 10^{-5}(14.13 \times 10^{-6}) = 565.2pF \text{ .....(15)}$$

Use a standard 680pF capacitor.

6.0.5 The circuit works in Continuous-Conduction Mode (CCM), so the peak switch current in inductance is:

$$I_{pk} = 2 I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$$
$$= 2\,(200mA)(2.41 + 1) \quad \text{..... (16)}$$
$$= 1.364A$$

6.0.6 By using the peak switch current and on time, a minimum value of inductance can be calculated.

$$L_{(min)} = \frac{V_{in(min)} - V_{sat}}{I_{pk}} \times t_{on}$$
$$= \left(\frac{12 - 0.8}{1.364}\right) \times 14.13 \times 10^{-6} \quad \text{..... (17)}$$
$$= 116\,\mu H$$

Since the minimum value of inductance is 116μH, we use 120μH for the inductance.

6.0.7 The current limit resistor R_{SC} can be determined by using the peak switch current when V_{in} = 12V.

$$I_{pk} = \frac{V_{in} - V_{sat}}{L} \times t_{on}$$

$$= \left(\frac{12 - 0.8}{120 \times 10^{-6}} \right) \times 14.13 \times 10^{-6}$$

$$= 1.32A$$

$$R_{SC} = \frac{0.3}{I_{pk}}$$

$$= \frac{0.3}{1.32} \quad \text{..... (18)}$$

$$= 0.22\Omega$$

6.0.8 With knowledge of the peak switch current, minimum operation frequency, and the peak to peak voltage of the ripple, an ideal output filter capacitor can be obtained.

$$C_{out} = \frac{I_{out}}{V_{ripple(p-p)} f_{(min)}}$$

$$= \frac{200 \times 10^{-3}}{(40 \times 10^{-3})(50 \times 10^{3})} \text{.....(19)}$$

$$= 100 \mu F$$

In order to suppress the output voltage of the ripple under 40mV, we choose 470μF for this capacitor. If you want the lowest output voltage of the ripple, consider using the lowest ESR of capacitor you used now.

6.0.9 The output voltage is programmed by the R1, R2 resistors divider. The output voltage is:

$$V_{out} = 1.25\left(1+\frac{R2}{R1}\right) \quad \text{..... (20)}$$

Since the divider current can go as low as 500μA without affecting system performance, a minimum current divider R1 is equal to:

$$R1 = \frac{1.25}{500\mu A} = 2500\Omega = 2.5K\Omega$$

We choose R1 = 2.5KΩ.
Using equation (20), R2 can be solved:

$$R2 = R1\left(\frac{V_{out}}{1.25}-1\right)$$
$$= 2.5\times10^{3}\left(\frac{28}{1.25}-1\right)$$
$$= 53.5K\Omega \ \left(\text{use } 53K\Omega \text{ or } 54K\Omega\right)$$

Using the above derivation, the design circuit is optimized to meet the assumed conditions.

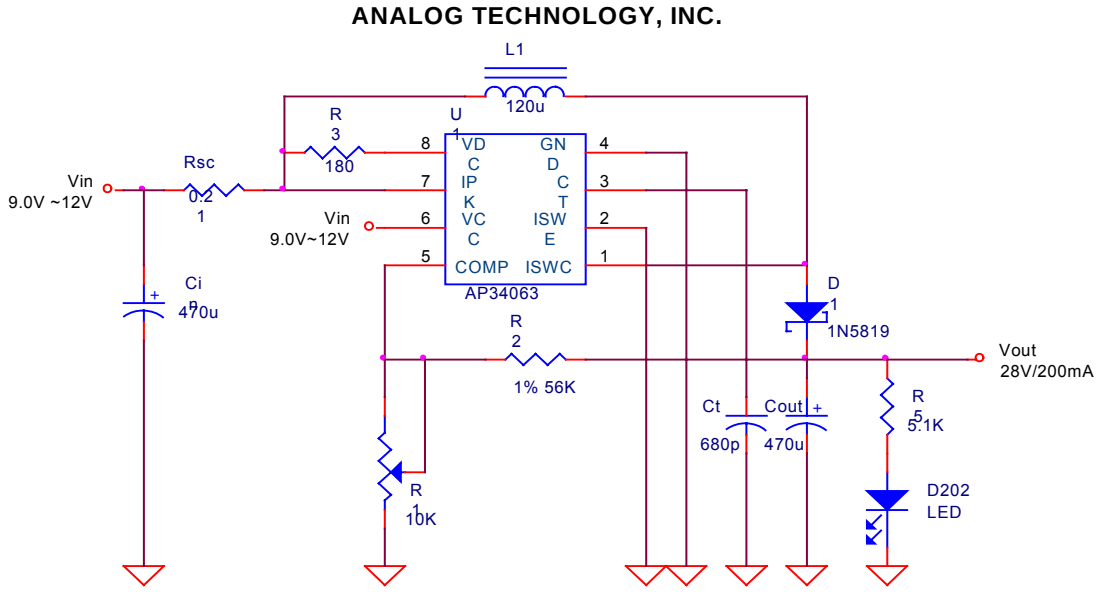


Figure 5

7.0 Voltage-Inverting Switching Regulator Design Example

A schematic of the basic voltage-inverting regulator is shown in Figure 6. The frequency chosen is a comprisal between switching losses and inductor size. Given are the following conditions:

$$\begin{aligned} V_{out} &= -12V \\ I_{out} &= 100mA \\ f_{min} &= 50KHz \\ V_{in} &= 4.5V\sim6.0V \\ V_{ripple(p-p)} &= 40mVp\text{-}p \end{aligned}$$

7.0.1 Determine the ratio of switch conductor t_{on} versus diode conduction t_{off} time.

$$\frac{ton}{toff} = \frac{|V_{out}| + V_F}{V_{in} - V_{sat}} = \frac{12 + 0.8}{4.5 - 0.8} = 3.46 \quad \text{..... (21)}$$

7.0.2 The cycle of the LC network is equal to $t_{on(max)} + t_{off}$

$$ton + toff = \frac{1}{fmin} = \frac{1}{50 \times 10^3} = 20\mu s \text{ per cycle} \quad \text{..... (22)}$$

7.0.3 Using equation (21) and equation (22), we can obtain T_{on} and T_{off} time respectively.

$$toff = \frac{ton + toff}{\frac{ton}{toff} + 1} = \frac{20 \times 10^{-6}}{3.46 + 1} = 4.48\mu s \quad \text{..... (23)}$$

Since $ton + toff = 20\mu s$

$$ton = 20 - 4.48 = 15.52\ \mu s \quad \text{.....(24)}$$

7.0.4 The t_{on} is set by selecting a value for C_T

$$C_T = 4.0 \times 10^{-5} \times t_{on}$$
$$= 4.0 \times 10^{-5}(15.52 \times 10^{-6}) = 620.8\text{pF} \quad \text{..... (25)}$$

Use a standard 680pF capacitor.

7.0.5 The circuit works in Continuous-Conduction Mode (CCM), so the peak switch current in inductance is:

$$I_{pk} = 2I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$$
$$= 2(100\text{mA})(3.46 + 1) \quad \text{..... (26)}$$
$$= 0.892\text{A}$$

7.0.6 By using the peak switch current and on time, a minimum value of inductance can be calculated.

$$L_{(min)} = \frac{V_{in(min)} - V_{sat}}{I_{pk}} \times t_{on}$$
$$= \left(\frac{4.5 - 0.8}{0.892}\right) \times 15.52 \times 10^{-6} \quad \text{..... (27)}$$
$$= 64\mu\text{H}$$

Since the minimum value of inductance is 64μH , we use 100μH for the inductance.

7.0.7 The current limit resistor R_{SC} can be determined by using the peak switch current when V_{in} = 6.0V.

$$I_{pk} = \frac{V_{in} - V_{sat}}{L_{min}} \times t_{on}$$
$$= \left(\frac{6.0 - 0.8}{64 \times 10^{-6}}\right) \times 15.52 \times 10^{-6}$$
$$= 1.261$$
$$R_{SC} = \frac{0.33}{I_{pk}}$$
$$= \frac{0.33}{1.261} \quad \text{..... (28)}$$
$$= 0.26\Omega$$

7.0.8 With knowledge of the peak switch current, minimum operation frequency, and the peak to peak voltage of the ripple, an ideal output filter capacitor can be obtained.

$$C_{out} = \frac{I_{out}}{V_{ripple(p-p)} f_{(min)}}$$
$$= \frac{100 \times 10^{-3}}{(40 \times 10^{-3})(50 \times 10^{3})} \quad \text{..... (29)}$$
$$= 50 \mu F$$

In order to suppress the output voltage of ripple under 40mV, we choose 470μF for this capacitor. If you want the lowest output voltage of ripple, consider using the lowest ESR of capacitor you used now.

7.0.9 The output voltage is programmed by the R1, R2 resistors divider. The output voltage is:

$$\left|V_{out}\right| = 1.25\left(1 + \frac{R2}{R1}\right) \quad \text{.....(30)}$$

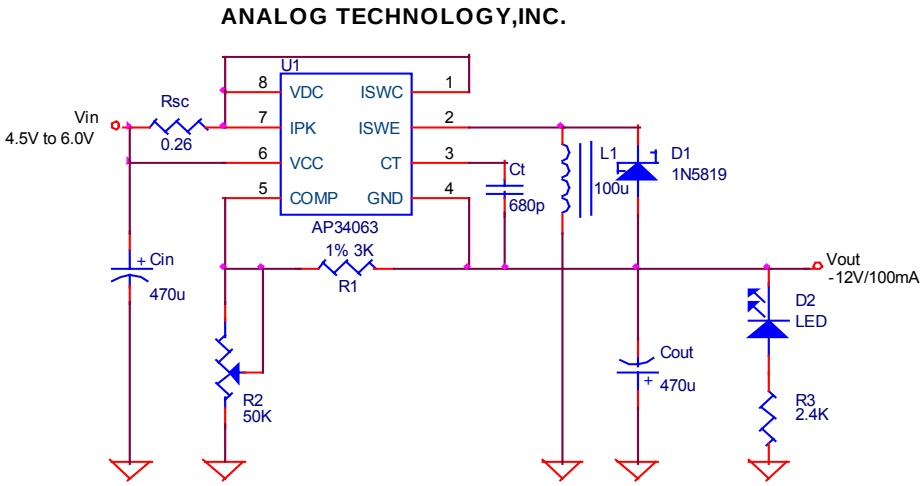
Since the divider current can go as low as 400μA without affecting system performance, a minimum current divider R1 is equal to:

$$R1 = \frac{1.25}{400 \mu A} = 31250\Omega = 3.125K\Omega$$

We choose R1 = 3KΩ.
Using equation (30), R2 can be solved:

$$R2 = R1\left(\frac{\left|V_{out}\right|}{1.25} - 1\right)$$
$$= 3 \times 10^{3}\left(\frac{12}{1.25} - 1\right)$$
$$= 25.8K\Omega \ \left(\text{use } 26K\Omega\right)$$

Using the above derivation, the design circuit is optimized to meet the assumed conditions.



VOLTAGE INVERTING CONVERTER

Figure 6