Design Consideration with AP3440

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1. Introduction

The AP3440 are current mode, PWM synchronous step-down DC-DC converters, capable of driving a 4A load with high efficiency, excellent line and load regulation.

The AP3440 integrate two N-channel MOSFETs with low on-resistance, which allows for high efficiency power supply designs with continual output currents up to 4A. The reference voltage of AP3440 is 0.803V.

The switching frequency of AP3440 can be programmable from 200kHz to 2MHz, which can realize efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor connected to ground on the RT/CLK pin. The RT/CLK pin can be used to synchronize the power switch with a falling edge of an external system clock.

The under voltage lockout of AP3440 is internally set at 2.6V, and can be increased by programming the threshold with a resistor network on the enable pin. The output voltage ramp is controlled by the soft-start pin. An open drain power good signal indicates the output is within 93% to 107% of its nominal voltage.

2. Operation

The AP3440 consists of a reference voltage module, slope compensation circuit, error amplifier, PWM comparator, current limit circuit, two N-channel MOSFETs etc. (Refer to Figure 1 for detailed information)

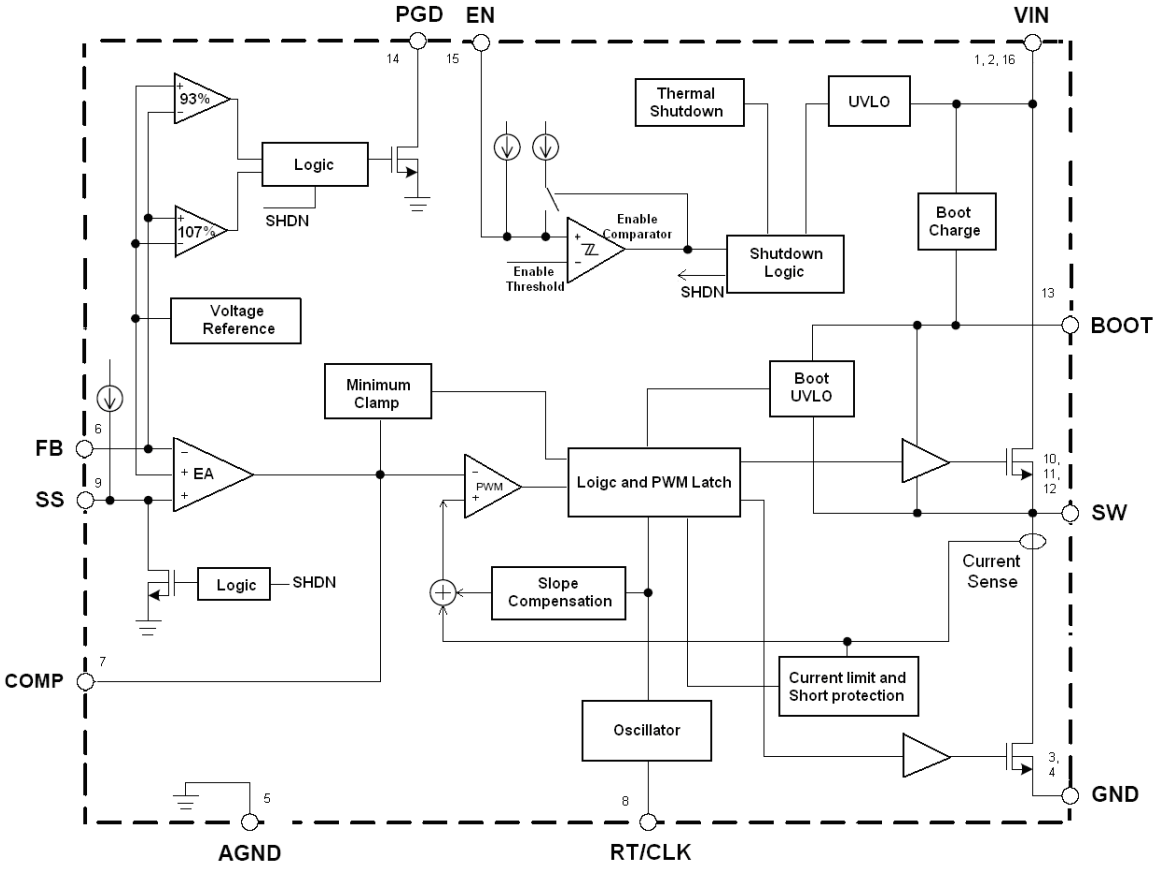

Figure 1. Functional Block Diagram of AP3440

2.1 Soft-start

The AP3440 integrates an internal soft start circuit to minimize inrush currents or provide power supply sequencing during power up. A capacitor connected between SS pin and ground implements the soft-start time. The AP3440 has an internal pull-up current source of 2μA, which charges the external slow start capacitor. Equation 1 calculates the required slow start capacitor, I_{SS} is the internal slow start charging current of 2μA, and V_{REF} is the internal voltage reference of 0.803V.

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \quad \text{.....(1)}$$

During normal operation, if the V_{IN} goes below the UVLO, or the EN pin is pulled below 1.2V, or a thermal shutdown occurs, the AP3440 will stop switching and the SS pin will be discharged to 40mV before reinitiating a powering up sequence.

2.2 Enable and Adjusting UVLO

The AP3440 are disabled when the V_{IN} falls below 2.6V. If an application requires a higher under-voltage lockout (UVLO), use the EN pin as shown in Figure 2 to adjust the input voltage UVLO by using two external resistors. The EN pin has an internal pull-up current source that provides the default condition of the AP3440 operating when the EN pin floats. Once the EN pin voltage exceeds 1.25V, an additional 2.55μA of hysteresis is added. When the EN pin is pulled below 1.18V, the 2.55μA hysteresis is removed. This additional current facilitates input voltage hysteresis.

For AP3440, the divider resistor R1 and R2 on the EN pin can be calculated according to equation 2 and 3.

$$R1 = \frac{0.944 \times V_{START} - V_{STOP}}{2.59 \times 10^{-6}} \quad \text{.....(2)}$$

$$R2 = \frac{1.18 \times R1}{V_{STOP} - 1.18 + R1 \times 3.2 \times 10^{-6}} \quad \text{.....(3)}$$

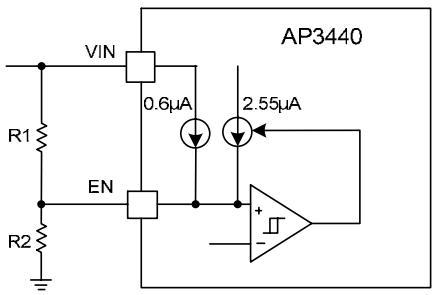

Figure 2. Adjustable Under Voltage Lock Out

2.3 Adjusting Output Voltage

The output voltage is set with a resistor divider from the FB pin. It is recommended to use divider resistors with 1% tolerance or better. Start with a 10kΩ R2 resistor and use the equation 4 to calculate R1. To improve efficiency at very light loads consider using larger value resistors. If the values are too high, the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable.

Resistor R1 can be calculated according to equation 4.

$$R1 = R2 \times \left(\frac{V_{OUT}}{0.803} - 1 \right) \quad \text{..... (4)}$$

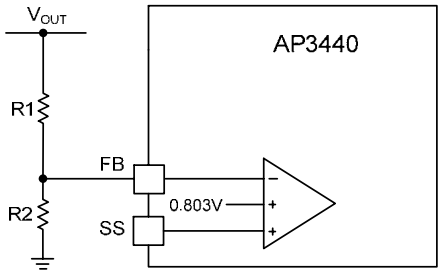

Figure 3. Voltage Divider Circuit

2.4 Synchronize Using the RT/CLK Pin

The RT/CLK pin of AP3440 is used to synchronize the converter with an external system clock referring to Figure 4. To implement the synchronization feature in a system, connect a square wave to the RT/CLK pin with an on-time of at least 75ns. When the clock is detected on the RT/CLK pin, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled. If clocking edges stop, the internal amplifier is re-enabled and the mode returns to the frequency set by the resistor. The low level of the square wave must be lower than 0.6V and the high level higher than 1.6V typically. The synchronization frequency range is from 300kHz to 2000kHz. The rising edge of the SW is synchronized to the falling edge of RT/CLK pin. Figure 5 shows a typical synchronizing waveform, the clock frequency is 2MHz.

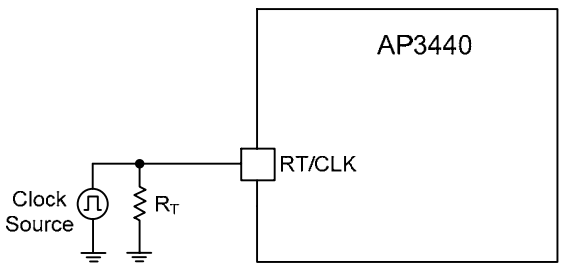

Figure 4. Synchronizing to a System Clock

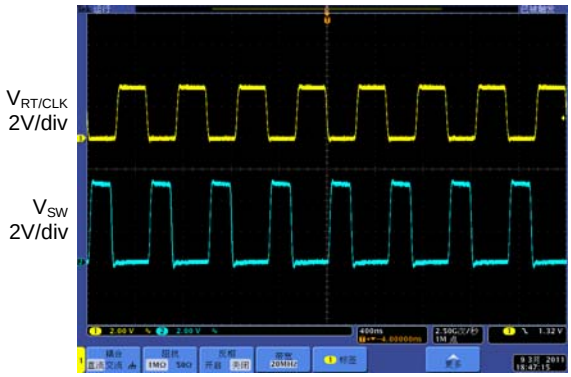

Figure 5. Synchronizing Waveform

2.5 Constant Switching Frequency and Timing Resistor

The switching frequency of the AP3440 is adjustable over a wide range from 200kHz to 2000kHz by placing a resistor with maximum value of 1000kΩ and minimum of 85kΩ, respectively, on the RT/CLK pin. An internal amplifier holds this pin at a fixed voltage when connecting an external resistor to ground to set the switching frequency. The $V_{RT/CLK}$ is typically 0.5V. To determine the timing resistance for a given switching frequency, use the equation 5.

$$R_T(k\Omega) = \frac{311890}{f_{SW}(kHz)^{1.0793}} \quad \text{.....(5)}$$

$$f_{SW}(kHz) = \frac{133870}{R_T(k\Omega)^{0.9393}} \quad \text{.....(6)}$$

To reduce the solution size one should typically set the switching frequency as high as possible, but tradeoffs of the efficiency, maximum input voltage and minimum controllable on time should be considered.

2.6 Over Current Protection

The AP3440 implements a cycle-by-cycle current limit. The high side switch current is detected during each cycle. During SCP conditions, V_{OUT} is pulled down and V_{COMP} is drived to high, increasing the switch current. When the increased high side switch current is continuously detected to trigger the current limit of high side switch 6 times, the high side and low side switches are turned off for about 2.5ms. Then both switches start switching and they will not be turned off until the next 6 OCPs are triggered. The IC works with a hiccup mode during SCP conditions.

2.7 Power Good

The PGD pin output is an open drain MOSFET. The output is pulled low when the FB voltage enters the fault condition by falling below 91% or rising above 107% of the nominal internal reference voltage. There is a 2% hysteresis on the threshold voltage, so when the FB voltage rises to the good condition above 93% or falls below 105% of the internal voltage reference the PGD output MOSFET is turned off. It is recommended to use a pull-up resistor between the values of 1kΩ and 100kΩ to a voltage source that is 5V or less. The PGD is in a valid state once the VIN input voltage is greater than 1.2V.

2.8 Thermal Shutdown

The AP3440 implement an internal thermal shutdown to protect itself if the junction temperature exceeds 140°C. Switching is stopped when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below 120°C, the device reinitiates the soft start operation. The thermal shutdown hysteresis is 20°C.

3. Component Selection

Typical application circuit of AP3440 is shown in Figure 6. For the major component selection please refer to the following section.

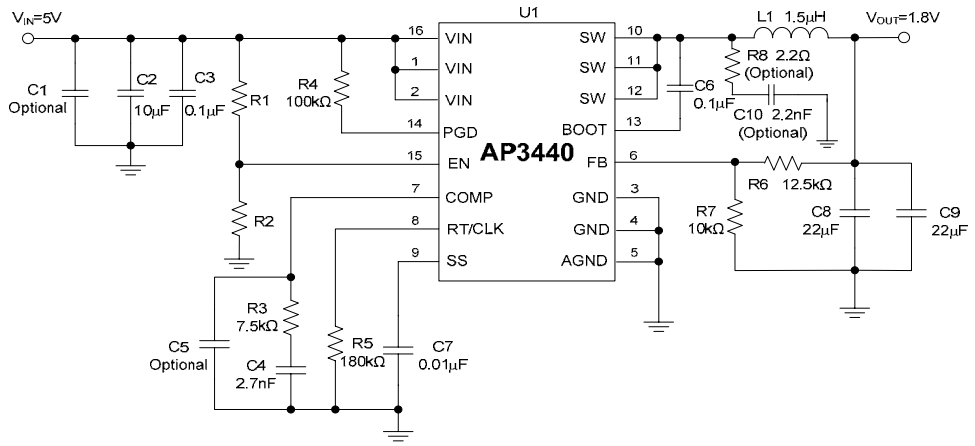

Figure 6. Typical Application of AP3440

3.1 Input Capacitor

The AP3440 requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 4.7μF effective capacitance and in some applications a bulk capacitor. The effective capacitance includes any DC bias effects. To ensure a stable operation, the input capacitor should be placed as close to the VIN pin as possible, and its value varies according to different load and different characteristic of input impedance.

There are two important parameters of the input capacitor: the voltage rating and RMS current rating. The voltage rating of the input capacitor should be at least 1.25 times larger than the maximum input voltage. The capacitor must also have a RMS current rating greater than the maximum input current ripple of the AP3440. The RMS current of input capacitor can be expressed as:

$$I_{CIN\_RMS} = I_{OUT(MAX)} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad \text{.....(7)}$$

3.2 Output Capacitor

The output capacitor is the most critical component of a switching regulator. It is used for filtering output and keeping the loop stable. The typical value is 44μF.

The primary parameters for output capacitor are the voltage rating and the equivalent series resistance (ESR). A low ESR capacitor is preferred to keep the output voltage ripple low. The output ripple is calculated as the following:

$$\Delta V_{OUT} \approx \Delta I_L \times \left(R_{ESR} + \frac{1}{8 \times f \times C_{OUT}}\right) \quad \text{.....(8)}$$

Where f is the switching frequency, C_{OUT} is the output capacitance and $\triangle I_L$ is the ripple current in the inductor.

3.3 Inductor

The inductor is used to supply smooth current to output when it is driven by a switching voltage. The higher the inductance, the lower the peak-to-peak ripple current, as the higher inductance usually means the larger inductor size, so some trade-offs should be made when select an inductor. The AP3440 is a synchronous buck converter. It always works on continuous current mode (CCM), and the inductor value can be selected as the following:

$$L = V_{OUT} \times \left(\frac{V_{IN} - V_{OUT}}{f \times V_{IN} \times I_{OUT} \times k}\right) \quad \text{.....(9)}$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, I_{OUT} is the output current, k is the coefficient of ripple current, and its typical value is 20% to 40%. Another important parameter for the inductor is the current rating. Exceeding an inductor's maximum current rating may cause the inductor to saturate and overheat. If inductor value has been selected, the peak inductor current can be calculated as the following:

$$I_{PEAK} = I_{OUT} + V_{OUT} \times \left(\frac{V_{IN} - V_{OUT}}{2 \times f \times V_{IN} \times L}\right) \quad \text{.....(10)}$$

It should be ensured that the current rating of the selected inductor is 1.5 times of the I_{PEAK}.

3.4 Slow Start Capacitor

The slow start capacitor determines the output voltage soft start time during power up.

The slow start capacitor value can be calculated using equation 11.

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \quad \text{.....(11)}$$

In AP3440, I_{SS} is 2μA and V_{REF} is 0.803V.

3.5 Bootstrap Capacitor

A 0.1μF ceramic capacitor must be connected between the BOOT pin and the SW pin for normal operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric.

3.6 Feedback Resistors

It is recommended to use divider resistors with 1% tolerance or better. Start with a 10kΩ for the R7 resistor and use the equation 12 to calculate R6.

$$R6 = R7 \times \left(\frac{V_{OUT}}{0.803} - 1\right) \quad \text{.....(12)}$$

3.7 Compensation

The output capacitor and the load resistance largely determine where the error amplifier poles and zeros need to be placed for optimum transient response and loop stability. The corner frequency of the pole and zero generated by output capacitor are:

$$f_{P1} = \frac{1}{2\pi \times R_{LOAD} \times C_{OUT}} \quad \text{.....(13)}$$

$$f_{Z1} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad \text{.....(14)}$$

Where R_{LOAD} is the load resistance, C_{OUT} is the output capacitance and R_{ESR} is the capacitor ESR.

The error amplifier provides most of the loop gain. After selecting the output capacitor, the control loop is compensated by tailoring the frequency response of the error amplifier. The low frequency pole of the error amplifier is the dominant pole and is determined primarily by C_{COMP} and the output resistance of the error amplifier as shown by:

$$f_{P2} = \frac{1}{2\pi \times R_{OUT\_EA} \times C_{COMP}} \quad \text{.....(15)}$$

Resistor R_{COMP} adds a zero to the frequency response to

control gain in the midfrequency range. This zero frequency is:

$$f_{Z2} = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}} \quad \text{.....(16)}$$

Where R_{COMP} and C_{COMP} are compensation resistor and capacitor connected to COMP pin, R_{OUT_EA} is the output impedance of the error amplifier.

A 7.5kΩ resistor and 2.7nF capacitor are used in typical application.

4. Layout Consideration

PCB layout is very important to the performance of AP3440. The loop which switching current flows through should be kept as short as possible. The external components (especially C_{IN}) should be placed as close to the IC as possible.

The feedback trace should be routed far away from the inductor and noisy power traces, and it needs to be routed as direct as possible. Locate the feedback divider resistor network near the feedback pin with short leads.

Since the SW connection is the switching node, the output inductor should be located very close to the SW pins, and the area of the PCB conductor is minimized to prevent excessive capacitive coupling.

The boot capacitor must also be located close to the device. The sensitive analog ground connections for the feedback voltage divider, compensation components, slow start capacitor and frequency set resistor should be connected to a separate analog ground trace.

The RT/CLK pin is sensitive to noise so the R_T resistor should be located as close as possible to the IC and routed with minimal lengths of trace.

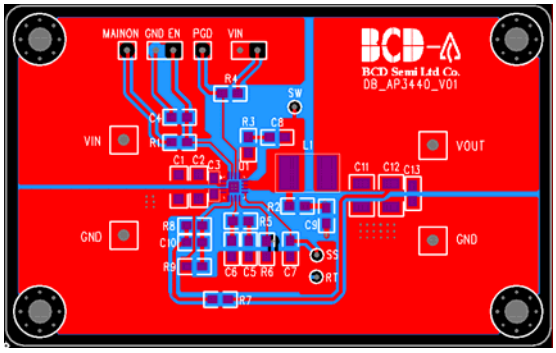

Figure 7. Top View of PCB Layout

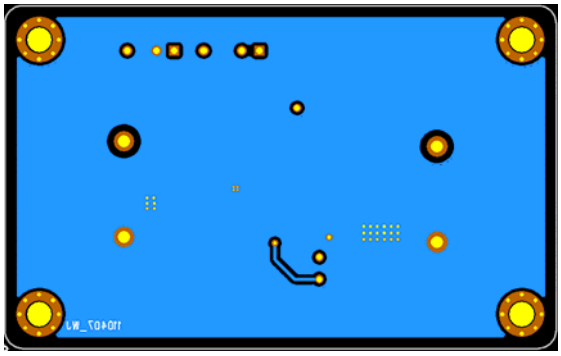

Figure 8. Bottom View of PCB Layout