### 1. Introduction

The AP3765 uses Pulse Frequency Modulation (PFM) method to realize Discontinuous Conduction Mode (DCM) operation for flyback power supplies. The principle of PFM is different from that of Pulse Width Modulation (PWM), so the design of transformer is also different.

The AP3765 can provide accurate constant voltage, constant current (CV/CC) regulation by using Primary Side Regulation (PSR).

The AP3765 can also achieve ultra-low standby power due to its PFM operation and an innovative ultra-low startup current technique. Less than 30mW standby power can be obtained to meet five-star charger criteria with AP3765 system solution.

A typical AP3765 application circuit is shown in Figure 1.

### 2. Operation Description

#### 2.1 Constant Primary Peak Current

The primary current $i_p(t)$ is sensed by a current sense resistor $R_s$ as shown in Figure 1. The current rises up linearly at a rate of:

$$\frac{dv(t)}{dt} = \frac{v_g(t)}{L_M}$$  \hspace{1cm} (1)

Figure 1. Typical Schematic of AP3765 Solution
As illustrated in Figure 2, when the current $I_p(t)$ rises up to $I_{pk}$, the switch Q1 turns off. The constant peak current is given by:

$$I_{pk} = \frac{V_{CS}}{R_S}$$

(2)

The energy stored in the magnetizing inductance $L_M$ each cycle is therefore:

$$E_g = \frac{1}{2} \cdot L_M \cdot I_{pk}^2$$

(3)

So, the power transferring from input to output is given by:

$$P = \frac{1}{2} \cdot L_M \cdot I_{pk}^2 \cdot f_{SW}$$

(4)

Where the $f_{SW}$ is the switching frequency. When the peak current $I_{pk}$ is constant, the output power depends on the switching frequency $f_{SW}$.

### 2.2 Constant Voltage Operation

The AP3765 captures the auxiliary winding feedback voltage at FB pin and operates in constant voltage (CV) mode to regulate the output voltage. Assuming the secondary winding is master, the auxiliary winding is slave during the D2 on-time and the auxiliary voltage is given by:

$$V_{aux} = \frac{N_{aux} \cdot (V_d + V_d)}{N_s}$$

(5)

where the $V_d$ is the diode forward drop voltage. $N_{aux}$ is the turns of auxiliary winding, and $N_s$ is the turns of secondary winding.

The output voltage is different from the secondary voltage in a diode forward drop voltage that depends on the current. If the secondary voltage is always detected at a fixed secondary current, the difference between the output voltage and the secondary voltage will be a fixed $V_d$. For AP3765, the voltage detection point is at 3.2μs of the D2 on-time, which means the secondary voltage is detected at a fixed secondary current. The CV loop control function of AP3765 then generates a D2 off time to regulate the output voltage.

### 2.3 Constant Current Operation

In CC operation, the CC loop control function of AP3765 will keep a fixed proportion between D2 on-time $t_{ONS}$ and D2 off-time $t_{OFFS}$ by discharging or charging the built-in capacitance connected. The fixed proportion is

$$\frac{t_{ONS}}{t_{OFFS}} = \frac{4}{3}$$

(6)

The relationship between the output constant current and secondary peak current $I_{pks}$ is given by:

$$I_{out} = \frac{1}{2} \times I_{pks} \times \frac{t_{ONS}}{t_{ONS} + t_{OFFS}}$$

(7)

At the instant of D2 turn-on, the primary current transfers to the secondary at an amplitude of:

$$I_{pks} = \frac{N_p}{N_s} \times I_{pk}$$

(8)

Thus the output constant-current is given by:

$$I_{out} = \frac{1}{2} \times \frac{N_p}{N_s} \times I_{pk} \times \frac{t_{ONS}}{t_{ONS} + t_{OFFS}} = \frac{2}{7} \times \frac{N_p}{N_s} \times I_{pk}$$

(9)

### 2.4 Leading Edge Blanking

When the power switch is turned on, a turn-on spike will occur on the sense-resistor. To avoid false termination of the switching pulse, a 750ns leading
edge blanking is built in. During this blanking period, the current sense comparator is disabled and the gate driver can not be switched off.

2.5 CCM Protection
The AP3765 is designed to operate in Discontinuous Conduction Mode (DCM) in both CV and CC modes. To avoid operating in Continuous Conduction Mode (CCM), the AP3765 detects the falling edge of the FB input voltage on each cycle. If a 0.075V falling edge of FB is not detected at the end of $t_{ON}$, the AP3765 will stop switching.

2.6 OVP & OCkP
The AP3765 includes over-voltage protection (OVP) and open circuit protection (OCkP) circuitries as shown in Figure 5. If the voltage at FB pin exceeds 8V, 100% above the normal detection voltage, the AP3765 will enter OVP mode. However, if the AP3765 doesn’t monitor 0.075V rising edge of FB input at the end of $t_{ONP}$ or high voltage (>0.075V) after $t_{SAMPLE}$, it will enter OCkP mode. When AP3765 enters OVP or OCkP mode, it will send out a fault detection pulse every 18ms until the fault has been removed.

![Figure 5. OVP & OCkP Function Block](image)

3. Design Guidelines
3.1 Low Standby Power Design
The tradeoff between the low standby power and the output overshoot at no load should be considered during the selection of the dummy resistor R8. In order to achieve less than 30mW standby power while having an acceptable output voltage rise at no load, 5.1K to 10k is recommended for R8. The power consumed in the startup resistors (R1+R2) also becomes considerable in no load or light load conditions. So 10MΩ to 13MΩ resistance is recommended for the sum of R1 and R2 considering the target of less than 30mW standby power and less than 3s turn-on delay time. And the bias capacitor C2 is recommended as 1µF to 1.5µF accordingly.

3.2. Transformer Design
Figure 1 describes a flyback converter controlled by AP3765 with a 3-winding transformer---Primary winding ($N_P$), Secondary winding ($N_S$) and Auxiliary winding ($N_A$) for bias power and output voltage detecting. The AP3765 senses the auxiliary winding feedback voltage at FB pin and obtains power supply at VCC pin. In Figure 6, a series of relative ideal operation waveforms are given to illustrate some parameters used in following design steps. And the nomenclature of the parameters in Figure 6 is as the following:

- $V_{dr}$---a simplified driving signal of primary transistor
- $I_P$---the primary side current
- $I_S$---the secondary side current
- $V_S$---the secondary side voltage
- $t_{ONP}$---the switching period of frequency
- $f_{SW}$---the switching frequency
- $t_{ON}$---the time of primary side “ON”
- $t_{OFF}$---the discontinuous time
- $I_{PK}$---peak current of primary side
- $I_{PKS}$---peak current of secondary side
- $V_{DS}$---the sum of $V_o$ and the forward voltage drop of rectification diode

![Figure 6. Operation Waveforms](image)
4. Design Steps:

Step 1. Select a Reasonable $I_{pk}$ for the Flyback Converter with AP3765

1-1. Calculate the Maximum Turn Ratio of XFMR

The maximum turn ratio of transformer should be designed first, which is to ensure that the system should work in DCM in all working conditions, especially at the minimum input voltage and full load.

If the system can meet equation (10) at minimum input voltage and full load, it can work in DCM in all working conditions.

$$t_{SW} \geq t_{ONP} + t_{ONS}$$  \hspace{1cm} (10)

For the primary side current,

$$t_{ONP} = I_{pk} \frac{L_{p}}{V_{indc}}$$  \hspace{1cm} (11)

Where $L_{p}$ is the inductance of primary winding. $V_{indc}$ is the rectified DC voltage of input.

When $V_{indc}$ is the minimum value, the maximum $t_{ONP}$ can be obtained. So,

$$t_{ONP_{MAX}} = I_{pk} \frac{L_{p}}{V_{indc_{min}}}$$ \hspace{1cm} (12)

For the secondary side current,

$$t_{ONS} = I_{pk} \frac{L_{s}}{V_{s}}$$  \hspace{1cm} (13)

In (13), $L_{s}$ is the inductance of secondary winding.

$V_{s} = V_{O} + V_{d}$, $V_{d}$ is the forward voltage drop of the secondary diode.

For (13), in CV regulation, the $V_{s}$ is a constant voltage, so $t_{ONS}$ is a constant value with different input voltage.

In the flyback converter, when the primary transistor turns ON, the energy is stored in the magnetizing inductance $L_{p}$. So the power stored in $L_{p}$ is given by,

$$P_{in} = \frac{1}{2} L_{p} I_{pk}^{2} f_{SW}$$  \hspace{1cm} (14)

Then,

$$t_{SW} = \frac{L_{p} I_{pk}^{2}}{2P_{in}}$$  \hspace{1cm} (15)

$t_{SW}$, $t_{ONP}$ and $t_{ONS}$ in (10) are replaced with (15), (12) and (13),

$$\frac{L_{p} I_{pk}^{2}}{2P_{in}} \geq I_{pk} \frac{L_{p}}{V_{s}} + I_{pk} \frac{L_{p}}{V_{indc_{min}}}$$ \hspace{1cm} (16)

Because the peak current and inductance of primary side and secondary side have the following relationship,

$$I_{pk} = n_{ps} \times I_{pk}$$ \hspace{1cm} (17)

$$L_{s} = \frac{L_{p}}{n_{ps}}$$ \hspace{1cm} (18)

Where $n_{ps}$ is the turn ratio of primary winding to the secondary winding.

With (16), (17) and (18), then,

$$\frac{L_{pk}}{2P_{in}} \geq \frac{1}{V_{O} n_{ps}} + \frac{1}{V_{in}}$$ \hspace{1cm} (19)

Because,

$$P_{in} = \frac{V_{O} I_{O}}{\eta}$$ \hspace{1cm} (20)

Where $\eta$ is the system efficiency.

At maximum load, the system will work in the boundary between CV and CC stages. $I_{O}$ can be given by,

$$I_{O} = \frac{1}{2} \frac{t_{ONS}}{t_{SW}} I_{pk}$$ \hspace{1cm} (21)

Then, $I_{pk}$ can be defined,

$$I_{pk} = k I_{O}$$ \hspace{1cm} (22)

In the design of AP3765,

$$k = \frac{2 t_{SW}}{t_{ONS}} = 3.5 \quad \text{(In CC mode, the proportion of $t_{ONS}$ and $t_{OFFS}$ is 4:3)}$$ \hspace{1cm} (23)

So it can be obtained,
\[ n_{ps} \leq V_{\text{indc}_{\text{max}}} \left( \frac{k \times \eta}{2V_0} - \frac{1}{V_S} \right) \]  
\[ N \leq V_{\text{indc}_{\text{max}}} \left( \frac{k \times \eta}{2V_0} - \frac{1}{V_0 + V_d} \right) \]

Therefore, the maximum turn ratio of primary and secondary side N can be obtained.

Because above calculations are all based on ideal conditions without considering precision of system, k is given an experiential value 3.85 to replace the real value 3.5.

1-2. Calculate the Peak Current of Primary Side and Current Sensed Resistor

\[ I_{pk} \text{ can be calculated by the output current.} \]

\[ I_{pk} = \frac{I_{pk}}{n_{ps}} = \frac{k \times I_o}{n_{ps}} \]  
\[ (26) \]

Here, \( k = 3.85 \)

\( n_{ps} \) is the calculated value of \( n_{\text{MAX}} \).

In AP3765, 0.5V is an internal reference voltage. If the sensed voltage \( V_{CS} \) reaches 0.5V, the power transistor will be shut down and \( t_{\text{ONP}} \) will be ended.

\[ R_{CS} = \frac{0.5V}{I_{pk}} \]

Then, \( R_{CS} \) can be obtained from equation (27) and selected with a real value from the standard resistor series. After \( R_{CS} \) is selected, \( I_{pk} \) should be modified based on the selected \( R_{CS} \).

From now on, \( I_{pk} \) and \( R_{CS} \) have been designed.

Step 2. Design Transformer

2-1. Calculation of the Primary Side Inductance --- \( L_P \)

The primary side inductance \( L_P \) is relative with the stored energy. \( L_P \) should be big enough to store enough energy, so that \( P_{o_{\text{Max}}} \) can be obtained from this system.

From formula (20), the output power can be given by,

\[ P_o = \frac{1}{2} I_{pk}^2 f_{\text{sw}} \eta \]  
\[ (\eta: \text{system efficiency}) \]  
\[ (28) \]

Then, \( L_P \) can be got by,

\[ L_P = \frac{2P_o}{I_{pk}^2 f_{\text{sw}} \eta} \]

Here, to achieve good overall system performance, the optimum switching frequency \( f_{\text{sw}} \) is recommended to be 50kHz to 60kHz under full load.

2-2. Re-calculate the Turn Ratio of Primary and Secondary Sides---\( n_{ps} \)

From formula (26), the turn ratio of primary and secondary side \( n \) can be re-calculated.

\[ n_{ps} = \frac{k \cdot I_0}{I_{pk}} (k = 3.85) \]  
\[ (30) \]

2-3. Calculate the Turns of Primary, Secondary and Auxiliary Sides

First, the reasonable core-type and \( \Delta B \) should be selected. Then, the turns of 3-winding transformer can be obtained respectively.

The turns of primary winding,

\[ N_P = \frac{L_P I_{pk} 10^4}{A_e \times \Delta B} (L_P:mH, I_{pk}:mA, A_e:mm^2, \Delta B:GS) \]

\[ (31) \]

The turns of secondary winding,

\[ N_S = \frac{N_P}{n_{ps}} \]  
\[ (32) \]

The turns of auxiliary winding,

\[ N_A = \frac{N_S V_A}{V_S} \]  
\[ (33) \]

Here, \( V_A \) can be set a typical value of 20V. \( V_s \) is equal to \( V_0 + V_d \).

\( A_e \) can be got automatically after core-type is selected.

Step 3. Select Diode and Primary Transistor

3-1. Select Diodes of Secondary and Auxiliary Sides

Maximum reverse voltage of secondary side

\[ V_a = V_o + \frac{V_{\text{indc}_{\text{max}}} N_S}{N_P} \]  
\[ (34) \]
Maximum reverse voltage of auxiliary side,

\[ V_{\text{av}} = V_A + \frac{V_{\text{in-leak}} N_A}{N_p} \]  \hspace{2cm} (35)

In (34) and (35), the maximum DC input voltage should be used.

### 3-2. Select the Primary Side Transistor

\[ V_{\text{dc-max}} = V_{\text{dc-spike}} + V_{\text{in-leak}} + \frac{V_A N_p}{N_S} \]  \hspace{2cm} (36)

Be careful that the value of \( V_{\text{dc-spike}} \) will be varied with different snubber circuit.

## 5. Design Example

**Specification:**
- Input voltage: 85VAC-265VAC
- Output voltage: \( V_O = 5V \)
- Output current: \( I_O = 0.7A \)
- System Efficiency: 75%
- Switching frequency: \( f_{SW} = 60kHz \)
- Forward voltage of secondary diode: \( V_d = 0.4V \)
- Forward voltage of auxiliary diode: \( V_{da} = 1V \)
- Feedback voltage of auxiliary winding: \( V_a = 20V \)
- Core_type: EE16 (\( \Lambda_e = 19.2mm^2 \))
- \( \Delta B : \Delta B = 2450GS \)
- \( V_{\text{dc-spike}} = 100V \) (with snubber circuit)
- Output cable: 28AWG, 1.5m long, 0.214\( \Omega \)/m
- Secondary diode turns on duty cycle: \( D_{\text{on}} = 4/7 \)
- Feedback resistor: \( R6 = 36.5k \), \( R7 = 9.1k \)

**Design Steps:**

**Step 1. A Reasonable Ipk of Flyback with AP3765 Should be Designed**

1-1. Calculate the Max. Turn Ratio of XFMR

\[ N_{\text{MAX}} = V_{\text{in-leak}} \left( \frac{k \times \eta}{2V_O} - \frac{1}{V_O + V_d} \right) (k \approx 3.85) \]  \hspace{2cm} (37)

\[ V_{\text{in-leak}} = V_{\text{in-leak}} \times \sqrt{2} - 40 \]  \hspace{2cm} (when \( I_O = 0.7A \), Set: \( V_{\text{in-leak}} \) drops about 40V)  \hspace{2cm} (38)

\[ N_{\text{MAX}} = 8.3 \]  \hspace{2cm} (39)

1-2. Calculate the Peak Current of Primary Side and Current Sensed Resistor

\[ I_{pk} = \frac{I_{pk}}{N} = \frac{k \times I_O}{N} \]  \hspace{2cm} (40)

\[ I_{pk,max} = 325mA \]  \hspace{2cm} (41)

Sensed current resistor,

\[ R_{CS} = \frac{0.5V}{I_{pk}} \]  \hspace{2cm} (42)

\[ R_{CS} \approx 1.538\Omega \]  \hspace{2cm} (Set: \( R_{CS} = 1.54\Omega \))  \hspace{2cm} (43)

Re-calculate peak current of primary side,

\[ I_{pk,max} = 325mA \]  \hspace{2cm} (44)

**Step 2. Design Transformer**

2-1. Calculation of the Inductance of Primary Side—\( L_p \)

\[ L_p = \frac{2P_O}{f_{SW} \eta} \]  \hspace{2cm} (45)

\[ L_p = 1.47mH \]  \hspace{2cm} (46)

2-2. Re-calculate the Turn Ratio of Primary and Secondary Side—\( N \)

\[ N = \frac{k \times I_O}{I_{pk}} (k \approx 3.85) \]  \hspace{2cm} (47)

\[ N = 8.3 \]  \hspace{2cm} (48)

2-3. Calculate the Turns of Primary, Secondary and Auxiliary Sides

The turns of primary winding,

\[ N_p = \frac{L_p I_{pk}}{10^4} \frac{10^4}{Ae \times \Delta B} \]  \hspace{2cm} (49)

\[ N_p = 102N \]  \hspace{2cm} (50)

The turns of secondary winding,

\[ N_S = \frac{N_p}{N} \]  \hspace{2cm} (51)

\[ N_S = 12T \]  \hspace{2cm} (52)
The turns of auxiliary winding,

\[ N_A = \frac{N_S V_A}{V_s} \]  
\[ N_A = 44T \]  

### Step 3. Select Diode and Primary Transistor

#### 3-1. Select Diodes of Secondary and Auxiliary Sides

Maximum reverse voltage of secondary side

\[ V_{dr} = V_A + \frac{V_{dc, max} N_A}{N_P} \]  
\[ V_{dr} = 181.8V \]

Maximum reverse voltage of auxiliary side

\[ V_{dar} = V_{dc, max} + \frac{V_A N_P}{N_S} \]  
\[ V_{dar} = 520.9V \]

#### 3-2. Select Primary Side Transistor

\[ V_{dc, max} = V_{dc, spike} + V_{dc, max} + \frac{V_A N_P}{N_S} \]

Step 4. Select Reasonable Feedback Resistor R6 and R7

\[ V_{FB} = 4V = V_A \times \frac{R_7}{R_6 + R_7} \]  
\[ \text{Set: } R_7 = 9.1k\Omega, R_6 = 36.5k\Omega \]

### Design Results Summary:

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Calculate the Maximum Peak Current of Primary Side and RCS</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( I_{PK} ) = 325 mA Peak current of primary side</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( R_{CS} ) = 1.54 ( \Omega ) Current sensed resistor</td>
<td></td>
</tr>
<tr>
<td>2.</td>
<td>Design Transformer</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( L_p ) = 1.47 mH (±8%) Inductance of primary side</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( N ) = 8.3 Turn ratio of primary and secondary</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( N_P ) = 102 T Turns of primary side</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( N_S ) = 12 T Turns of secondary side</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( N_A ) = 44 T Turns of auxiliary side</td>
<td></td>
</tr>
<tr>
<td>3.</td>
<td>Select Diode and Primary Transistor</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_{dr} ) = 49.1 V Maximum reverse voltage of secondary diode</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_{dar} ) = 181.8 V Maximum reverse voltage of auxiliary diode</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_{dc, max} ) = 520.9 V Voltage stress of primary transistor</td>
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</tr>
<tr>
<td>4.</td>
<td>Select Feedback Resistor</td>
<td></td>
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<tr>
<td></td>
<td>( R_6 ) = 36.5 k\Omega Feedback resistor</td>
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<tr>
<td></td>
<td>( R_7 ) = 9.1 k\Omega Feedback resistor</td>
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