Design Consideration with AP3408

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1. Introduction

The AP3408 is a current mode, PWM synchronous buck DC/DC converter, capable of driving a 2A load with high efficiency, excellent line and load regulation. It operates in continuous PWM mode.

The AP3408 integrates synchronous P-channel and N-channel power MOSFET switches with low on-resistance. The reference voltage of the AP3408 is 0.8V. It is ideal for portable applications powered from a single Li-ion battery. 100% duty cycle and low on-resistance P-channel internal power MOSFET can maximize the battery life.

The switching frequency of AP3408 can be programmable from 300kHz to 4MHz, which allows small-sized components, such as capacitors and inductors. A standard series of inductors from several different manufacturers are available. This feature greatly simplifies the design of switch-mode power supplies.

2. Operation

The AP3408 consists of a reference voltage module, slope compensation circuit, error amplifier, PWM comparator, current limit circuit, P-channel and N-channel MOSFETs (used as a main switch and synchronous switch respectively), etc. (Refer to Figure 1 and Figure 2 for detailed information).

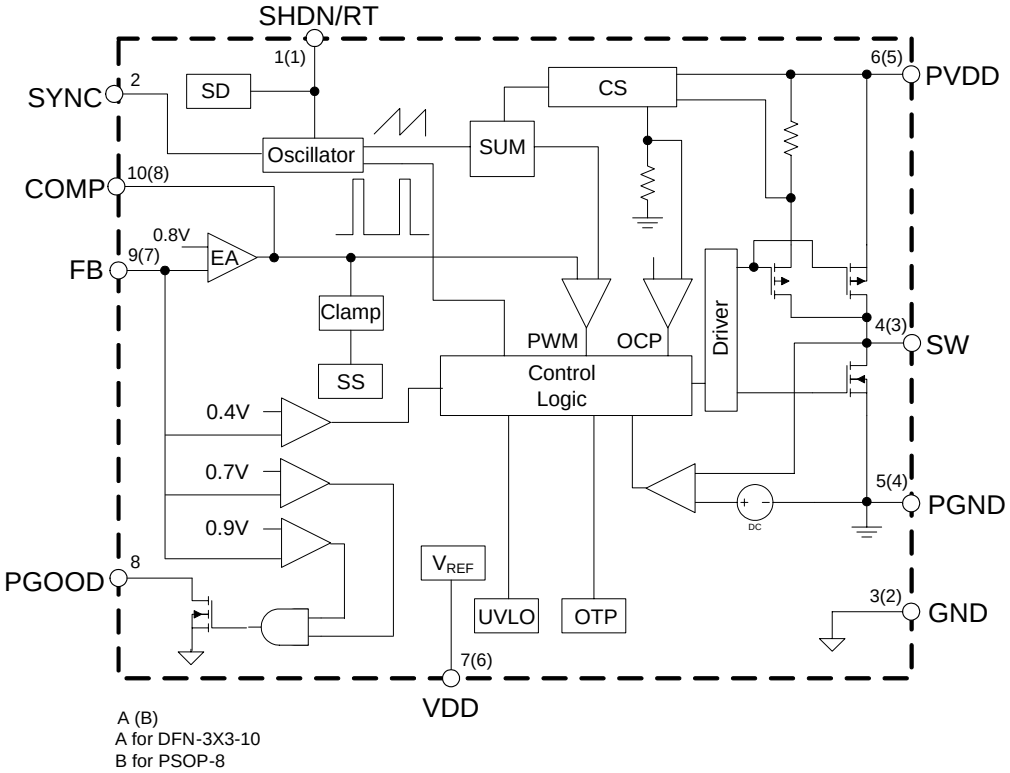


Figure 1. Functional Block Diagram of AP3408

2.1 Main Loop Control

At the beginning of each cycle initiated by the clock signal (generated from the internal oscillator), the P-channel MOSFET switch is turned on, and the inductor current ramps up until the comparator tripped and the control logic turns off the switch. The current limit comparator also turns off the switch in case the current limit of the P-channel MOSFET is exceeded. Then the N-channel synchronous switch is turned on with the inductor current ramping down. The next cycle is initiated by the clock signal again, turning off the N-channel synchronous switch and turning on the P-channel switch (Refer to Figure 2).

2.2 Short Circuit Protection

When output short to ground, the system enters HICCUP mode, shutting down the P-channel and N-channel MOSFETs for a period about 2000T (T=1/f). After that period, the AP3408 will implement softstart again. And this repeats until released from short circuit status. After released from short circuit status, the AP3408 recovers into normal operation.

2.3 Soft Start

The AP3408 integrates an internal soft start circuit to limit the inrush current during start-up. This feature allows the output to smoothly climb up to the rated output voltage, thus reducing start-up stresses and current surges.

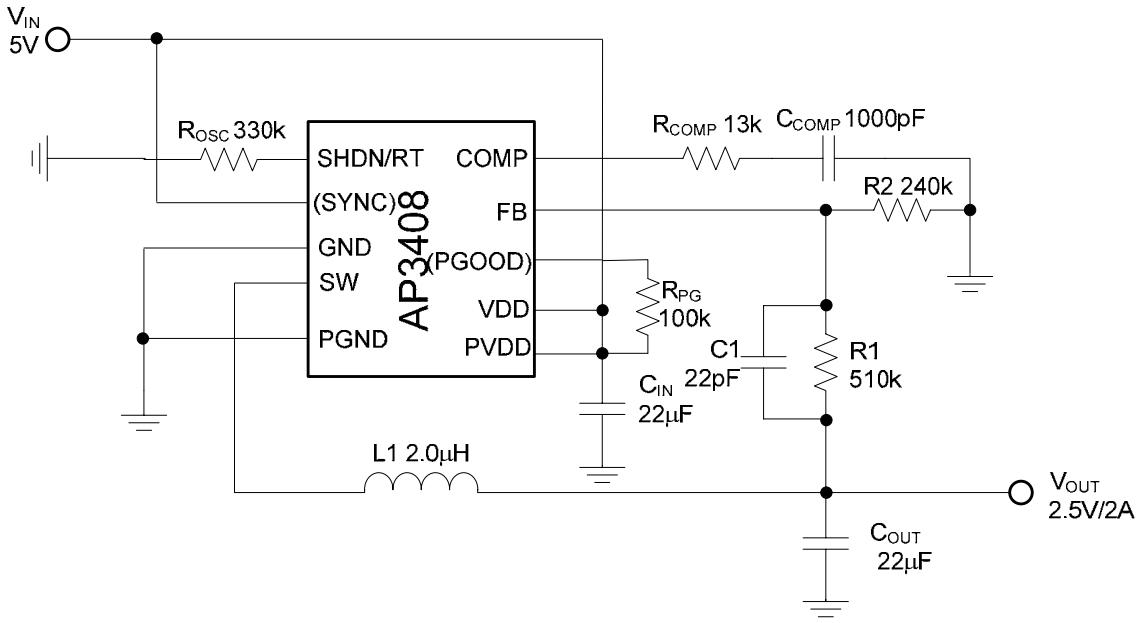


Figure 2. Typical Application of AP3408

2.4 UVLO

If the UVLO threshold is not met, all functions of the AP3408 will be disabled, preventing the device from damage by mis-operation at low input voltage. It prevents the converter from turning on the main switch and synchronous switch under undefined condition

2.5 Operation Frequency

The Operation frequency selection should be a tradeoff between efficiency and component size. High frequency allows the use of small-sized inductor and small-valued capacitor while the low frequency improves efficiency, however, requires larger-valued inductor and/or capacitor to maintain low output ripple voltage. The operation frequency of AP3408 can be determined via an external resistor, connected between the RT pin and GND. The operation frequency ranges from 0.3MHz to 4MHz (Refer to Figure 3).

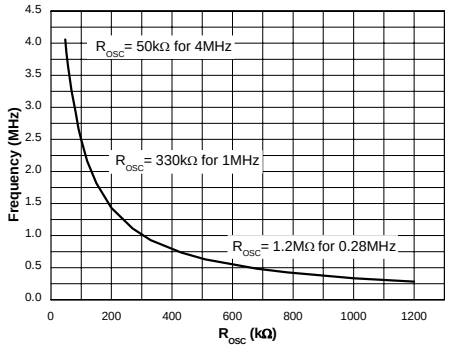


Figure 3. Frequency vs. R_{OSC}

2.6 Frequency Synchronization

The internal oscillator of the AP3408 can be synchronized to an external clock connected to the SYNC pin. The frequency of the external clock can be in the range of 300kHz to 4MHz. For this application, the oscillator timing resistor should be chosen to correspond to a frequency that is about 20% lower than the synchronization frequency.

2.7 Thermal Protection

If ⩾160ºC junction temperature sensed by the thermal protection circuit, the main switch and synchronous switch will be turned off to prevent the device from damaging. The thermal protection and shutdown circuit has a 20ºC of system hysteresis, which can prevent the converter from thermal damage under some unexpected condition.

2.8 Power Good Output Voltage Monitoring

The PGOOD pin is open-drain logic output that is pulled to ground when the output voltage is not within ±12.5% of regulation point.

3. Components Selection

3.1 Input Capacitor

Due to the discontinuous input current of the buck converter, a bulk capacitor is required to keep the input voltage constant. To ensure a stable operation, the input capacitor should be placed as close to the PVDD pin as possible, and its value varies according to different load and different characteristics of input impedance. With a typical value about 22μF for the input capacitor, the X5R or X7R ceramic capacitor are recommended due to their best temperature and voltage characteristics.

3.2 Output Capacitor

As a most critical component of a switching regulator, the output capacitor is used for output filtering and keeping the loop stable, and its typical value is 22μF.

Two primary parameters of the output capacitor are known as the voltage rating and the Equivalent Series Resistance (ESR). The higher the voltage rating, the smaller the ESR value will be. To keep a small output voltage ripple, lower ESR value should be selected. The output ripple can be expressed as the following:

$$\Delta V_{OUT} \approx \Delta I_L \times (ESR + \frac{1}{8 \times f \times C_{OUT}})$$

Where f is the switching frequency, C_{OUT} is the value of output capacitor and ΔI_L is the ripple current inside the inductor.

3.3 Inductor

The inductor is used to supply smooth current to the output when driven by a switching voltage. The higher the inductance, the lower the peak-to-peak ripple current will be. As higher inductance usually means larger inductor size, so some trade-offs should be made when selecting an inductor. The AP3408 is a synchronous buck converter, and it always works in Continuous Current Mode (CCM). The inductor value can be expressed as the following:

$$L = V_{OUT} \times \frac{V_{IN} - V_{OUT}}{f \times V_{IN} \times I_{OUT} \times k}$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, I_{OUT} is the output current and k is the ripple current coefficient, which is 20% to 40% typically.

Another important parameter is the current rating. Exceeding an inductor's maximum current rating may cause saturation and overheating to the inductor. If the inductor value is determined, peak inductor current can be expressed as the following:

$$I_{PEAK} = I_{OUT} + V_{OUT} \times \frac{V_{IN} - V_{OUT}}{2 \times f \times V_{IN} \times L}$$

It should be ensured that the current rating of the selected inductor is 1.5 times of I_{PEAK}.

3.4 Loop Compensation

A good compensation should allow the transient response to be optimized for a wide range of loads and output capacitors. The external components connected to COMP pin shown in the Figure 2 will provide an adequate starting point for most applications. The R_{COMP} in series with C_{COMP} sets a dominant zero pole of loop compensation. The values

can be modified slightly to optimize transient response. The type and value of output capacitor is determined once the final layout is made out.

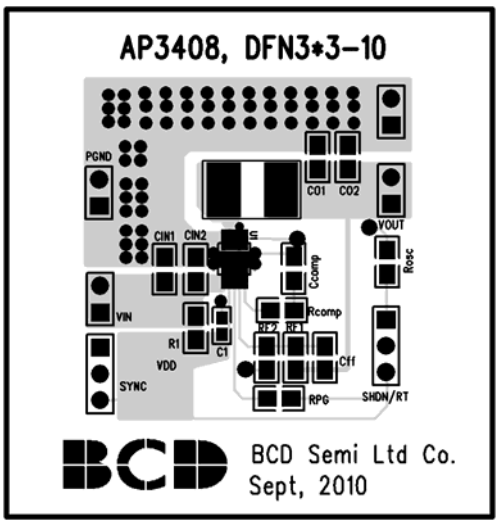
3.5 Feedforward

A feedforward capacitor C1 must be added into the circuit for better loop stability, and its typical value is 22pF. This capacitor adds a zero point to the loop to increase its phase margin.

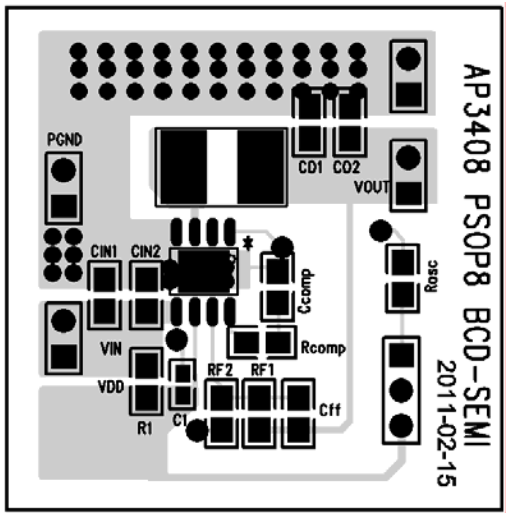
4. Layout Consideration

PCB layout is of great importance to the AP3408 performance. The high-current paths should be placed close to the AP3408 with copper or short, direct and wide traces. Input capacitors should be placed as close as possible to PVDD and PGND pin respectively.

The external feedback resistors shall be placed next to the FB pin. The exposed pad on the bottom of the IC must be connected to PGND and GND. SW node is with high frequency voltage swing and should be kept within a small area. All sensitive small-signal nodes, especially the FB pin, should be kept far away from the SW node. An example of PCB layout is illustrated in Figure 4.



For DFN-3×3-10



For PSOP-8

Figure 4. AP3408 PCB Layout (Example)