

Design Consideration with AP3409/A

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1. Introduction

The AP3409/A is a current mode, PWM synchronous buck DC/DC converter, capable of driving a 3A load with high efficiency, excellent line and load regulation. It operates in continuous PWM mode.

The AP3409/A integrates synchronous P-channel and N-channel power MOSFET switches with low on-resistance. The reference voltage of the AP3409/A is 0.8V. It is ideal for portable applications powered from a single Li-ion battery. 100% duty cycle and low on-resistance P-channel internal power MOSFET can maximize the battery life.

The switching frequency of AP3409/A can be

programmable from 300kHz to 4MHz, which allows small-sized components, such as capacitors and inductors. A standard series of inductors from several different manufacturers are available. This feature greatly simplifies the design of switch-mode power supplies.

2. Operation

The AP3409/A consists of a reference voltage module, slope compensation circuit, error amplifier, PWM comparator, current limit circuit, P-channel and N-channel MOSFETs (used as a main switch and synchronous switch respectively), etc. (Refer to Figure 1 and Figure 2 for detailed information).

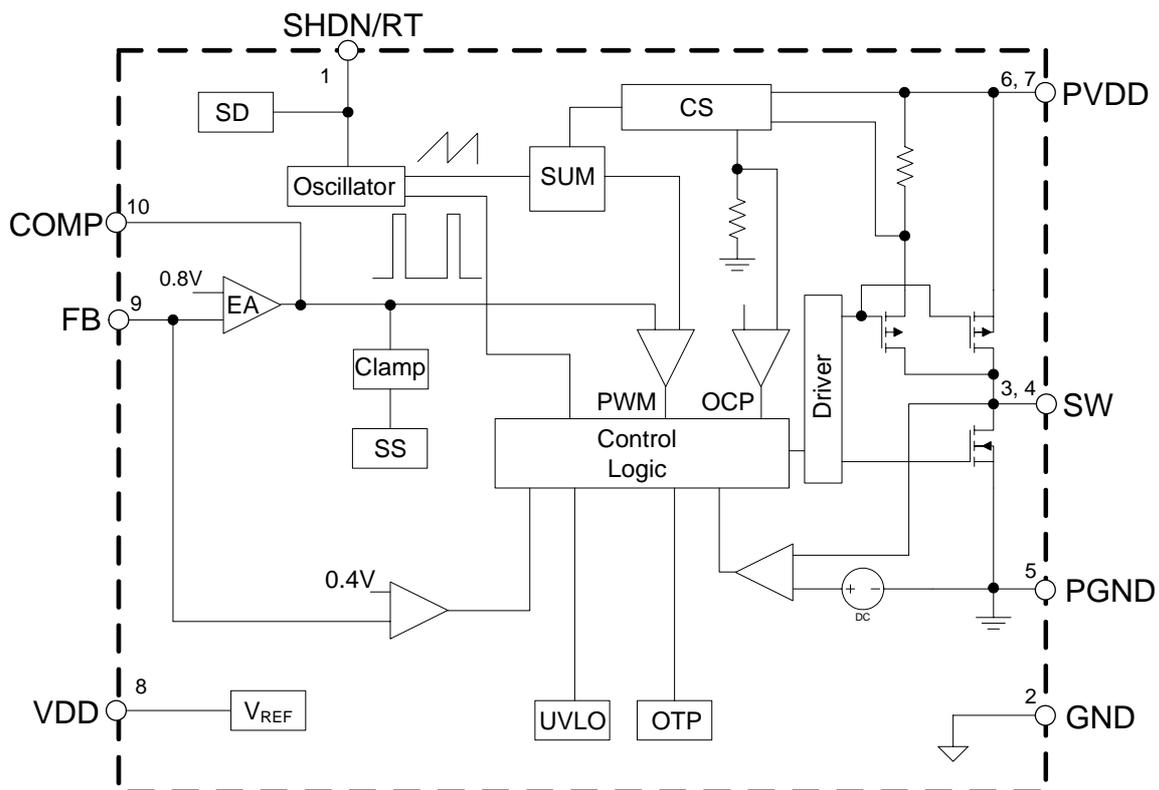


Figure 1. Functional Block Diagram of AP3409

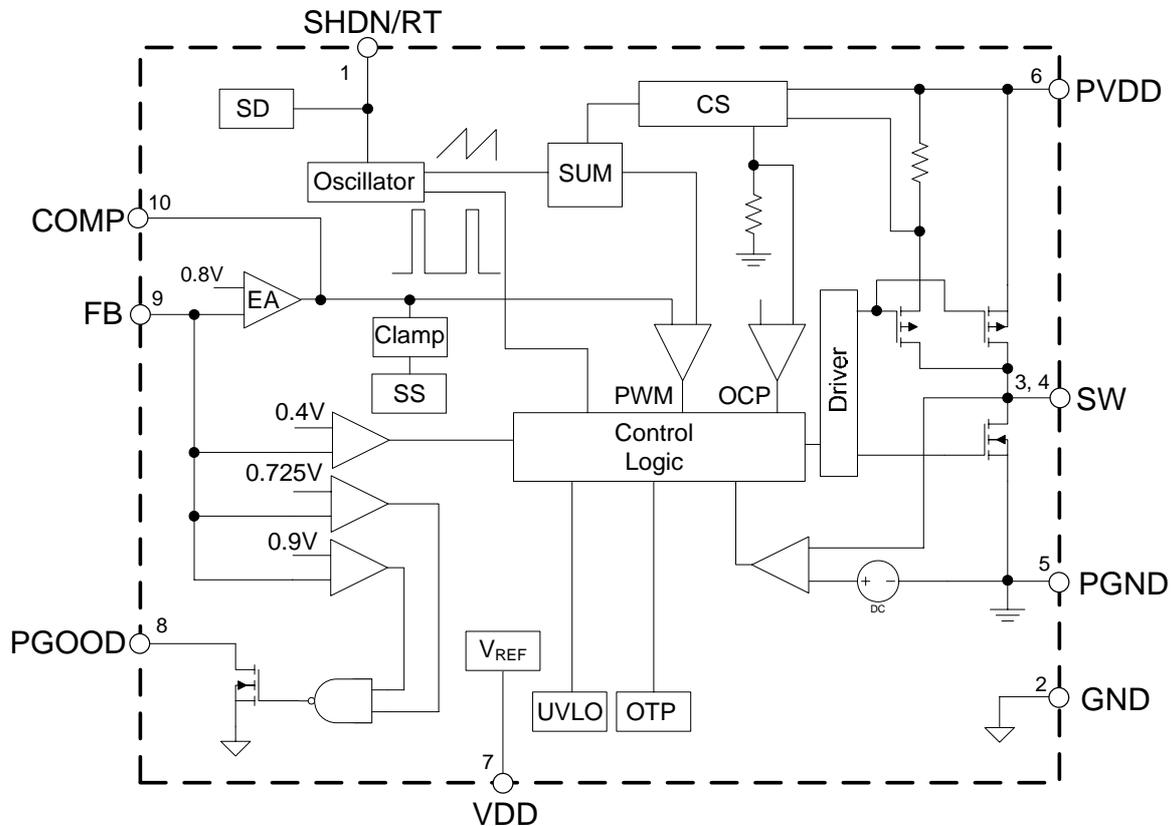


Figure 2. Functional Block Diagram of AP3409A

2.1 Main Loop Control

At the beginning of each cycle initiated by the clock signal (generated from the internal oscillator), the P-channel MOSFET switch is turned on, and the inductor current ramps up until the comparator tripped and control logic turns off the switch. The current limit comparator also turns off the switch in case the current limit of the P-channel MOSFET is exceeded. Then the N-channel synchronous switch is turned on with the inductor current ramping down. The next cycle is initiated by the clock signal again, turning off the N-channel synchronous switch and turning on P-channel switch (Refer to Figure 3, 4.).

2.2 Short Circuit Protection

When output short to ground, the system enters HICCUP mode, shutting down the P-channel and N-channel MOSFETs for a period about $2000T$ ($T=1/f$). After that period, the AP3409/A will implement softstart again. And this repeats until released from short circuit status. After released from short circuit status, the AP3409/A recovers into normal operation.

2.3 Soft Start

The AP3409/A integrates an internal soft start circuit to limit the inrush current during start-up. This feature allows the output to smoothly climb up to the rated output voltage, thus reducing start-up stresses and current surges.

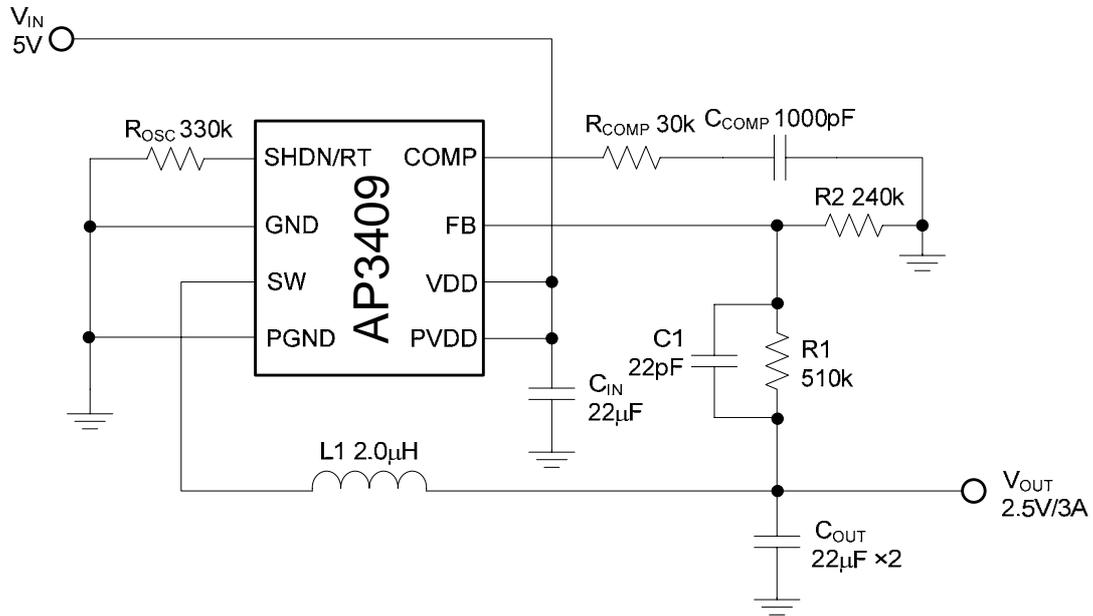


Figure 3. Typical Application of AP3409

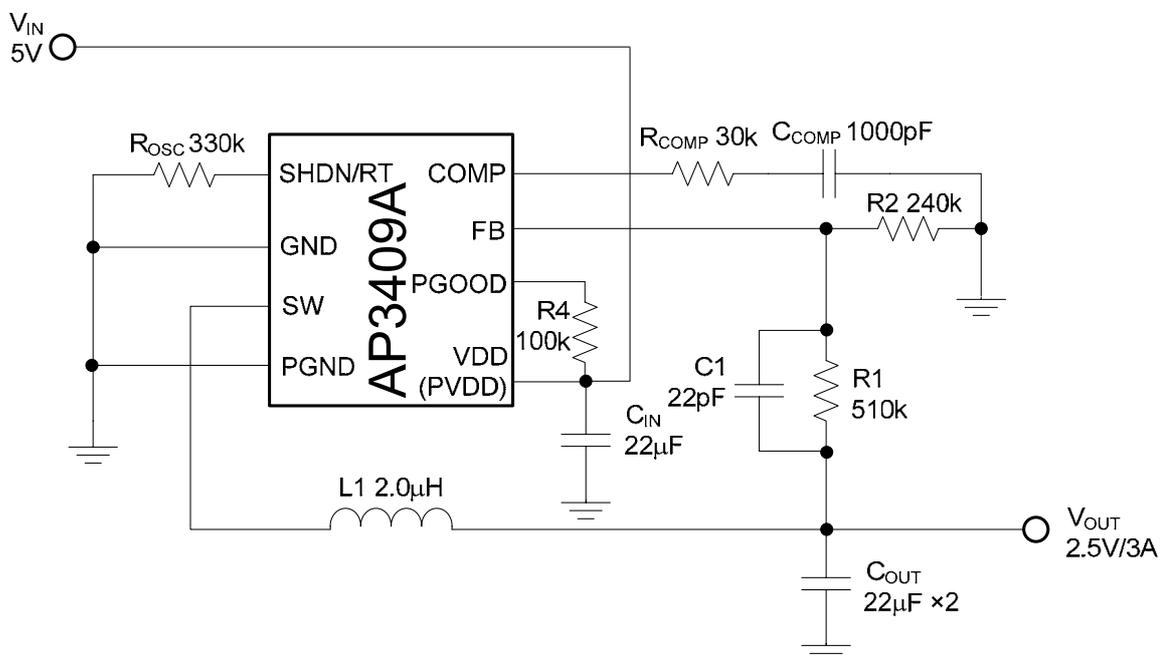


Figure 4. Typical Application of AP3409A

2.4 UVLO

If the UVLO threshold is not met, all functions of the AP3409/A will be disabled, preventing the device from damage by mis-operation at low input voltage. It prevents the converter from turning on the main switch and synchronous switch under undefined condition.

2.5 Operation Frequency

The Operation frequency selection should be a tradeoff between efficiency and component size. High frequency allows the use of small-sized inductor and small-valued capacitor while the low frequency improves efficiency, however, requires larger-valued inductor and/or capacitor to maintain low output ripple voltage. The operation frequency of AP3409/A can be determined via an external resistor, connected between the RT pin and GND. The operation frequency ranges from 0.3MHz to 4MHz (Refer to Figure 5).

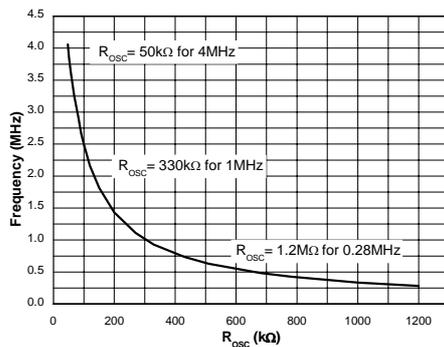


Figure 5. Frequency vs. R_{osc}

2.6 Thermal Protection

If $\geq 160^{\circ}\text{C}$ junction temperature sensed by the thermal protection circuit, the main switch and synchronous switch will be turned off to prevent the device from damaging. The thermal protection and shutdown circuit has a 20°C of system hysteresis, which can prevent the converter from thermal damage under some unexpected condition.

2.7 Power Good Output Voltage Monitoring (Only for AP3409A)

The PGOOD pin is open-drain logic output that is pulled to ground when the output voltage is not within $\pm 12.5\%$ of regulation point.

3. Components Selection

3.1 Input Capacitor

Due to the discontinuous input current of the buck converter, a bulk capacitor is required to keep the input voltage constant. To ensure a stable operation, the input capacitor should be placed as close to the PVDD pin as possible, and its value varies according to different load and different characteristics of input impedance. With a typical value about $22\mu\text{F}$ for the input capacitor, the X5R or X7R ceramic capacitor are recommended due to their best temperature and voltage characteristics.

3.2 Output Capacitor

As a most critical component of a switching regulator, the output capacitor is used for output filtering and keeping the loop stable, and its typical value is $2 \times 22\mu\text{F}$. Two primary parameters of the output capacitor are known as the voltage rating and the Equivalent Series Resistance (ESR). The higher the voltage rating, the smaller the ESR value will be. To keep a small output voltage ripple, lower ESR value should be selected. The output ripple can be expressed as the following:

$$\Delta V_{OUT} \approx \Delta I_L \times \left(ESR + \frac{1}{8 \times f \times C_{OUT}} \right)$$

Where f is the switching frequency, C_{OUT} is the value of output capacitor and ΔI_L is the ripple current inside the inductor.

3.3 Inductor

The inductor is used to supply smooth current to the output when driven by a switching voltage. The higher the inductance, the lower the peak-to-peak ripple current will be. As higher inductance usually means larger inductor size, so some trade-offs should be made when selecting an inductor. The AP3409/A is a synchronous buck converter, and it always works in Continuous Current Mode (CCM). The inductor value can be expressed as the following:

$$L = V_{OUT} \times \frac{V_{IN} - V_{OUT}}{f \times V_{IN} \times I_{OUT} \times k}$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, I_{OUT} is the output current and k is the ripple current coefficient, which is 20% to 40% typically.

Another important parameter is the current rating. Exceeding an inductor's maximum current rating may cause saturation and overheating to the inductor. If

the inductor value is determined, peak inductor current can be expressed as the following:

$$I_{PEAK} = I_{OUT} + V_{OUT} \times \frac{V_{IN} - V_{OUT}}{2 \times f \times V_{IN} \times L}$$

It should be ensured that the current rating of the selected inductor is 1.5 times of I_{PEAK} .

3.4 Loop Compensation

The AP3409/A employs current mode control for easy compensation and fast transient response. The system stability and transient response are controlled through COMP pin. The COMP is the output of the internal transconductance error amplifier. A series capacitor-resistor combination sets a pole-zero combination to govern the characteristics of the control system.

Optimal loop compensation depends on the output capacitor, inductor, load, compensation network and also the device itself. For a stable system, the values for the compensation network is shown in Table 1.

V_{IN}/V_{OUT} (V)	R1 (k Ω)	R _{COMP} (k Ω)	C _{COMP} (nF)
3.3/2.5	510	30	1
5/2.5	510	30	1
3.3/1.8	300	25	1
5/1.8	300	20	1
3.3/1.2	120	5	2.2

Table 1. Compensation Value R-C Combination

If the V_{IN}/V_{OUT} value of desired solution are not found from the table above, the loop transfer function should be analyzed to optimize the loop compensation.

The DC gain of the voltage feedback loop is given by:

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_{VEA} \times \frac{V_{FB}}{V_{OUT}}$$

Where V_{FB} is the feedback voltage (0.8V), A_{VEA} is the error amplifier voltage gain, G_{CS} is the current sense transconductance and R_{LOAD} is the load resistor value.

The system has two poles of importance. One is due to the compensation capacitor (C_{COMP}) and the output resistor of the error amplifier, and the other is due to

the output capacitor and the load resistor. These poles are located at:

$$f_{P1} = \frac{G_{EA}}{2\pi \times C_{COMP} \times A_{VEA}}$$

$$f_{P2} = \frac{1}{2\pi \times C_{OUT} \times R_{LOAD}}$$

Where G_{EA} is the error amplifier transconductance. The system has one zero of importance, due to the compensation capacitor (C_{COMP}) and the compensation resistor (R_{COMP}). This zero is located at:

$$f_{Z1} = \frac{1}{2\pi \times C_{COMP} \times R_{COMP}}$$

The system may have another zero of importance, if the output capacitor has a large capacitance and/or a high ESR value. The zero, due to the ESR and capacitance of the output capacitor, is located at:

$$f_{ESR} = \frac{1}{2\pi \times C_{OUT} \times R_{ESR}}$$

The goal of compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the feedback loop has the unity gain is important. Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could cause system instability. A good standard is to set the crossover frequency below one-tenth of the switching frequency.

To optimize the compensation components, the following procedure can be used.

1) Choose the compensation resistor (R_{COMP}) to set the desired crossover frequency. A good standard is to set the crossover frequency below one-tenth of the switching frequency.

Determine R_{COMP} by the following equation:

$$R_{COMP} < \frac{2\pi \times C_{OUT} \times 0.1 \times f_S \times V_{OUT}}{G_{EA} \times G_{CS} \times V_{FB}}$$

Where f_S is switch frequency.

2) Choose the compensation capacitor (C_{COMP}) to achieve the desired phase margin. For applications with typical inductor values, setting the compensation zero (f_{Z1}) below one-fourth of the crossover frequency provides sufficient phase margin.

Determine C_{COMP} by the following equation:

$$C_{COMP} > \frac{4}{2\pi \times R_{COMP} \times f_C}$$

Where f_C is crossover frequency.

3.5 Feedforward

A feedforward capacitor $C1$ must be added into the circuit for better loop stability, and its typical value is 22pF. This capacitor adds a zero point to the loop to increase its phase margin.

4. Layout Consideration

PCB layout is of great importance to the AP3409/A performance. The high-current paths should be placed close to the AP3409/A with copper or short, direct and wide traces. Input capacitors should be

placed as close as possible to PVDD and PGND pin respectively

The external feedback resistors shall be placed next to the FB pin. The exposed pad on the bottom of the IC must be connected to PGND and GND. The SW node is with high frequency voltage swing and should be kept within a small area. All sensitive small-signal nodes, especially the FB pin, should be kept far away from the SW node. An example of PCB layout is illustrated in Figure 6.

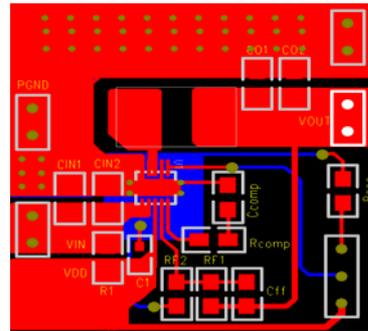


Figure 6. AP3409 PCB Layout (Example)