Design Consideration with AP3202

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1. Introduction

The AP3202 is a current mode step-down DC-DC converter, capable of driving a 2A load with high efficiency, excellent line and load regulation. The internal compensation provides simple and stable power supplies with the minimum of external components.

The AP3202 is optimized to work over the input voltage ranges from 4.75V to 18V, making it suit for a wide variety of power supply systems. Current mode control provides fast transient response and cycle-by-cycle current limit. Internal soft-start function provides a controlled startup with no overshoot, even at light loads. The over current protection, short circuit protection and over temperature protection functions are built inside which increase the system reliability.

2. General Description

The AP3202 is a non-synchronous step-down converter with a built-in power MOSEFT. Turn on/off MOSFET M1 and Schottky diode alternately to chop the input voltage. The current sense signal compared with the EA output signal to regulate the output voltage and adjust the MOSFETs duty cycle. The AP3202 is also a high reliability IC with integrated OCP, OVP, OTP, UVLO circuits. For more description information, please refer to the functional block diagram.

A representative block diagram of AP3202 is shown in Figure 1:

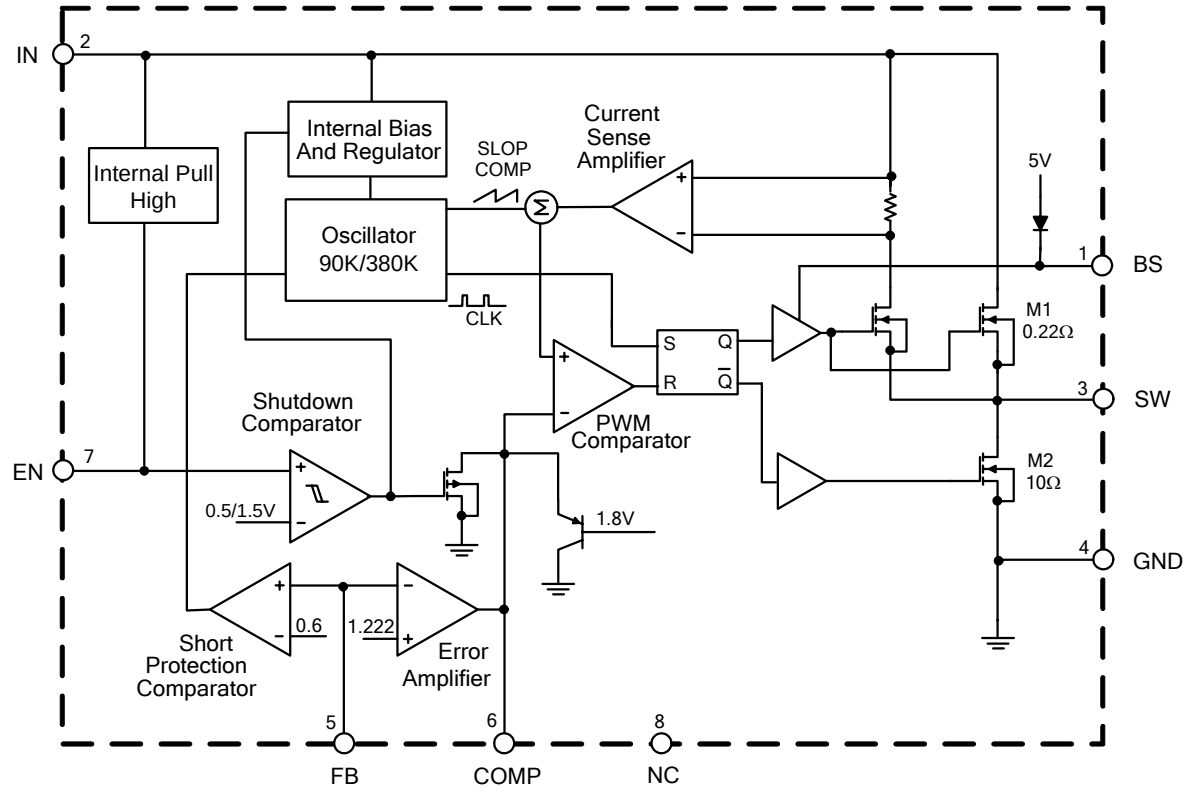

Figure 1. Functional Block Diagram of AP3202

2.1 Enable and Soft Start

The AP3202 provides an internal soft-start feature, which ramps the output voltage and output current from 0 to the full value. This feature prevents output voltage from overshoot at light load and large inrush current upon startup.

EN pin is an input control pin that turns on/off the regulator. Forcing this pin above 1.5V or leave this pin floating enables the IC, while forcing this pin below 0.5V shuts down the IC.

2.2 Over Current Protection (OCP)

The AP3202 has an internal over current function to protect itself from catastrophic failure. The AP3202 monitors the drain-to-source current of the internal upper power MOSFET. The current limit threshold is internally set at 3.8A. When the inductor current is higher than the current limit threshold, OCP is triggered and forces the power switching MOSFET turning off until the next switching cycle. The FB voltage is proportional to the output voltage. When FB pin voltage falls below 0.3V, the operating frequency reduces to 90kHz. The AP3202 will restart once released from OCP condition.

2.3 Over Voltage Protection

The AP3202 has an internal over voltage protection circuit. When the output voltage goes higher than the OVP threshold, the power switching is turned off. The AP3202 will restart once released from OVP condition.

2.4 Over Temperature Protection

The internal thermal temperature protection circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When the junction temperature exceeds 160°C, it shuts down the internal control circuit and switching power MOSFET. The AP3202 will restart automatically under the control of soft-start circuit when the junction temperature decreases to 130°C.

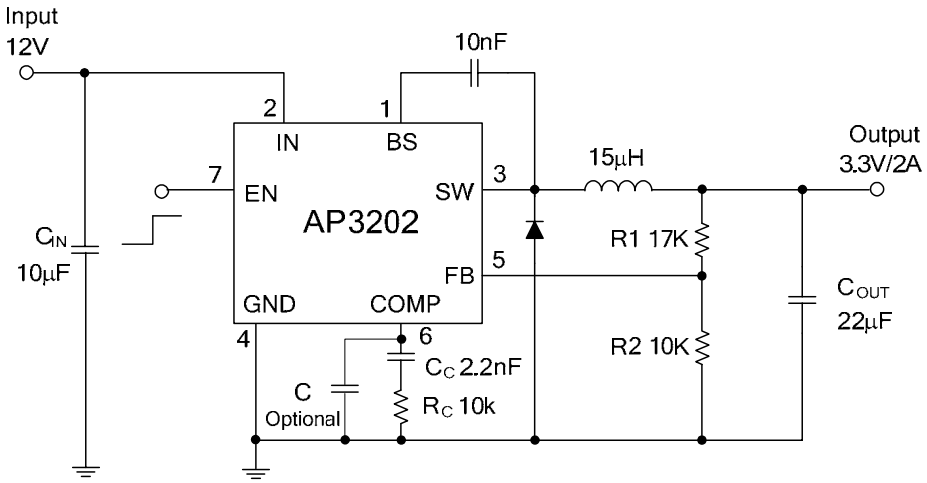

Figure 2. Typical Application of AP3202

3. Application Information

The typical application circuit of AP3202 is shown in Figure 2. For the setting of parameters, please refer to the following descriptions.

3.1 Output Voltage

The output voltage can be set by using a resistor voltage divider from the output to FB. The V_{OUT} is divided by the voltage divider as below:

$$V_{FB} = V_{OUT} \times \left(\frac{R_2}{R_1 + R_2} \right) \text{----------(1)}$$

Where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

Thus, V_{OUT} can be expressed as:

$$V_{OUT} = 1.222 \times \left(\frac{R_1 + R_2}{R_2} \right)$$

First, select a value for R2 whose recommended value is 10kΩ. Then, R1 is determined by:

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{1.222} - 1 \right) \text{----------(2)}$$

3.2 Inductor

The inductor is used to supply smooth current to output when driven by a switching voltage. Its value is determined by the operating frequency, load current, ripple current and duty cycle.

A higher-value inductor can decrease the ripple current and output ripple voltage, however usually with larger physical size. So some compromise needs to be made when selecting the inductor.

Assuming that the IC is operating in the continuous mode and the peak-to-peak inductor ripple current is 26% of maximum output current (In most applications, a good compromise is to select the peak-to-peak ripple current between 20% and 30% of the maximum load current of the converter), the inductor L1 can be selected according to:

$$L1 = V_{OUT} \times \frac{V_{IN} - V_{OUT}}{f_{SW} \times V_{IN} \times 26\% \times I_{OUT}}$$

Where V_{IN} is the input voltage, I_{OUT} is the output current and f_{SW} is the oscillator frequency.

Another important parameter for the inductor is the current rating. After fixing the inductor value, the peak inductor current can be calculated as:

$$I_{PEAK} = I_{OUT} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times V_{IN} \times f_{SW} \times L1}$$

Here, I_{PEAK} is the peak inductor current.

It should be ensured that the current rating of the selected inductor is 1.5 times of the peak inductor current.

3.3 Input Capacitor

A high-quality input capacitor with big value is needed to filter noise at input voltage source and limit the input ripple voltage while supplying most of the switch current during ON time. For input capacitor selection, a ceramic capacitor is highly recommended due to its low impedance and small size. However, tantalum or low electrolytic capacitor is also sufficed.

There are two important parameters for input capacitor: the voltage rating and RMS current rating. The voltage rating should be at least 1.25 times greater than the maximum input voltage (1.5 times is regarded as the conservative value). Since the input current is discontinuous in a buck converter, the current stress on the input capacitor should be considered. The RMS of input capacitor current can be calculated as:

$$I_{CIN\_RMS} = I_{OUT(MAX)} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

Here, I_{CIN_RMS} is the RMS of input capacitor current.

As indicated by the RMS current equation above, I_{CIN_RMS} reaches the highest level at the duty cycle of 50%. So the RMS current of input capacitor should be greater than half of the output current under this worst case. For reliable operation and best performance, ceramic capacitors are preferred for input capacitor because of their low ESR and high ripple current rating. And X5R or X7R type dielectric ceramic capacitors are preferred due to their better temperature and voltage characteristics. Additionally, when selecting ceramic capacitor, make sure its capacitance is big enough to provide sufficient charge to prevent excessive voltage ripple at input. The input ripple voltage can be approximately expressed as below:

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \frac{V_{OUT}}{V_{IN}}$$

Where ΔV_{IN} is the input ripple voltage.

3.4 Output Capacitor

The output capacitor can be selected based upon the desired output ripple and transient response. The output voltage ripple depends directly on the ripple current and is affected by two parameters of the output capacitor: total capacitance and the Equivalent Series Resistance (ESR). The output ripple voltage can be expressed as:

$$\Delta V_O = \Delta I_L \times \left[R_{ESR} + \left(\frac{1}{8 \times C_{OUT} \times f_{SW}} \right) \right]$$

ΔV_O stands for the output ripple voltage and R_{ESR} stands for the ESR of output capacitor.

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum capacitor or aluminum electrolytic capacitor are recommended.

The output capacitor selection will also affect the output drop voltage during load transient. The output drop voltage during load transient is dependent on many factors. However, an approximation of the

transient drop ignoring loop bandwidth can be expressed as:

$$V_{DROP} = \Delta I_{TRAN} \times R_{ESR} + \frac{L \times \Delta I_{TRAN}^{2}}{C_{OUT} \times (V_{IN} - V_{OUT})}$$

Where ΔI_{TRAN} is the output transient load current step, and V_{DROP} is the output voltage drop (ignoring loop bandwidth).

Both the voltage rating and RMS current rating of the capacitor needs to be carefully examined when designing a specific output ripple or transient drop. The output capacitor voltage rating should be greater than 1.5 times of the maximum output voltage. In the buck converter, output capacitor current is continuous. The RMS current is decided by the peak-to-peak inductor ripple current. It can be expressed as:

$$I_{COUT\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Where I_{COUT_RMS} is the RMS current of output capacitor.

3.5 Loop Compensation

The AP3202 employs current-mode control to achieve easy compensation and fast dynamic response. Optimal loop compensation depends on the output capacitor, inductor, load, compensation network and also the device itself. For a stable system, the recommended values for the compensation network are shown in the table below.

V_{IN}/V_{OUT} (V)	L (μH)	C_{OUT} (μF)	C_C (nF)	R_C (kΩ)	C_{OPTION} (pF)
12V/5V	15	22	1	15	None
12V/3.3V	15	22	2.2	10	None
12V/2.5V	15	22	1	5.1	None
12V/1.8V	15	22	2.2	4.3	None
5V/3.3V	22	22	3.3	9.1	None
5V/2.5V	15	22	1	4.7	None
5V/1.8V	15	22	2.2	5.1	None

If the desired solution differs from the table above, the loop transfer function should be analyzed to optimize the loop compensation. The overall loop transfer function is the product of the power stage and the feedback network transfer function. The power stage transfer function is dictated by the modulator, the output LC filter and load. The feedback transfer function is dictated by the error amplifier gain, external compensation network and feedback resistor ratio.

The purpose of loop compensation is to shape the loop transfer function in order to meet the desired loop gain. The crossover frequency should be set firstly. Because lower crossover frequency result in slower line and load transient responses, while higher crossover frequency could cause system instability. A good compromise is to set the crossover frequency below 10% of the switching frequency. The crossover frequency (f_C) can be calculated by:

$$f_C = \left(\frac{G_{EA} \times G_{CS} \times R_C}{2\pi \times C_C} \times \frac{V_{FB}}{V_{OUT}} \right) < 0.1 \times f_{SW}$$

Where f_C is the crossover frequency, G_{EA} is the error amplifier transconductance, G_{CS} is the current sense trans-conductance. And the desired crossover frequency can be set via compensation resistor R_C.

For sufficient phase margin, the loop gain slope should be -20db/decade at the cross frequency. To suffice this requirement, the output filter pole (f_{P_OUT}), which is produced by output capacitor and the load resistor, should be cancelled by the zero point of error amplifier (f_{Z_EA}) due to the compensation capacitor (C_C) and the output resistor. They can be expressed as:

$$f_{P\_OUT} = \left(\frac{1}{2\pi \times C_{OUT} \times R_O} \right)$$

$$f_{Z\_EA} = \left(\frac{1}{2\pi \times C_C \times R_C} \right)$$

Where, f_{P_OUT} is the output filter pole and f_{Z_EA} is the zero point of error amplifier.

In general, we can set f_{Z_EA} below one-forth of the f_C. R_C and C_C should be set appropriately to make sure the system work at the desired transient voltage drop and setting time.

If the output capacitor has a large capacitance and/or a high ESR value, the zero point resulting from the output capacitor as well as its ESR should be considered. In this case, the additional capacitor (C_{OPTION}) should be placed between the COMP pin and GND. And, C_{OPTION} can add a pole to the circuit, thus increasing the mid-frequency width of the control circuit.

$$f_{Z\_ESR} = \left(\frac{1}{2\pi \times C_{OUT} \times R_{ESR}} \right)$$

Where f_{Z_ESR} is the zero point of output filter.

If needed, the value of C_{OPTION} can be expressed as:

$$C_{OPTION} = \frac{C_{OUT} \times R_{ESR}}{R_C}$$

3.6 Catch Diode

Buck regulators require a diode to provide a return path for the inductor current when the switch turns off. A fast-diode is necessary which must be located as close to the AP3202 as possible using short leads and short printed circuit traces.

Schottky diode is recommended for its fast switching times and low forward voltage drop. The reverse voltage rating and the current rating of the catch diode should ensure the system to function normally with a certain safety margin. The reverse voltage should be over 2 times of the system operating voltage and the current rating should be over 1.5 times of the full load current. Additionally, a Schottky diode with a low forward voltage drop must be choosing to improve efficiency.

3.7 Bootstrap Capacitor

The bootstrap capacitor provided is used to drive the power switch's gate above the supply voltage. The bootstrap capacitor is supplied by an internal 5V supply and placed between SW pin and BS pin to form a floating supply across the power switch driver. So the bootstrap capacitor should be a good quality and high-frequency ceramic capacitor. For best performance, the bootstrap capacitor should be X5R and X7R ceramic capacitor, and is recommended to be 10nF.

4. PCB Layout Guideline

PCB layout is an important part for DC-DC converter design. Poor PCB layout may reduce the converter performance and disrupt its surrounding circuitry due to EMI. A good PCB layout should follow guidelines below:

4.1 Power Path Length

The power path of AP3202 includes an input capacitor, output inductor and output capacitor. Place them on the same side of PCB and connect them with thick traces or copper plans on the same layer. The power components must be kept together closely. The longer the paths, the more they act as antennas, radiating unwanted EMI.

4.2 Coupling Noise

The external control components should be placed as close to the IC as possible.

4.3 Feedback Net

Special attention should be paid to the route of the feedback wring. The feedback trace should be routed far away from the inductor and noisy power traces. Try to minimize trace length to the FB pin and connect feedback network behind the output capacitors.

4.4 Via Hole

Be careful to the via hole. Via hole will result in high resistance and inductance to the power path. If heavy switching current must be routed through via holes and/or internal planes, use multiple via holes parallel to reduce their resistance and inductance.

Figure 3, 4 and 5 are examples of AP3202 PCB layer.

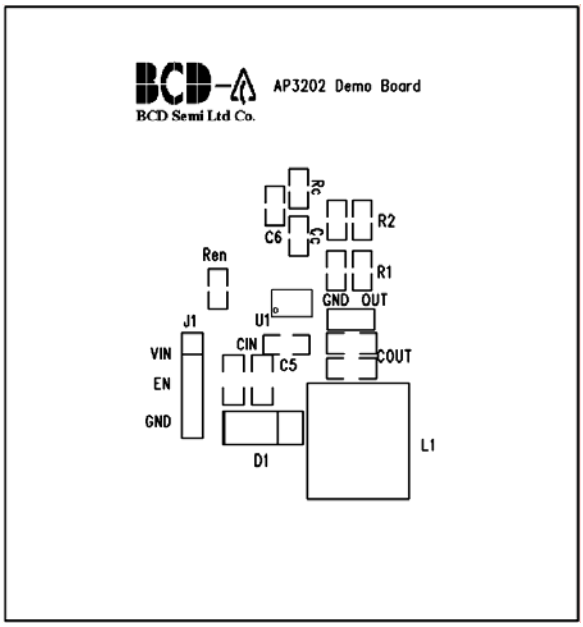

Figure 3. Top Silk Layer

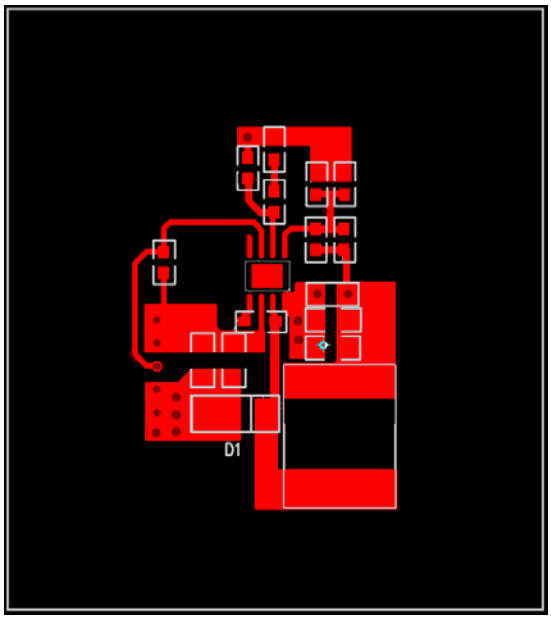

Figure 4. Top Layer

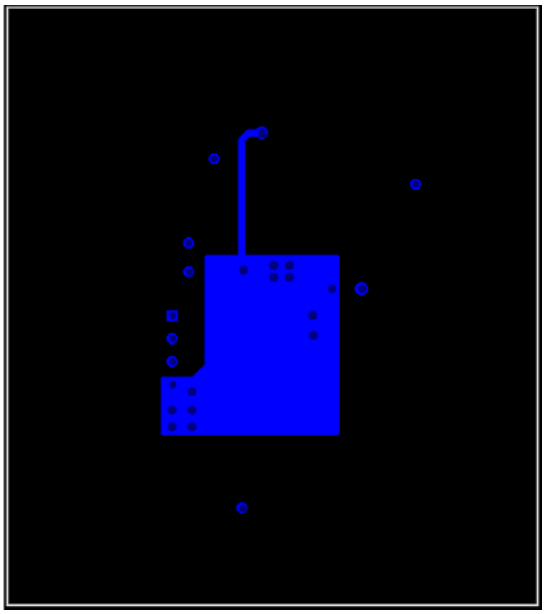

Figure 5. Bottom Layer