

## Load Switch

### Introduction.

Extended battery life is becoming more important in today's applications.

Consumers are demanding more complex features resulting in greater power demands in products such as laptop computers, mobile phones, etc. Load switching is an effective technique for disconnecting power to electronic subsystems, that are not required, extending battery life.

It is important that the load switch has minimal losses in order to maximise efficiency and extend battery life for the end user. Size is also critical, with the consumer requiring smaller, lighter portable equipment.

Using Zetex High Density MOSFETs or SuperSOT Transistors for load switching, high efficiency and reduced space can be achieved. This is because their low on-resistance or saturation voltage enable high current density in small packages.

### Theory of Operation.

Figure 1. shows a typical portable system architecture. The various sections of the system are selected when required, via the load switch. The power management circuitry controls the load switch and thus power to the relevant subsystem.

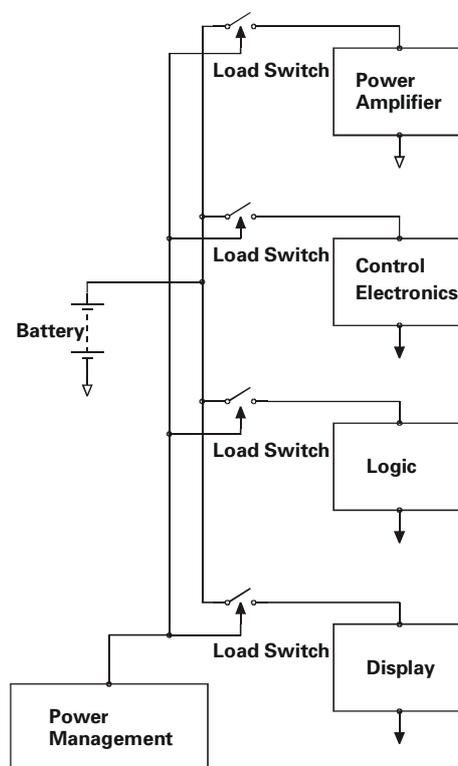
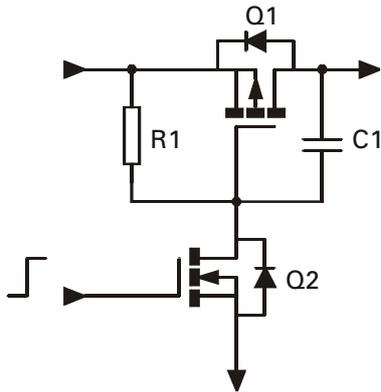


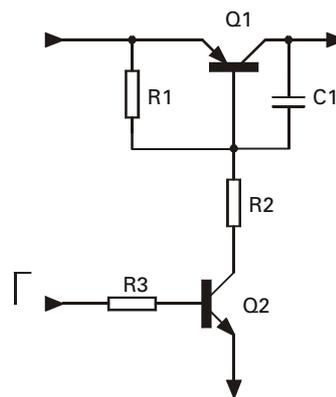
Figure 1.  
Typical Portable System Architecture.



**Figure 2a.**  
**Typical MOSFET Load Switch.**

Figures 2a and 2b are typical load switch schematics for MOSFET and bipolar technologies. The capacitors, C1, may not be required in some applications (see inrush current section).

The load switch consists of a P-Channel pass element, Q1 (PNP transistor for bipolar), which is controlled by a low power, logic level switch, Q2 (NPN transistor for bipolar). With a logic 'low' at the input to Q2, Q1 is held off via R1. When logic 'high' is at the input to Q2, Q1's gate is pulled to zero volts and is switched on, allowing power to the subsystem. Note that it is important, when using MOSFETs as load switches, to ensure that the input voltage is higher than the output voltage. The intrinsic body diode will conduct if forward biased which results in significant current flow. This could be a problem in multiple power source systems such as battery chargers where excess battery drain could be introduced.



**Figure 2b.**  
**Typical Bipolar Load Switch.**

#### Thermal Considerations.

Load switches are selected by their power handling capability and low on-state losses. Optimisation for the load switch is critical. If the junction temperature is increased the device could be damaged. Therefore it is important to ensure that the load switch is designed for its operating environment.

#### Design Example

This is a design example using the Zetex High Density MOSFET, ZXM64P02X. (Note 1)

Ambient temperature,  $T_a = 70^\circ\text{C}$ .

$I_{\text{steady-state(max)}} = 1\text{A}$ .

$V_{\text{GS}} = 5\text{V}$ .

$R_{\text{th(j-a)max}} = 69.4^\circ\text{C/W}$  (supplied by Zetex) (Note 2).

Now some general calculations can be made.

$$T_j = T_a + (R_{th(j-a)} \times P_d(\text{practical})) = \text{°C}$$
$$T_j = 70\text{°C} + (69.4\text{°C/W} \times 135\text{m}\Omega) = 79.4\text{°C}.$$

Power Dissipation,  
 $P_d(\text{maximum allowable}) =$   
 $(T_j(\text{max}) - T_a(\text{max})) / R_{th(j-a)} = \text{Watts}.$

Therefore,  
 $T_j = 79.4\text{°C}$  giving a 47% design margin.

$$P_d(\text{maximum allowable}) =$$
$$(150\text{°C} - 70\text{°C}) / 69.4\text{°C/W} = 1.152\text{W}.$$

Note 1. For bipolar transistors the same procedure can be used except that  $P_d(\text{practical}) = I_{\text{steady-state}} \times V_{CE(\text{sat})}$  @ 150°C.

For a MOSFET the on-resistance increases by 50% when the junction temperature reaches 150°C. Therefore assume worse case on-resistance.

Note 2. This figure is measured by mounting the device on a 25 x 25mm area of FR4 PCB of full copper. If you do not use the same area, derate using thermal derating graphs supplied by Zetex.

$$R_{DS(on)}\text{worse-case} =$$
$$1.5 \times R_{DS(on)}\text{max at } 25\text{°C} = \text{m}\Omega$$

### Inrush Current.

$$R_{DS(on)}\text{worse-case} =$$
$$1.5 \times 90\text{m}\Omega = 135\text{m}\Omega$$

Load switches which turn on into low ESR capacitors can have high inrush current, this can be detrimental to overall system performance and reliability. The inrush current transients are limited by the ESR of the output capacitor and the on-resistance of the pass element and can be in the order of several amperes. There are a number of ways in which to slow down the turn on of the device and resolve this problem. The simplest is to add a capacitor, C1, between the gate and drain (base and collector for bipolar) of the pass element, Q1, as shown in fig 2.

Where  $P_d(\text{practical}) =$   
 $I_{\text{steady-state}}^2 \times R_{DS(on)}\text{worse-case} = \text{W}.$

$$P_d(\text{practical}) = 1\text{A}^2 \times 135\text{m}\Omega = 135\text{mW}.$$

By comparing the absolute allowable power dissipation and the practical power dissipation you can see that the MOSFET would be suitable for this application.

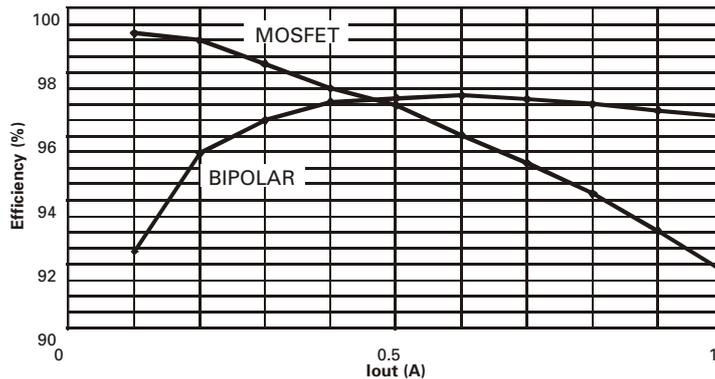
It is important to know the design margin in the event of future environment changes.

**Performance.**

In Figure 3, a comparison is performed between MOSFET and Bipolar technologies with equal die area.

The results clearly indicate that for a given area of silicon there is a point where the two technologies crossover. At the lower levels the base drive required by PNP Bipolar transistors dominates the losses in the pass element. As the load current increases and the ratio of base current to load current reduces the efficiency is seen to improve and hold up.

In a MOSFET the drive losses are negligible and therefore the device performs best at lower currents. As the load current increases the on-resistance has a larger effect on the losses and the efficiency falls off.



**Figure 3.**  
P-Channel and PNP. Optimised for 1A operation with equal die area.