AN1157

Understanding Thermal Resistance in the Real World

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Introduction

There can be significant differences between the thermal characteristics stated on a device datasheet and what actually happens in a real-world application. Semiconductor manufacturers usually provide thermal resistance values for Junction to Case ($R_{\theta JC}$) and Junction to Ambient ($R_{\theta JA}$); although these are extremely useful parameters to estimate a device power handling capability, there can still be a disconnection between those figures and reality.

This note will illustrate how the thermal data provided in manufacturer's datasheets compare to real world applications and will also discuss the relative thermal performance of Diodes PowerDI5060 package against similar competitor packages.

Thermal Resistance and MOSFET packages

Junction to Case thermal resistance is a MOSFET's intrinsic characteristic that refers to the thermal resistance inside the device package. $R_{\theta JC}$ is a fixed value defined by die size and package design. This means that $R_{\theta JC}$ deals with the power dissipated in the device only. For the purpose of this application note $R_{\theta JC}$ refers to the thermal resistance from the junction to the bottom of the exposed pad. On the other hand, Junction to Ambient thermal resistance is made up of all thermal resistance involved in the heat flow path from the die to the outside environment and it is much more dependent on the board's layout and heat sinking capability. For example, if we modify the size of copper area where heat is dissipated $R_{\theta JA}$ is expected to change. The figure below gives a visual representation of the thermal resistive network inside a MOSFET.

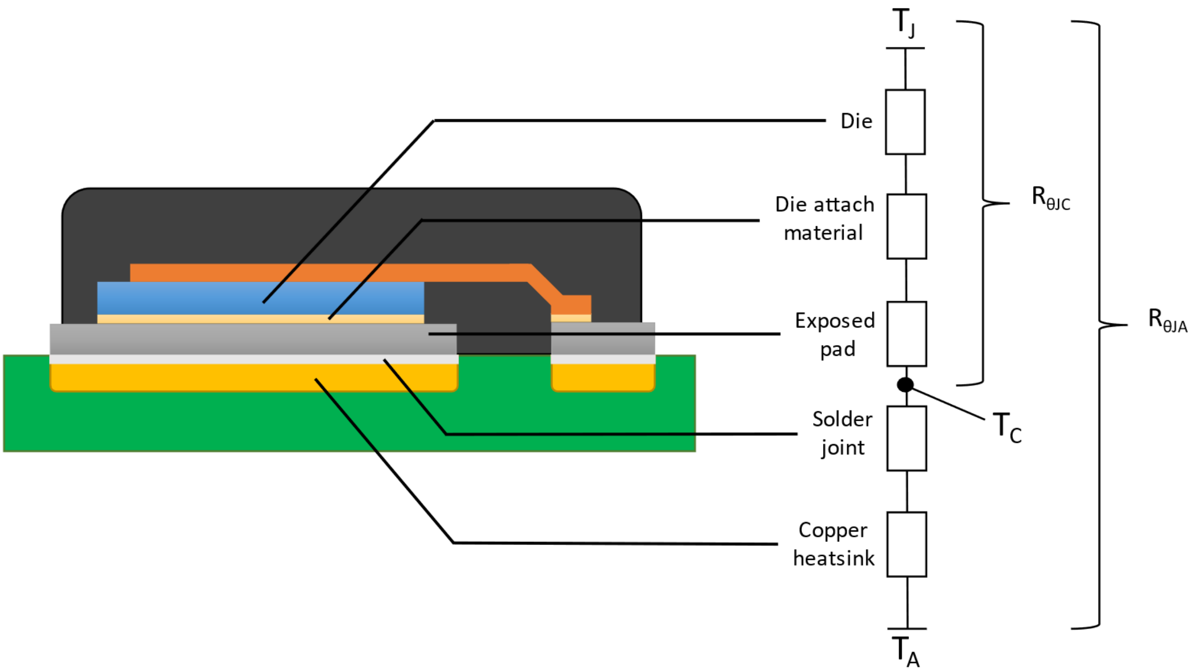


Figure 1. Cross-section of a power MOSFET package and thermal resistive network

As most of the heat generated by the MOSFET will be dissipated through the copper heatsink on the PCB, it follows that the larger the heatsink area is the lower $R_{\theta JA}$ will be. Conversely, the opposite happens if the area is reduced. Thus, $R_{\theta JA}$ is the dominant thermal resistance in an application.

To understand the influence of $R_{\theta JA}$ in a device thermal behavior MOSFETs of the DMTH family in 3 different packages were tested:

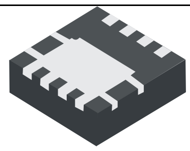
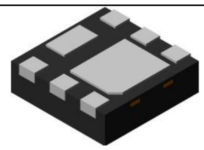
Device name	DMTH41M8SPSQ	DMTH43M8LFGQ	DMTH4008LFDFWQ
Package	 PowerDI5060-8	 PowerDI3333-8	 DFN2020-6
Package dimensions (mm)	5x6	3x3	2x2
Drain tab dimensions (mm)	4.0x3.7	2.3x1.6	1.0x1.2
Datasheet $R_{\theta JC}$ (°C/W)	1.0	2.3	14.8
Datasheet $R_{\theta JA}$ (°C/W)	49	57.8	153

Table 1. MOSFETs used in test

All devices were mounted on multiple 1oz copper, single-layer, FR-4 substrate boards with no additional heatsink attached. The drain pad area in each board ranged from the minimum allowed by package to a 25.4 × 25.4mm (1-inch) copper pad.

Thermal characterisation was performed with a dedicated thermal analyzer to find the temperature coefficient and consequently the Junction to Ambient thermal resistance of each board. A graph of thermal resistance in function of drain pad area was plotted with the collected data.

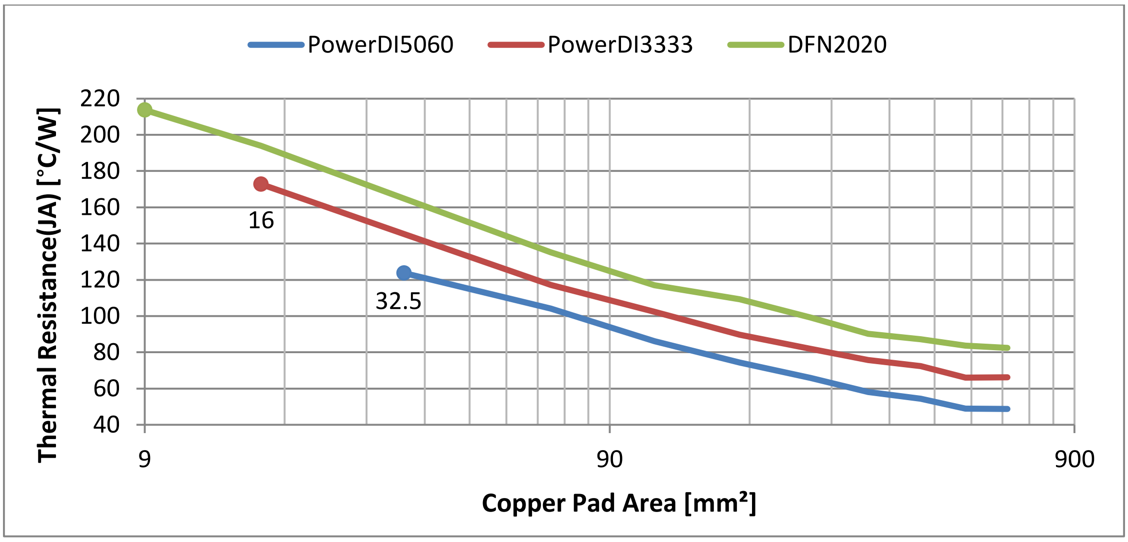


Figure 2. Junction to Ambient Thermal Resistance—$R_{\theta JA}$ vs Pad Area

We can see from Figure 2 a continuous decrease in thermal resistance as the copper area gets larger. The lowest $R_{\theta JA}$ is achieved with the largest copper area regardless of the package. Note that $R_{\theta JA}$ values scale up as the package gets smaller though a fairly constant difference is kept between the three datasets all along. Since all devices are tested under the same conditions this difference can only be due to package size and the die itself, in other words its $R_{\theta JC}$.

Thermal characterisation results also allow us to know the steady-state power dissipated in the board. The following graph shows the power dissipation according to the previous results.

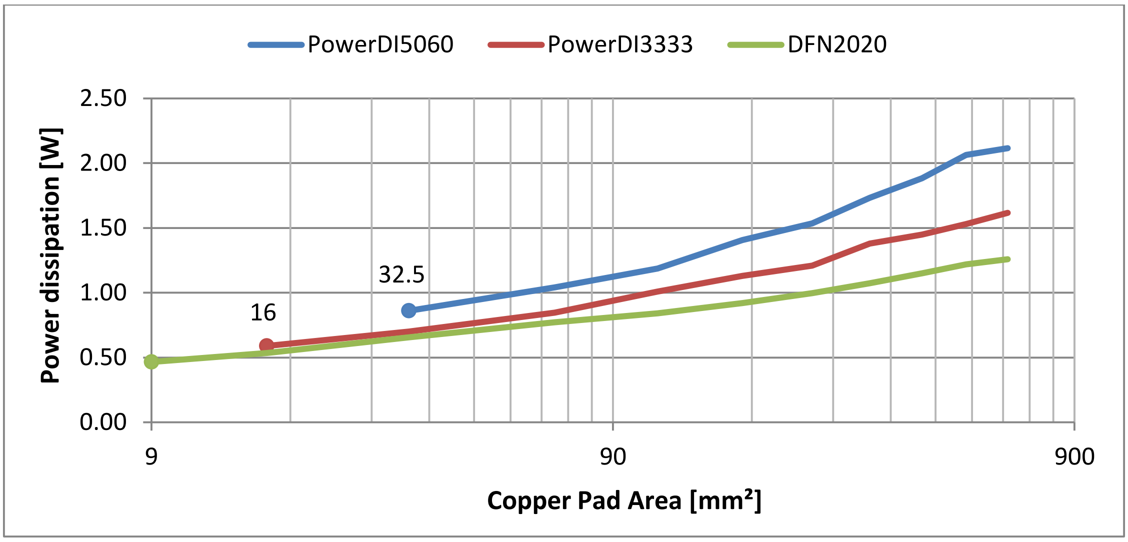


Figure 3. Power Dissipation—Pd vs. Pad Area

It can be seen that PowerDI5060 exhibits the best power dissipation capability of all 3 packages reaching 2.12W on the largest drain pad. Due to its size, the device can hold greater currents allowing for more power dissipation. Likewise, heat will spread more effectively over its larger area in comparison with other packages.

In the case of DFN2020 and PowerDI3333, the power dissipation difference on a drain pad of up to 70mm² is less than 100mW growing to a maximum of 360mW at the largest area.

Power dissipation for each device can be calculated with the following formula:

$$P_D = \frac{T_{Jmax} - T_{amb}}{R_\theta}$$

Where T_{Jmax} is the maximum temperature rating of the junction inside the die, T_{amb} is assumed to remain constant at 25°C and R_θ in this case is $R_{\theta JA}$.

The power dissipation of the 3 MOSFETs was calculated obtaining the following results:

PowerDI5060-8	3.06W
PowerDI3333-8	2.27W
DFN2020-6	1.81W

Table 2. Calculated Power Dissipation

These results appear to be close to datasheet figures. However, it is important to remember that these come from a theoretical calculation. Figure 3 shows that the actual power dissipation is lower than the calculated value. The main reason being the different conditions and environment in which thermal testing was performed.

Thermal management techniques are normally used to greatly reduce the thermal resistance of a PCB and its components. The addition of GND planes, thermal vias and extra copper reduces the $R_{\theta JA}$ and so allows for greater power dissipation. It is the case with PowerDI5060 that although the same $R_{\theta JA}$ value of the datasheet was obtained in test, the power dissipation shown in datasheet is about 1W above the measured value.

Comparison under same conditions of PowerDI5060 and competitor

To have a better understanding of how thermal characteristics affect real-world performance we compared Diodes' DMTH41M8SPSQ N-channel MOSFET with a competitor component of similar characteristics. Both devices use copper clip bonding rather than bond wires to common drain and come in a same-size package.

	Package	V_{DS}	I_D	$R_{\theta JC}$	$R_{DS(ON)}$
DMTH41M8SPSQ	PowerDI5060	40V	100A	1.0°C/W	1.8mΩ
Competitor device	"Power SO-8"	40V	120A	0.5°C/W	1.7mΩ

Table 3. Comparison between common MOSFET parameters

The $R_{\theta JC}$ of DMTH41M8SPSQ is 1.0°C/W while the competitor's part claims a $R_{\theta JC}$ of 0.5°C/W on its datasheet and does not provide a $R_{\theta JA}$ value. The omission of this parameter in the datasheet leads the designer to make the common mistake of using $R_{\theta JC}$ when calculating power dissipation. Recalling Figure 1, we saw that $R_{\theta JA}$ is already comprised of $R_{\theta JC}$ so the correct value to use in calculation is $R_{\theta JA}$. The graph below shows the actual $R_{\theta JA}$ of both devices under the same conditions.

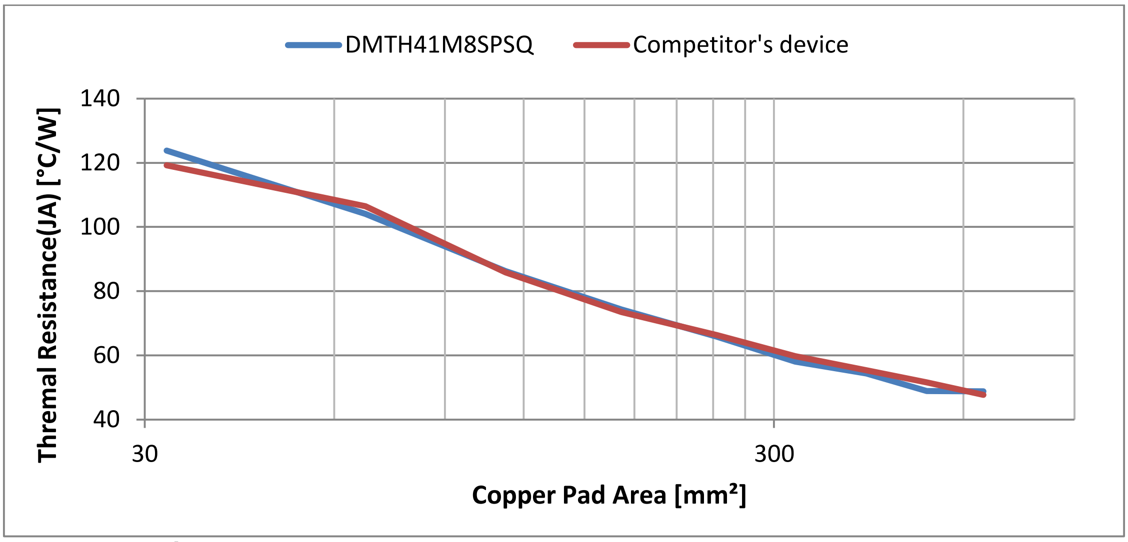


Figure 4. $R_{\theta JA}$ vs. Pad Area—DTMH41M8SPSQ and competitor's device

It can be seen that apart from the initial values there is minimal difference in $R_{\theta JA}$ along the trend; at the largest copper pad area the difference is less than 1.0°C/W suggesting that both devices share a similar thermal behavior.

The power dissipation formula provided before was used again to compare the performance of both devices. Taking the $R_{\theta JA}$ values from Figure 4 at maximum area we obtain:

$P_D = \frac{175-25}{48.776} = 3.07W$ for DMTH41M8SPSQ

$P_D = \frac{175-25}{47.713} = 3.14W$ for competitor's device

Where the power dissipation difference is minimal just as with thermal resistance in Figure 4. Another test was performed with proper equipment to measure the actual power dissipation.

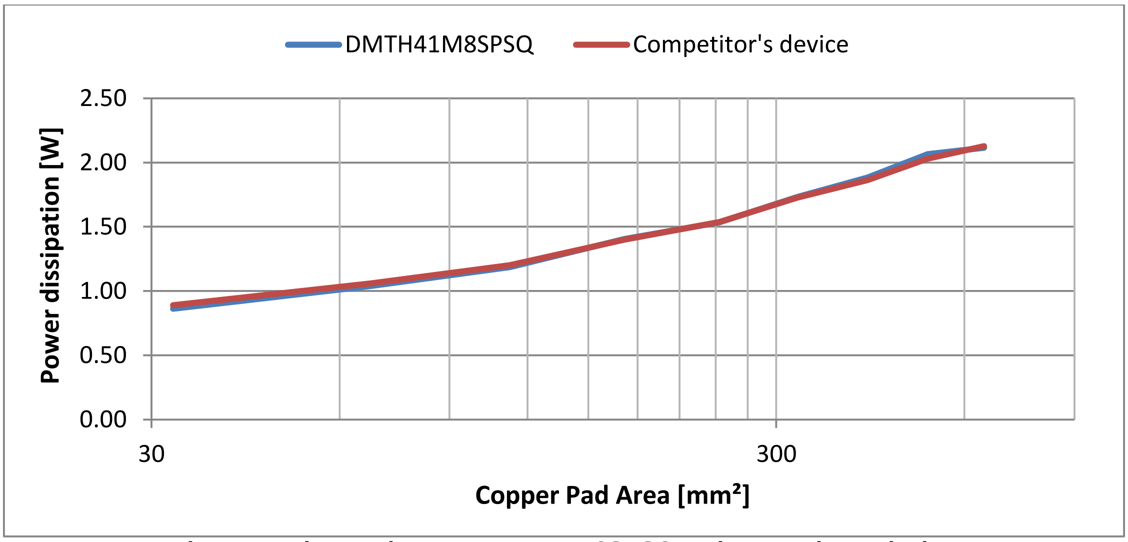


Figure 5. Pd vs Pad Area—DTMH41M8SPSQ and competitor's device

The graph above shows that the resulting power dissipation lines overlap making the difference barely noticeable. This only confirms that the performance of both devices is nearly the same.

So far, both graphical and numerical results tell that neither device can be considered 'thermally superior' but then, what is the difference between these two?

A second test was performed, this time to compare the $R_{\theta JC}$ of both MOSFET's. The devices were mounted on a piece of a solid copper plate that approximates an infinite heatsink and the same amount of power was dissipated through them. The device was kept at constant ambient temperature with a computerized thermostat, this way the only thermal resistance obtained was between the die and soldering point.

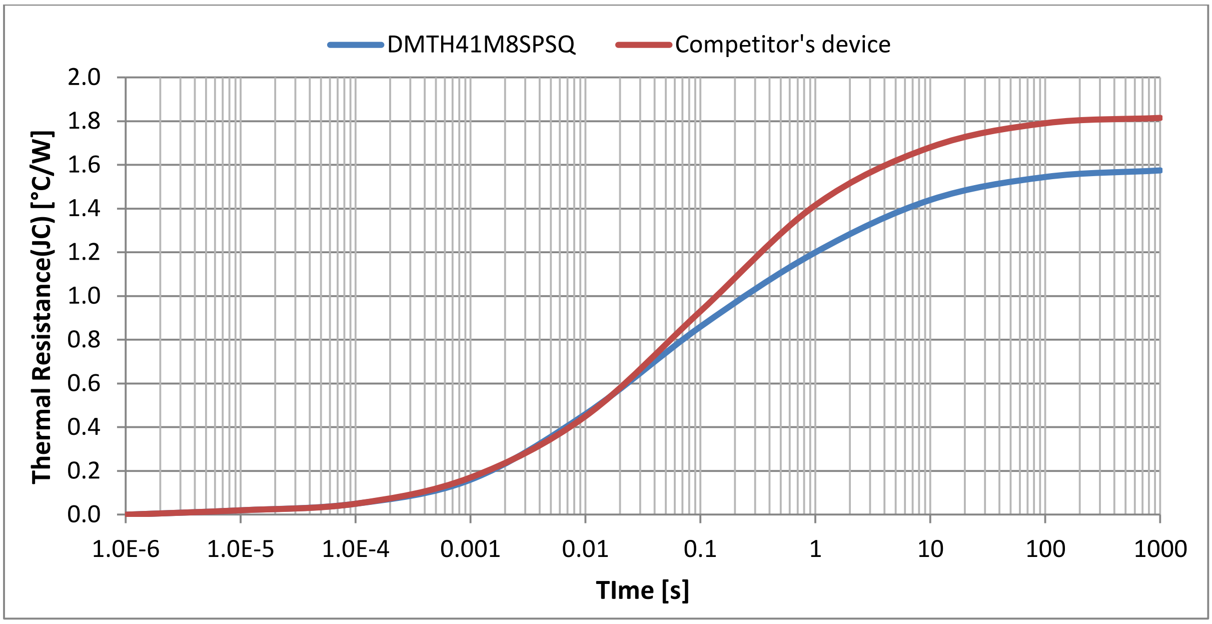


Figure 6. Junction to Case Thermal Resistance—$R_{θJC}$ vs Single Pulse Time

The graph above shows $R_{θJC}$ recorded for various single pulses, where at steady state DMTH41M8SPSQ has an $R_{θJC}$ value of 1.57°C/W while competitor's device 1.81°C/W. The behavior of both devices is similar for pulses of less than 30ms. Although the graph confirms that there is an $R_{θJC}$ difference of 0.24°C/W, it turns out to be half of what can be calculated with datasheet values.

In a real application, most of the heat power is going to be dissipated through the PCB where the dominant Thermal Resistance is $R_{θJA}$ because of its larger magnitude compared to $R_{θJC}$. In our comparison, both devices showed a similar behavior in Thermal Performance and almost identical results in Power Dissipation ensuring that a small difference in $R_{θJC}$ has little to no impact in actual applications.

Conclusion

It is true that datasheet values give precise information about a device, but when it comes to thermal information this has to be treated as reference only and may not reflect the real thermal behaviour of a device. Ambient conditions vary depending on the application and apart from thermal resistance values found in datasheets; package size and board design also play an important role in thermal resistance and consequently in power dissipation. Not only that, various techniques can also be used to manage heat dissipation on a board and its components.

As it could be seen, in most applications $R_{θJA}$ is dominated by PCB effects while $R_{θJC}$ is just a small part of the overall system. Although $R_{θJC}$ easily provides a consistent measure on a device level it does not reflect the key aspect of and actual application which is the device thermal performance at a system level.

In the case of devices with same-sized packages, performance resulted slightly different from what could be assumed by only reading the datasheet. In our comparison, the thermal behavior and power dissipation capability of two physically similar devices from different manufacturers was proved to be the same. This would be true for any other 5x6 packages if they were put under similar conditions. Thus, their small difference in $R_{θJC}$ does not necessarily mean better or worse performance in the real world.

It its worth reminding that as complex as it is, thermal information is based on empirical results that were measured under specific test conditions and has to be used as a design aid and not as absolute values.